SIEMENS

ICs for Communications

Signal Processing Codec Filter
SICOFI®, SICOFI®-2

User's Manual 03.92

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Introduction

The following chapters inform you about the technical data and programming of the Signal Processing Codec Filter SICOFI® / SICOFI®-2 PEB 2060/2260 and describe the hardware and software tools. Application notes show you how to use and work with the SICOFI family in a given application.

In order to get an overview of the architecture, the devices and the tools, we suggest to start having a look at the ’General Overview on Architectures and Devices’ as well as ’Development Support Tools’.

Detailed descriptions can be found in the other chapters.

For more information on related products and quality issues we provide the information on literature**.**

1 Type-Designation Code for ICs

IC type designations are based on the European Pro Electron system. The code system is explained in the Pro Electron brochure D 15*), edition 1988.

*) Available from Pro Electron
Avenue Louise, 430 (B.12)
B-1050 Bruxelles, Belgium

2 Mounting Instructions

Plastic Packages for Insertion

The pins of the packages are bent downwards by an angle of 90° and fit into holes on a grid of 2.54 mm and with diameters of between 0.7 and 0.9 mm. The dimension x is shown in the corresponding drawing of the package.

The bottom of the package will not touch the circuit board after insertion because the pins have shoulders just below the package **(see figure 1)**.

After insertion of a package on a board it is advisable to bend the ends of two pins at an angle of approx. 30° to the board so that the package does not have to be pressed down during soldering.
Plastic packages are soldered on the board on the side facing away from the package.

The maximum permissible soldering temperature is 260 °C (max.10 s) when using a solder bath, e.g. wave soldering, and 350 °C (max. 3 s) when using a soldering iron.

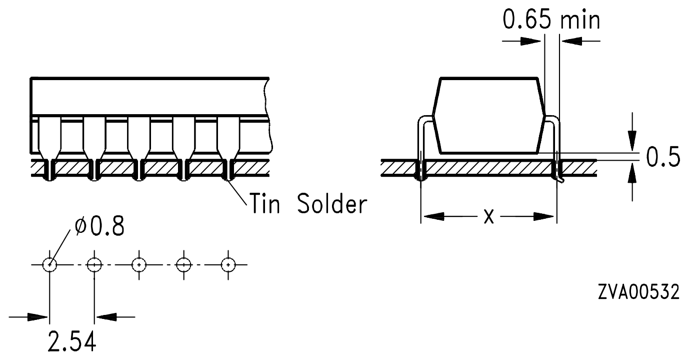


Figure 1

Plastic Packages (P-DSO and P-LCC) for Surface Mounting (SMD)

Reflow soldering: for a device temperature of 215 °C max. soldering time 2 x 40 s (typical figure for vapor-phase soldering)

Wave soldering: soldering temperature 260 °C, soldering time max. 10 s.

Soldering iron: the minimum thermal stress, based on experience, is at a soldering temperature of 350 °C (soldering time ≤ 3 s)

Storage and Pretreatment of SMD ICs

The components should be stored in a dry place. Some large and specially identified plastic ICs have to be processed in a dry condition. This is produced by dry packing or by means of a separate drying process shortly before they are processed (e.g. 16 h at 125 °C)

3 Processing Guidelines for ICs

Integrated circuits (ICs) are **e**lectro**s**tatic-**s**ensitive (ESS) devices. The demand for greater packing density has led to smaller structures on semiconductor chips, with the result that today every IC, whether bipolar, MOS, or CMOS, has to be protected against electrostatics.
MOS and CMOS devices generally have integrated protective circuits and it is virtually impossible for them to be destroyed by purely static electricity. On the other hand, there is acute danger from **e**lectro**s**tatic **d**ischarges (ESD).

Of the multitude of possible sources of discharge, charged devices should be mentioned in addition to charged persons. Low-resistive discharges can produce peak powers amounting to kilowatts.

For the protection of devices the following principles should be observed:

a) Reduction of charging voltage, below 200 V if possible.
Means which are effective here are an increase in relative humidity to ≥ 60 % and the replacement of highly charging plastics by antistatic materials.

b) With every kind of contact with the device pins a charge equalization is to be expected. This should always be highly resistive (ideally $R = 10^6$ to 10^9 Ω).

All in all this means that ICs call for special handling, because uncontrolled charges, voltages from ungrounded equipment or persons, surge voltage spikes and similar influences can destroy a device. Even if devices have protective circuits (e.g. protective diodes) on their inputs, the following guidelines for their handling should nevertheless be observed.

Identification

The packing of ESS devices is provided with the following label by the manufacturer:

Scope

The guidelines apply to the storage, transport, testing, and processing of all kinds of ICs, equipped and soldered circuit boards that comprise such components.

Handling of Devices

1 ICs must be left in their containers until they are processed.

2 ICs may only be handled at specially equipped work stations. These stations must have work surfaces covered with a conductive material of the order of 10^6 to10^9 Ω/cm.

3 With humidity of > 50 % a coat of pure cotton is sufficient. In the case of chargeablesynthetic fibers the clothing should be worn close-fitting. The wrist strap must be worn snugly on the skin and be grounded across a resistor of 50 kΩ to 100 kΩ.

4 If conductive floors, $R = 5 \times 10^4$ to 10^7 Ω are provided, further protection can be achieved by using so-called MOS chairs and shoes with a conductive sole ($R \approx 10^5$ to 10^7 Ω).

5 All transport containers for ESS devices and assembled circuit boards must first be brought to the same potential by being placed on the work surface or touched by the operator before the individual devices may be handled. The potential equalization should be across a resistor of 10^5 to 10^8 Ω.

6 When loading machines and production devices it is necessary to ensure that the devices do not come out of the transport magazine charged and that they are not damaged by touching metal, e.g. parts of a machine.

Example 1 conductive (black) tubes.
The devices may be destroyed in the tube by charged persons or come out of the tube charged if this is emptied by a charged person. Conductive tubes may only be handled at ESS work stations (high-resistance work-station and person grounding).

Example 2) anti-static (transparent) tubes.
The devices cannot be destroyed in the tube by charged persons (there may be a rare exception in the case of custom ICs with unprotected gate pins). The devices can be endangered as in 1) when the tube is emptied if the latter, especially at low humidity, is no longer sufficiently anti-static after a long period of storage (> 1 year).

In both cases damage can be avoided by discharging the devices across a grounded adapter of high-resistance material ($\approx 10^6$ to 10^8 Ω/cm) between the tube and the machine.

The use of metal tubes – especially of anodized aluminium – is not advisable because of the danger of low-resistance device discharge.

Storage

ESS devices should only be stored in identified locations provided for the purpose.

During storage the devices should remain in the packing in which they are supplied. The storage temperature should not exceed 30 °C.

Transport

ESS devices in approved packing tubes should only be transported in suitable containers of conductive or longterm anti-static-treated plastic or possibly unvarnished wood. Containers of both high-charging plastic or very low-resistance materials are unsuitable.

Transfer cars and their rollers should exhibit adequate electrical conductivity ($R < 10^6\ \Omega$). Sliding contacts and grounding chains will not reliably eliminate charges.

Incoming Inspection

In incoming inspection the above guidelines should be observed. Otherwise any right to refund or replacement if devices fail inspection may be lost.

Material and Mounting

1 The drive belts of machines used for the processing of the devices, in as much as they come into contact with them (e.g. bending and cutting machines, conveyor belts), should be treated with anti-static spray (e.g. anti-static spray 100 from Kontaktchemie). It is better, however, to avoid the contact completely.

2 If ESS devices have to be soldered or desoldered manually, soldering irons with thyristor control may not be used. Siemens EMI-suppression capacitors of the type B 81711-B31...–B36 have been proven very effective against line transients.

3 Circuit boards fitted and soldered with ESS devices are always to be considered as endangered.

Electrical Tests and Application Circuit

1 The devices should be processed with observation of these guidelines. Before assembled and soldered circuit boards are tested, remove any shorting rings.

2 The sockets or integrated circuits must not be conducting any voltage when individual devices or assembled circuit boards are inserted or withdrawn, unless works specifications state otherwise. Ensure that the test devices and power supplies do not produce any voltage spikes, either when being turned on and off in normal operation or if the power fuse blows or other fuses respond.

3 When supplying bipolar integrated circuits with current, the negative voltage ($-V_S$ or GND) has first to be connected. In general, an interruption of this potential during operation is not permissible.

4 Signal voltages may only be applied to the inputs of ICs when or better after the supply voltage is turned on. They must be disconnected when or better before the supply voltage is turned off.

5 Power supplies of integrated circuits are to be blocked as near as possible at the supply terminals of the IC. With bipolar ICs it is recommended to use a low-inductance electrolytic capacitor or at least a paralleled ceramic capacitor of 100 nF to 470 nF for example.

Using ICs with high output currents, the necessary value of the electrolytic capacitor must be adapted to the test or application circuit. Transient behavior and dynamic output resistance of the power supplies, line inductances in the supply and load circuit and in particular inductive loads or motors have to be considered.
When switching off line inductances of inducitve loads, the stored power has to be consumed externally, unless otherwise specified (e.g. by an electrolytic capacitor, diodes, Z-diodes or the power supply). Also a switching off of the supply voltage prior to the load rejection should be taken into account.

6 ICs with low-pass character of the output stages (e.g. PNP drivers or PNP/NPN end-stages), normally need an additional external compensation at the output. This applies particularly to complex loads. The output of AF power amplifiers is compensated by the Boucherot element. In individual cases, bridge circuits only need a capacitance for bypassing the load. Depending on the application it is, however, also recommended to connect one capacitor from each output to ground.

7 Observe any notes and instructions in the respective data books.

Packing of Assembled PC Boards or Flatpack Units

The packing material should exhibit low volume conductivity:
$10^5\ \Omega/\text{cm} < p < 10^{10}\ \Omega/\text{cm}$.

In most cases – especially with humidity of > 40 % – this requirement is fulfilled by a simple corrugated board.

Better protection is obtained with bags of conducitve polyethylene foam (e.g. RCAS 1200 from Richmond of Redlands, California).

You should always ensure that different boards cannot touch.

In special cases it may be necessary to provide protection against strong electric fields, such as can be generated by conveyor belts for example.

For this purpose a sheath of aluminium foil is recommended, although direct contact between the film and the PCB must be avoided.

Cardboard boxes with an aluminium-foil lining, such as those used for shipping our devices, are available from Laber of Munich.

Ultrasonic Cleaning of ICs

The following recommendation applies to plastic packages. For cavity packages (metal and also ceramic) separate regulations have to be observed.

Freon and isopropyl alcohol (trade name: propanol) can be used as solvents. These solvents can also be used for plastic packages because they do not eat into the plastic material.

An ultrasonic bath in double halfwave operation is advisable because of the low component stress.

The ultrasonic limits are as follows:

sound frequency	f > 40 kHz
exposure	t < 2 min
alternating sound pressure	p < 29 kPa
sound power	N < 0.5 W/cm^2/liter

4 Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

5 Quality Assurance

Quality Assurance System

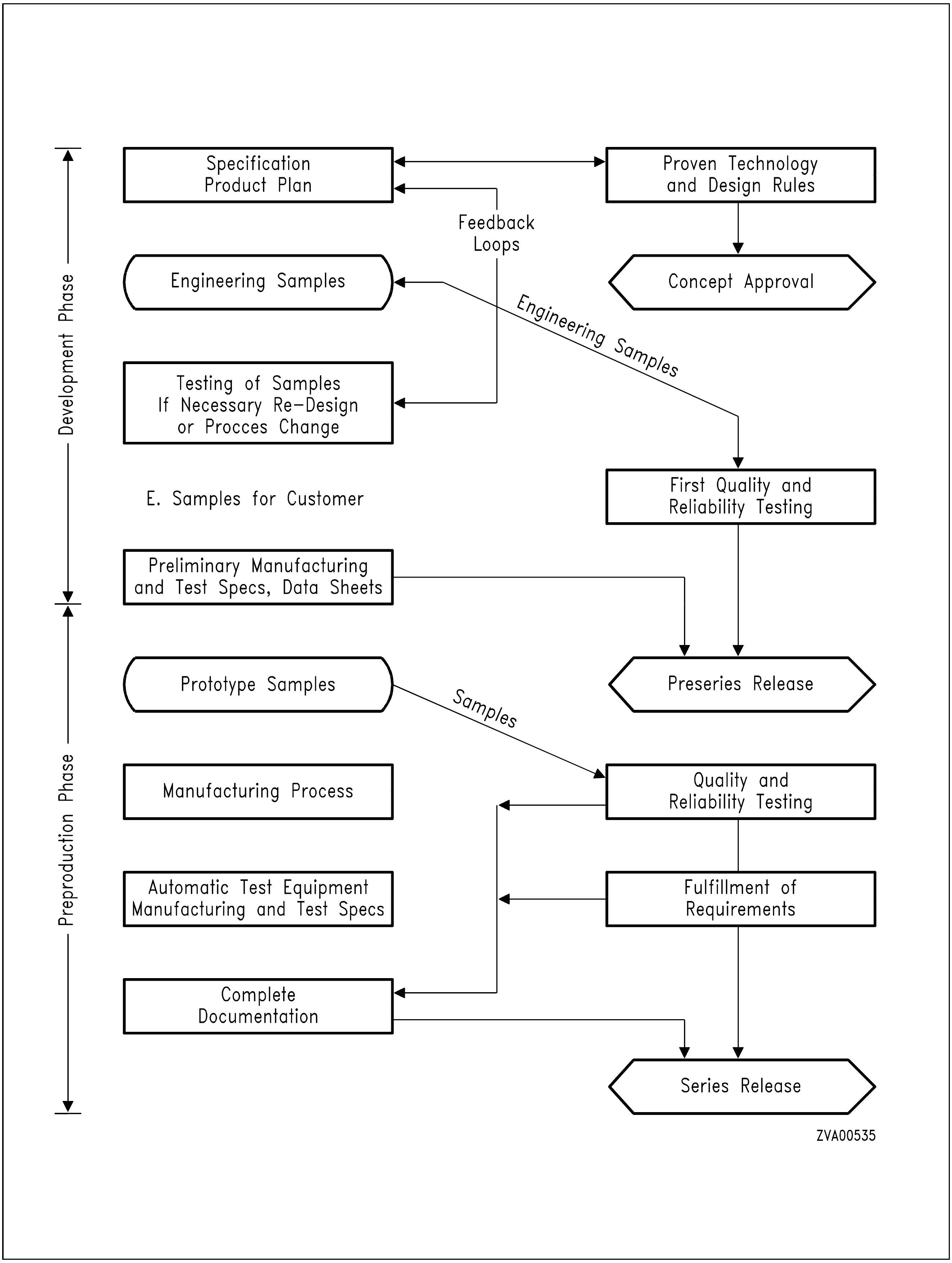
The high quality and reliability of integrated circuits from Siemens are the results of carefully managed design and production which is systematically checked and controlled at each stage.
The procedures are subject to a quality assurance system; full details are given in the brochure "Quality Assurance – Integrated Circuits".

Figure 1 and **2** show the most important stages of Quality Assurance (QA) system. QA departments independent of production and development are responsible for the selected measures, acceptance procedures and information feedback loops. Operating QA departments have state-of-the-art test and measuring equipment at their disposal, work according to approved methods of statistical quality control, and are provided with facilities for accelerate life and environmental tests used for both qualification and routine monitoring tests.

The latest methods and equipment for preparation and analysis are employed to achieve continuity of quality and reliability.

Conformance

Each integrated circuit is subjected to a final test at the end of the production process. These are carried out by computer-controlled, automatic test systems because hundreds of thousands of operating conditions as well as a large number of static and dynamic parameters have to be considered. Moreover, the test systems are extremely reliable and reproducible. The QA department carries out a final check in the form of a lot-by-lot sampling inspection to additionally ensure this minimum percent defectives to ensure statistically that the PDA of released lots is less than the AQL agreed. Sampling inspection is performed in accordance with the inspection plans of DIN 40 080, as well as of the identical MIL-STD-105 or IEC 410.



Specification
Product Plan
Proven Technology
and Design Rules
Feedback
Loops
Engineering Samples
Concept Approval
Engineering Samples
Testing of Samples
If Necessary Re–Design
or Procces Change
First Quality and
Reliability Testing
E. Samples for Customer
Preliminary Manufacturing
and Test Specs, Data Sheets
Development Phase
Prototype Samples
Preseries Release
Samples
Manufacturing Process
Quality and
Reliability Testing
Automatic Test Equipment
Manufacturing and Test Specs
Fulfillment of
Requirements
Complete
Documentation
Series Release
Preproduction Phase
ZVA00535

Figure 2

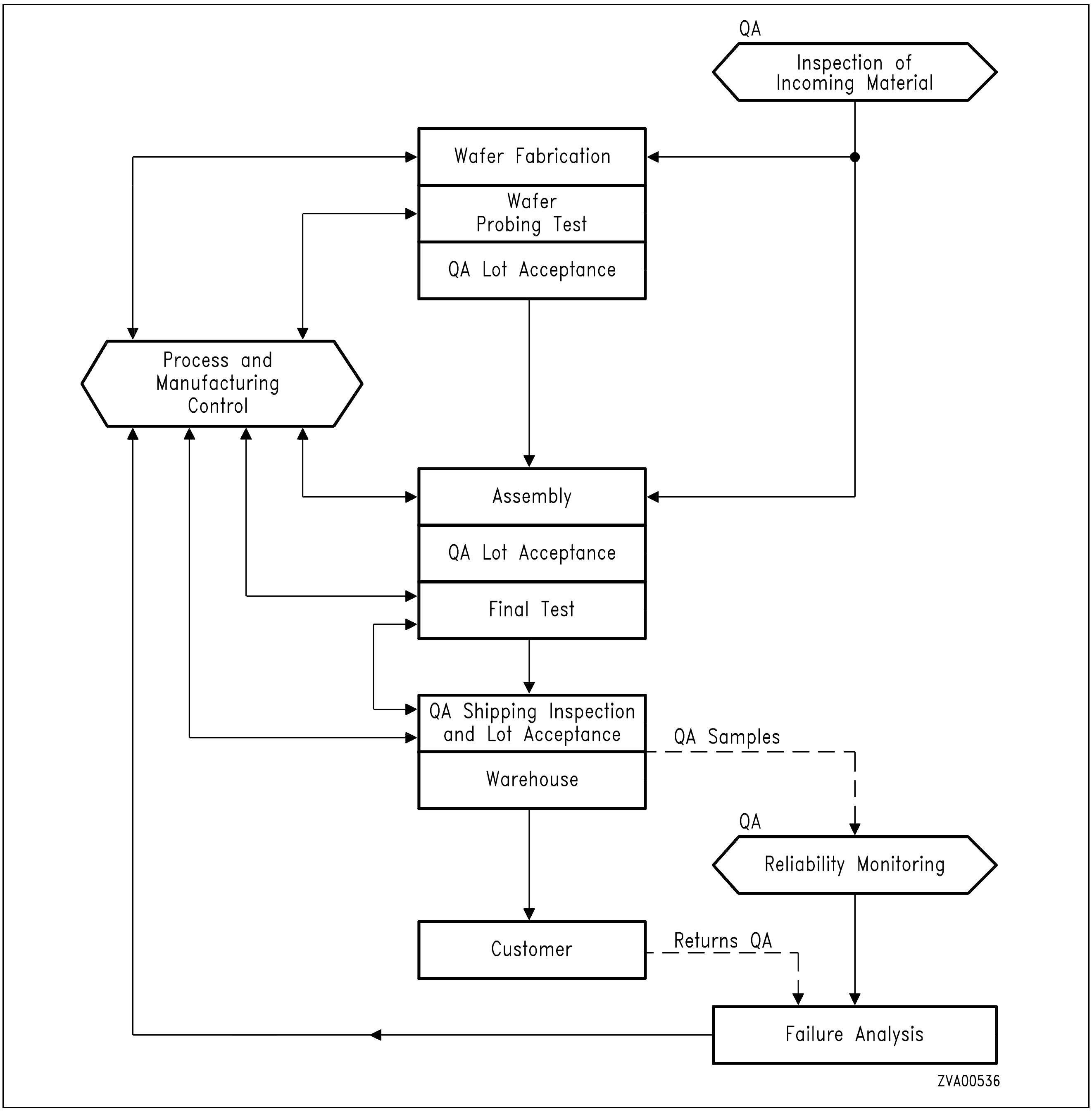


Figure 3

Reliability

Measures Taken During Development

The reliability of ICs is already considerably influenced at the development stage. Siemens has, therefore, fixed certain design standards for the development of circuit and layout, e.g. specifying minimum width and spacing of conductive layers on a chip, dimensions and electrical parameters of protective circuits for electrostatic charge, etc. An examination with the aid of carefully arranged programs operated on large-scale computers, guarantees the immediate identification and elimination of unintentional violations of these designs standards.

In-Process Control During Production

The manufacturing of integrated circuits comprises several hundred production steps. As each step is to be executed with utmost accuracy, the in-procress control is of outstanding importance. Some processes require more than a hundred different test measures. The tests have been arranged in a manner that the individual steps of the process can be reproduced continuously.

The decreasing failure rates reflect the persistent effort in this direction; in the course of the years they have been reduced considerably despite an immense rise in IC complexity.

Reliability Monitoring

The general course of the IC failure rate versus time is shown by a so-called "bathtub" curve. The failure rate has its peak during the first few operating hours (early failure period). After the early failure period has decayed, the "constant" failure rate period starts during which the failures may occur at an approximately uniform rate. This period ends with a repeated rise of the curve during the wear-out failure period. For ICs, however, the latter period usually lies far beyond the service life specified for the individual equipment.

Reliability tests for ICs are usually destructive examinations. They are, therefore, carried out with samples. Most failure mechanisms can be accelerated by means of higher temperatures. Due to the temperature dependence of the failure mechanisms, it is possible to simulate future operational behavior within a short time by applying high temperatures; this is called life test.

The acceleration factor *B* for the life test can be obtained from the Arrhenius equation

$$B = \exp\left(\frac{E_A}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right)$$

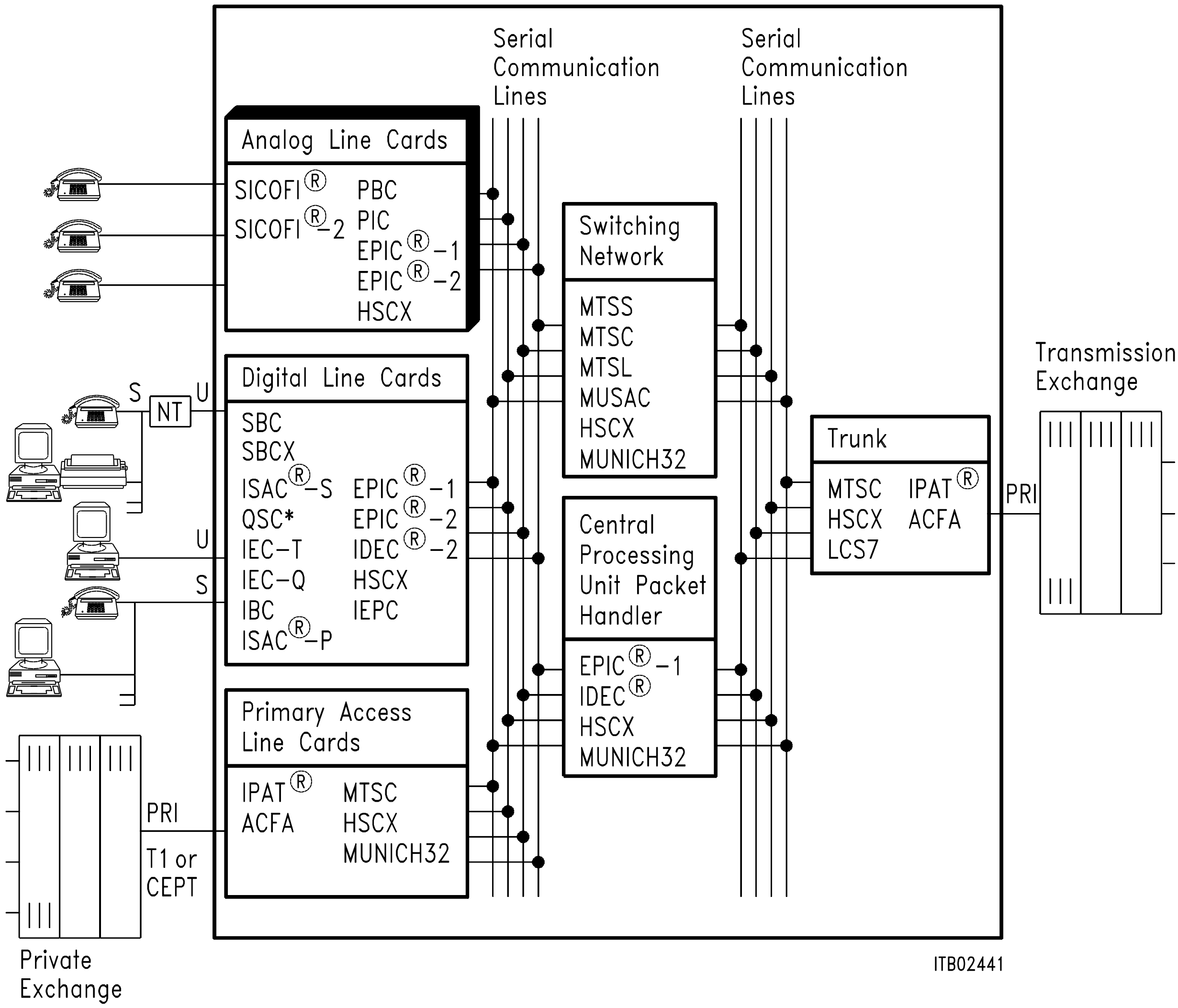
where T_2 is the temperature at which the life test is performed, T_1 is the assumed operating temperature, and *k* is the Boltzmann constant.

Important for factor B is the activation energy E_A. It lies between 0.3 and 1.3 eV and differs considerably for the individual failure mechanisms.

For all Siemens ICs, the reliability data gained from life tests are converted to an operating temperature of T_A = 55 °C, assuming an average activation energy of 0.5 eV. The acceleration factor for life tests at 125 °C is thus 24, compared with operational behavior. This method also considers failure mechanisms with low activation energy, i.e. which are only slightly accelerated by the temperature effect.

Various reliability tests are periodically performed with IC types that are representative of a certain production line – this is described in the brochure "Quality Assurance-Integrated Circuits". Such tests are e.g. humidity test at 85 °C and 85 % relative humidity, pressure cooker test, as well as life tests up to 1000 hours and more. Test results are available in the form of summary reports.

1 General Exchange Architecture



1.1 Analog Line Cards

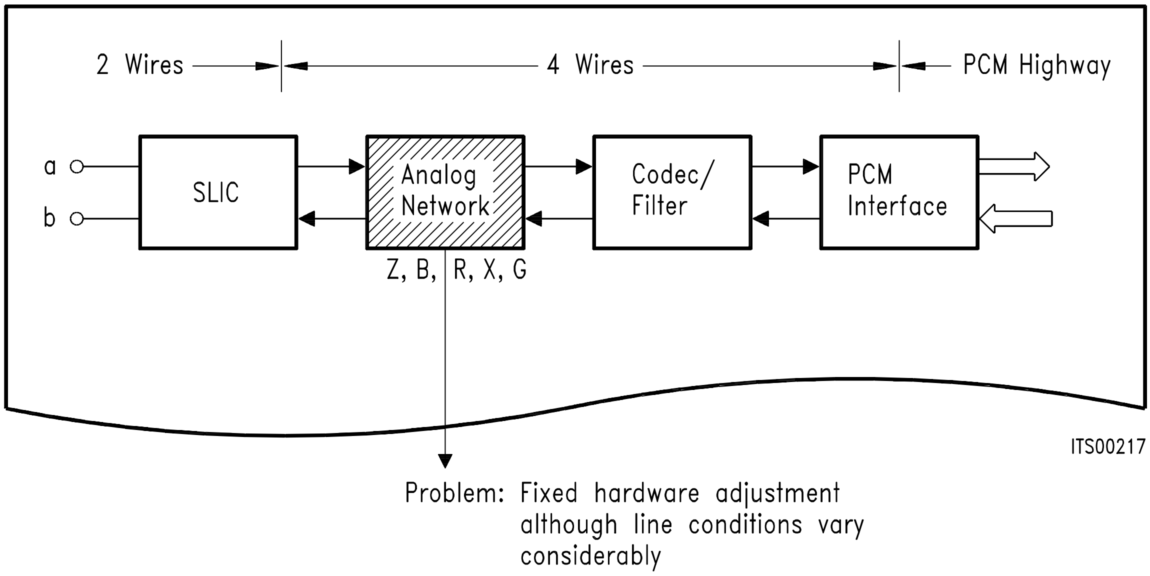
In a digital exchange system the subscriber line boards provide the link between the subscriber and the switching network. The basic functions of analog line boards are known under the acronym BORSHT (**b**attery, **o**vervoltage, **r**inging, **s**upervision, **h**ybrid, **t**esting). Moreover, further important tasks are voice frequency band limitation, analog to digital conversion into time discrete digital equivalents, time-slot assignment on the PCM highways and handling of signaling and control information.

Usual implementation uses two PCM ports and one µP interface per subscriber line leading to a large amount of wiring and, thus, problems such as crosstalk and large board size.

Usual implementation is also characterized by fixed adjustment of line interface conditions although telephone line conditions vary considerably with national standards and even with subscriber line installations. Under adverse conditions telecommunication equipment must match the subscriber line and termination impedances while suppressing return echoes in the two- to four-wire hybrid network. Compensating for line attenuation is just as critical for balancing the voice signals in the transmission and reception paths.

To improve voice quality, subscriber line boards have to be matched to different line conditions by means of interchangeable discrete components. This approach is very costly regarding line board design and manufacturing. Furthermore, the reliability of a board filled with parts, wires and connections will decrease rapidly.

The subscriber line board architecture proposed by Siemens Semiconductor is geared to eliminate many of these line board trouble spots.



General Line Board Structure and Functions

General Line Card Function

Component	**Function**
SLIC (Subscriber line interface circuit)	realisation of the BORSHT function B battery feed O overvoltage protection R ringing S supervision H hybrid T testing
analog network Z R,X B G	matching of input and line impedance frequency response correction hybrid balancing gain adjustment
CODEC/Filter	coding, A/D and D/A conversion according to A-law and μ-law, voice band limitation according to CCITT and LSSGR
PCM	time-slot assignment, PCM data rate

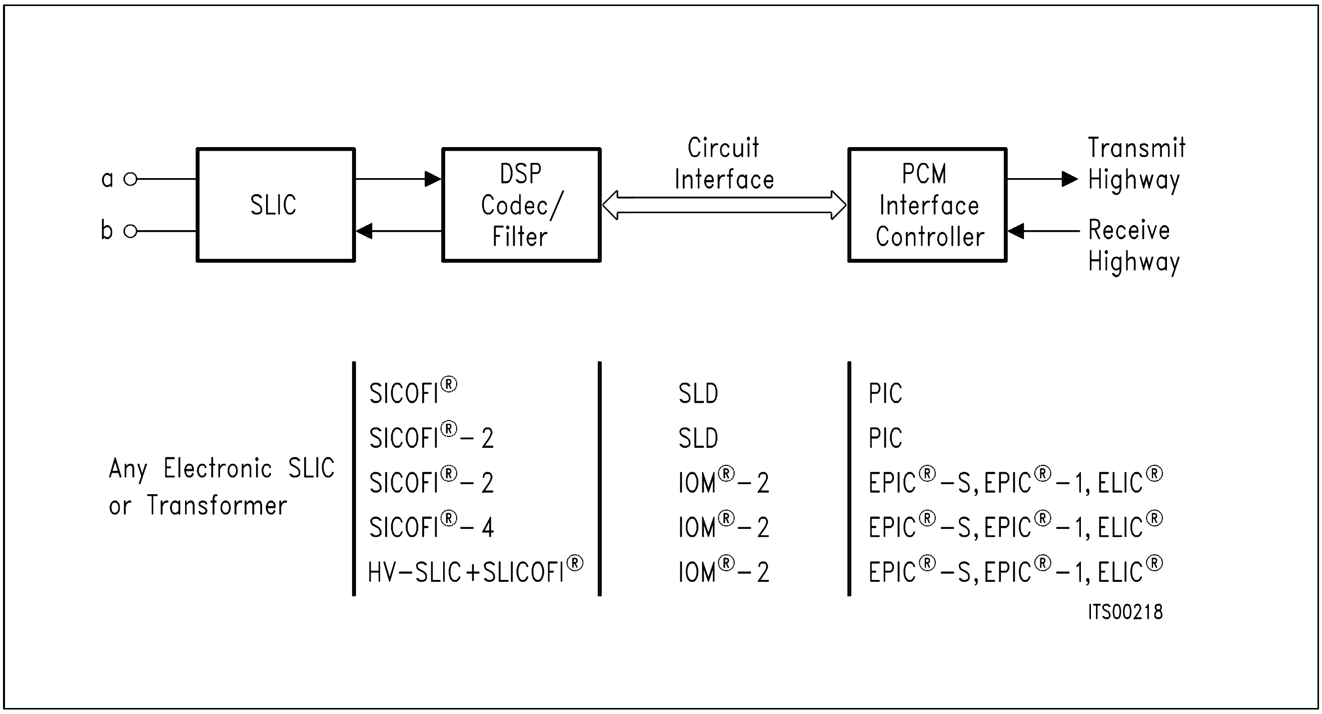
1.2 Optimized Line Board Architecture

The Siemens Semiconductor concept is characterized by a centralized PCM interface controller device providing the variable Time-Slot Assignment (TSA), the communication with up to 64 subscriber line devices such as signal processing codec/filter (SICOFI®) or ISDN devices via the SLD (Subscriber Line Data) or IOM®-2 (ISDN Oriented Modular) interface, and the interface with a microprocessor.

As a characteristic architectural feature, for test, monitring and control purposes, the device permits efficient switching of data streams between all these interfaces and, therefore, ensures transparency between the PCM channels and control or signaling data. This opens up attractive possibilities such as common-channel signaling and microprocessor access to PCM data.

The use of the signal processing codec/filter (SICOFI) avoids the analog network which has to be matched to different requirements by interchanging its discrete components. Based on Digital Signal Processing (DSP) methods the SICOFI allows the complete control of the line conditions by software.

The all-over flexibility of the unique device concept gives the user the capability for designing a standard line card which can be customized for each application under software control. The SLD/IOM-2 architecture leads to a highly modular line board configuration with low wiring, reduced board area and, depending only on the SLIC to be used, very few discrete elements.



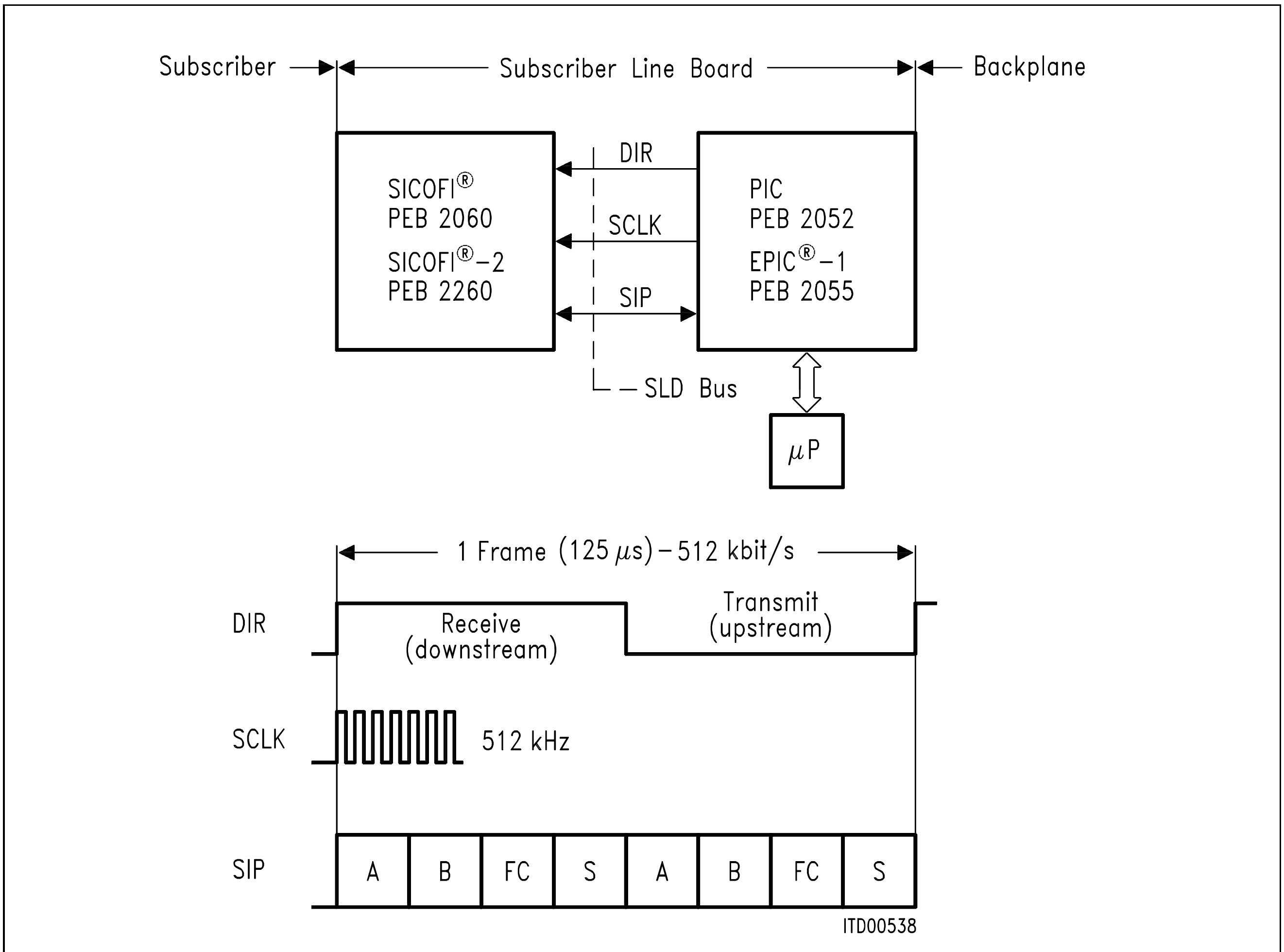
Siemens ICs for Analog Subscriber Lines

1.3 The SLD/IOM®-2 Interface

The SLD bus is used by the PBC/PIC to interface with the subscriber line devices. A **S**erial **I**nterface **P**ort (SIP) is used for the transfer of all digital voice and data, feature control and signaling information between the individual subscriber line devices, the PCM highways and the control backplane. The SLD approach provides a common interface for analog or digital per-line components. Through the PBC/PIC, which is the key device in the SLD architecture, the PCM data is transparently switched onto the PCM highways. The PBC will make analog and digital subscriber line boards plug-compatible in a line equipment rack.

There are three leads connecting each subscriber line device and the PBC/PIC: two common clock signals shared among all devices, and a unique bidirectional data lead for each of the eight SIP lines. The **Dir**ection signal (DIR) is an 8-kHz clock output from the PBC (master) that serves as a frame sync to the subscriber line devices (slave) as well as a transfer indicator. The data are transferred at a 512-kHz rate, clocked by the **S**ubscriber **Cl**oc**k** (SCLK). When DIR is high (first half of the SLD 125 µs frame), four bytes of digital data are transmitted on the SLD bus from the PBC/PIC to the slave (receive direction). During the second half of the frame when DIR is low, four bytes of data are transferred from the slave back to the PBC/PIC (transmit direction).

Channel A and B are 64-kbit/s channels reserved for voice or data to be routed to and from the PCM highways. In an application where one SICOFI is connected to a SIP, voice is received on channel A and transmitted on channel A and B. For a three-party conference, channel B is the third-party voice channel. If two SICOFIs are connected to one SIP, channel A is assigned to one and channel B to the other SICOFI. Conferencing is not possible in this configuration. With digital subscriber line devices the two bytes can be used to carry 64-kbit/s data channels. The third and sixth byte locations are used to transmit and receive control information for programming the slave devices. The last byte in each direction is reserved for signaling data.



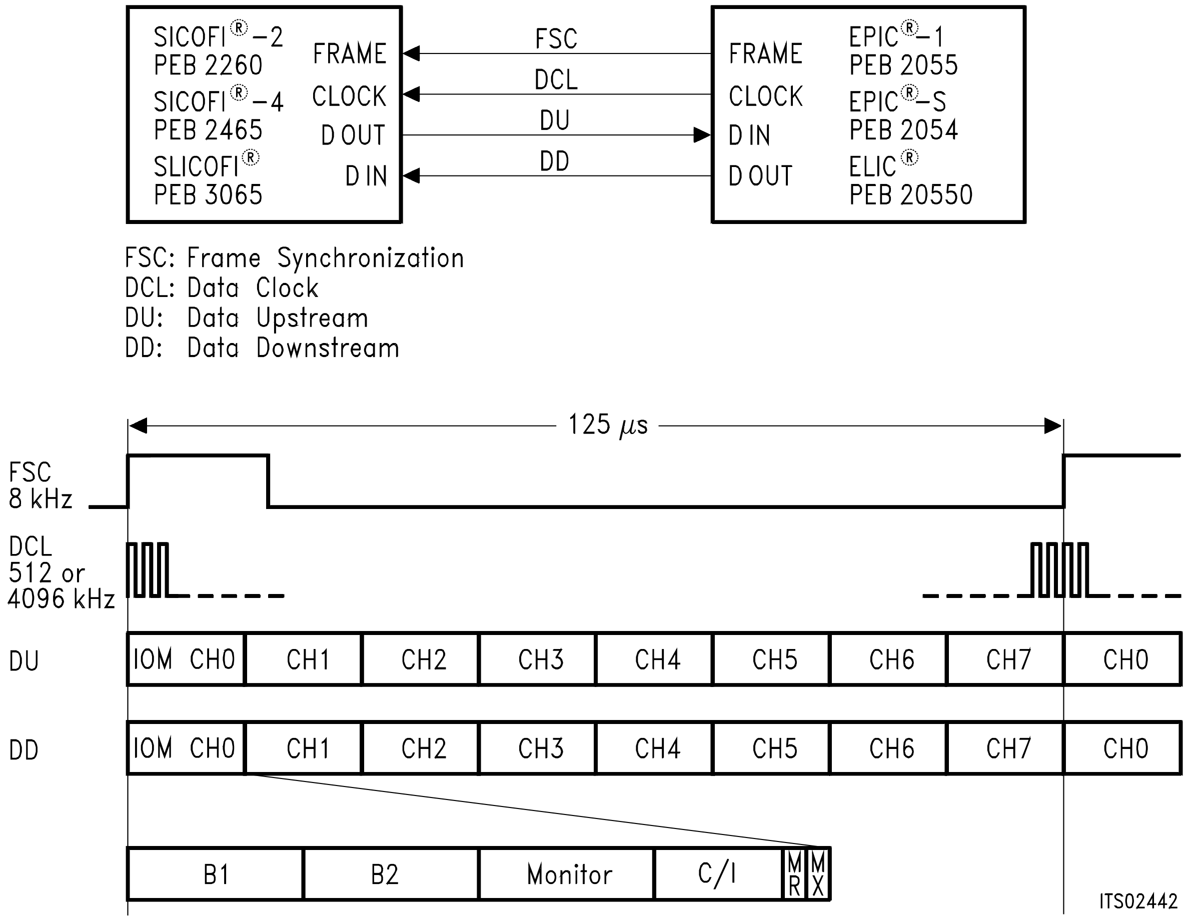
Frame Structure of the SLD Interface

Because of the unique requirements of ISDN systems, Siemens developed an interchip interface especially for these applications. As part of their joint definition of ISDN components, the "Group of Four" (ALCATEL, Siemens, Plessey and ITALTEL systems houses) adapted this Siemens Semiconductor interface and suggested some compatible additional features. The resulting IOM-2 interface has become the standard for interchip communication in ISDN terminals, terminal adaptors, network terminations, transmission repeaters and line cards for digital exchange systems.

The IOM-2 interface is a four wire interface with: a bit clock, a frame clock and one data line per direction. It has a flexible data clock. In this way, data transmission requirements are optimized for different applications.

On line cards, a 4096-kHz clock has been selected so that up to eight IOM channels and thus, eight ISDN or 16 analog subscribers can be multiplexed over a single IOM-2 bus. The channel structure of the IOM-2 interface is as follows:

- The first two octets constitute the two 64 kbit/s B channels.
- The third octet is the MONITOR channel. It is used for the exchange of data between devices using the IOM-2 MONITOR channel protocol.
- The fourth octet (control channel) contains
  - two bits for the 16 kbit/s D channel
  - a four-bit command/indication channel, in ISDN applications or
  - a six bit command/indication channel for analog subscriber applications
  - two bits MR and MX for supporting the MONITOR channel protocol.



Multiplexed Frame Structure of the IOM®-2 Interface

2 Device Overview

2.1 PCM Interface Controller (PBC/PIC/EPIC®)

The key device in the SLD architecture is the **P**eripheral **B**oard **C**ontroller (PBC) PEB 2050. Basically the PBC is a highly intelligent multiplexer/demultiplexer chip which performs the variable time-slot assignment for up to 16 PCM channels and handles the data streams for control and signaling. It constitutes the interface between the subscriber line devices such as codec filter or ISDN communication controller, the PCM lines, the central control unit and the optional onboard microprocessor.

Due to the importance of reliability in system design, the PBC provides a backplane interface with two fully redundant PCM highways. For the exchange of information between a central control unit and the PBC working as a "slave" in a point-to-multipoint configuration, the device supports a subset of the CCITT’s High Level Data Link Control (HDLC) communications protocol so that it can respond to certain HDLC frames without microprocessor intervention or software supervision.

The hardwired implementation of the physical level of the HDLC protocol (e.g. cyclic redundancy check) and of parts of this logical level (e.g. evaluation of HDLC commands and preparation of response packets) in the on-chip HDLC controller permits very high data rates of up to 4 Mbaud via the serial link to the central processor. By using a local standard microprocessor, such as the SAB 8051, it is possible to expand the range of the HDLC protocol to the full X.25 level, while still maintaining procedure handling, buffering and distribution of data packets hardwired in the PBC. Furthermore, the PBC is able, in conjunction with a microprocessor, to take over the "primary" function of a high speed HDLC communication link.

The PBC communicates with the subscriber line devices via a three-wire subscriber line data (SLD) bus based on a ping-pong type of protocol. The SLD bus ensures reduced line board wiring.

To cover a broad range of applications the PBC is adaptable to all standard commercial PCM systems (with 24, 32, 48, 64 channels per frame). Independently of the system clock used, the circuit computes all timing signals required for the standardized SLD bus, thus decoupling the subscriber line devices from the system clock. The PBC is an excellent example of the efficient realization of standard functions through the use of hardwired logic in order to increase realtime processing and speed without loss of flexibility.

A further device for interfacing subscriber line devices with PCM lines is the **P**CM **I**nterface **C**ontroller (PIC) PEB 2052. This CMOS device performs the **Time-Slot Assignment** (TSA) and the PCM interface functions. It is pin and software-compatible to the PBC PEB 2050, but leaves out the HDLC controller and the hardwired Last Look Logic.

The **E**xtended **P**CM **I**nterface **C**ontroller (EPIC) PEB 2055 is intended to be used as central PCM processor in the IOM architecture. The CMOS device can be programmed to operate at different data rates between 128 and 8192 kbit/s. The system interface consists of up to four duplex ports with a tristate indication signal for each output line. The configurable interface can be selected to incorporate either four duplex (IOM) or eight bidirectional I/O ports (SLD).

The EPIC can therefore be programmed to communicate either with SLD or with IOM (ISDN Oriented Modular) and IOM®-2 compatible devices. In both cases the device handles the layer-1 functions of buffering the C/I and MONITOR channels for IOM-compatible devices and the feature control and signaling channels for SLD compatible devices. The EPIC can handle up to 32 ISDN subscribers with their 2B + D channel structure or 64 analog subscribers in IOM configuration or up to 16 subscribers in SLD configuration. Since its interfaces can operate at different data rates, the EPIC is an ideal device for data rate adaptation.

Moreover, the EPIC is one of the fundamental building blocks for networks with either central, decentral or mixed signaling and packet data handling architectures.

The EPIC-2 PEB 2056 is a smaller version of the EPIC. The functions that are performed remain essentially the same but the EPIC-2 PEB 2056 has been optimized for time-slot assignment and switching functions on line cards with up to 8 ISDN or 16 analog subscriber lines.

Siemens Semiconductor therefore offers the optimal solution of PCM Interface Controller for every application.

– **PBC PEB 2050:** for up to eight ISDN and 16 analog subscribers. Especially suitable for powerful PABX.
– **PIC PEB 2052:** for up to eight ISDN and 16 analog subscribers. Ideal for price sensitive systems, e.g. small PABX and public exchanges (CO).
– **EPIC PEB 2055:** for up to 32 ISDN and 64 analog subscribers. Suitable as the central PCM processor in IOM architectures.
– **EPIC-2 PEB 2056:** for up to 8 ISDN or 16 analog subscribers in IOM architectures.

2.2 Signal Processing Codec/Filter (SICOFI®/SICOFI®-2)

The Codec/Filter used in the advantageous analog line board architecture is the programmable **Si**gnal Processing **Co**dec **Fi**lter (SICOFI) PEB 2060, fabricated in advanced CMOS technology. Based on Digital Signal Processing (DSP) methods, in addition to the standard functions of PCM coding and voice-band limitation that any codec filter features, the SICOFI provides a variety of user-programmable filters for impedance matching, 2/4-wire hybrid balancing, analog and digital gain adjustment as well as frequency response correction.

A sophisticated level of performance can therefore be achieved under complete software control. The use of external components or trimming procedures is completely avoided.

For impedance adjustments, the related filter implements a feedback loop to modify the SLIC's termination impedance. It can handle complex impedances, resulting in optimized return loss for almost all subscriber line conditions. In a similar manner, the hybrid balance filter can be programmed for optimal balance between the transmit and receive side and for minimum echoes.

For accurate adjustment of the gain in receive and transmit directions, four independently programmable filters can vary the level of the analog voice signal in a range of ± 22 dB.

Similar to the level control, the SICOFI contains digital filters in receive and transmit directions, which allow modification of the frequency response characteristics. Further features attractive for the realization of flexible exchange systems are selectable A/µ law coding, three-party conference support, supply voltage supervision, hardware and software reset, power-down mode and on-chip reference voltage. Different loopback modes enable both the line board and the total system to be tested during operation. The SICOFI can hook up directly to virtually any commercial SLIC, because of its flexible signaling interface consisting of ten ports. Three are dedicated to the status of voice transmissions and three to receptions. The remaining four can be programmed individually as either transmit or receive ports.

Due to the fact that the SICOFI needs extended control information, a message-oriented protocol is used for byte transfer via the SLD bus. Two bits in each control byte are used to define three different classes of commands, which contain information about the configuration of the SICOFI, the coefficient exchange and the number of subsequently transmitted data bytes. Per frame and direction, one control byte is transferred between the SICOFI and the PBC. With the appropriate commands, data can be written into or read back from the SICOFI. Selection of one of the two SICOFIs connected to one SLD port is accomplished by an address bit in the feature control byte. For programming the device the information usually is transferred via the HDLC link to the PBC, but all programming can also be done by means of an on-board microprocessor.

There are numerous good reasons why, the world over, major attention is given to digital signal processing methods. Compared to analog filtering, digital processing does not need precision elements, allows much higher accuracy along with precisely predictable transmission behavior including noise. It makes the device less sensitive to parameter fluctuations such as drift with temperature or aging and, moreover, it provides excellent power supply rejection, better testability and crosstalk behavior of the circuit.

In addition, the DSP technique allows a better and easier shrinking of the device and the implementation of codec/filter functions for two and more subscribers on one chip, which is not economic or completely impossible with switched capacitor methods. The next development stage has produced a Dual Channel Codec Filter (SICOFI-2) PEB 2260 that performs the functions of the SICOFI-1 PEB 2060 for two subscribers in one chip.

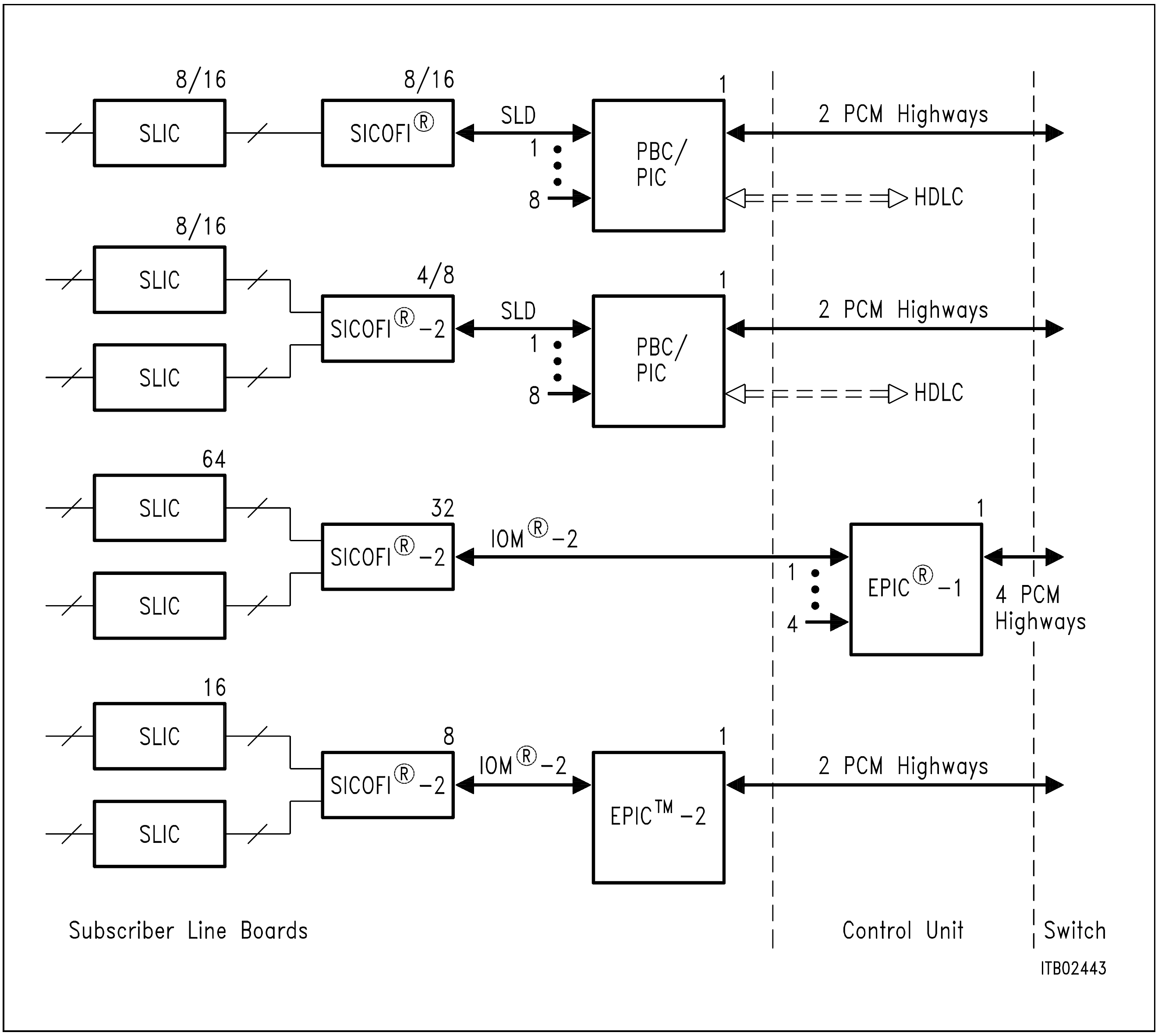
The sharing of the same digital signal processor part allows a reduced die size per line and leads to reduced line-card costs.

Moreover the CMOS device can be programmed to communicate either with SLD (PBC/PIC) or with IOM-2 (EPIC) compatible PCM interface controller.

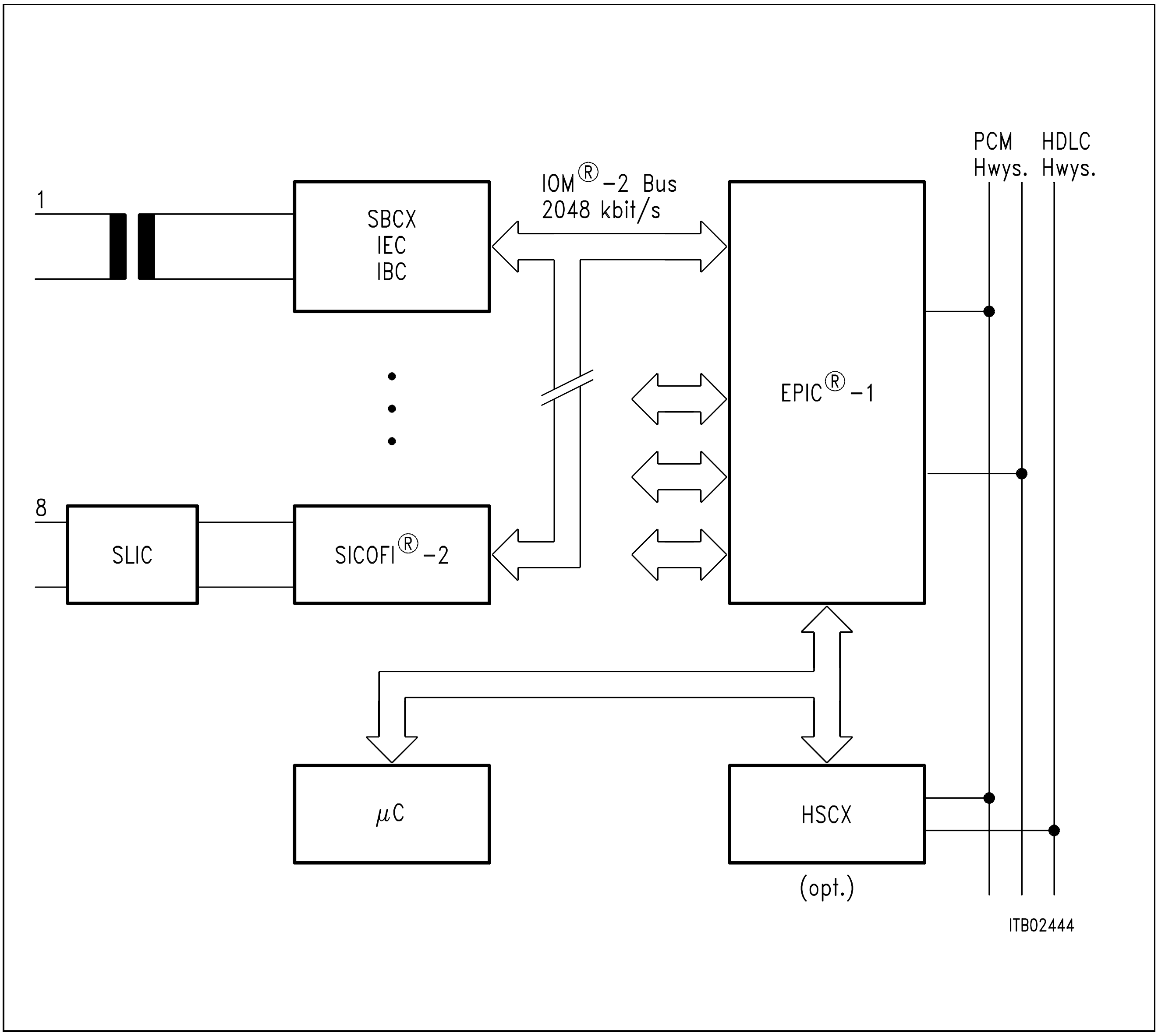
As shown with the SICOFI the DSP approach, in a cost-saving and programmable manner, allows the realization of new functions which would be very expensive or impractical in the analog domain.

Optimized Board Controller Concept

Circuit Interface	**Controller**	**Max. Subscriber**	**Highways**
SLD	PEB 2050 (PCB) with HDLC controller	16 analog or 8 ISDN	2 PCM (4 Mbit/s) 1 HDLC
SLD	PEB 2052 (PIC) low cost PBC for analog line cards with SICOFI	16 analog or 8 ISDN	2 PCM (4 Mbit/s)
IOM-2/ (SLD)	PEB 2055 (EPIC-1) key device for mixed ISDN/Analog systems	64 analog or 32 ISDN	4 PCM (8 Mbit/s)
IOM-2	PEB 2056 (EPIC-2) low cost EPIC	16 analog or 8 ISDN	2 PCM (4 Mbit/s)



Optimal Solutions for Every Application



Mixed Use of ISDN and Analog Subscribers with EPIC®

3 Advantages of Siemens Semiconductor Analog Line Card Concept

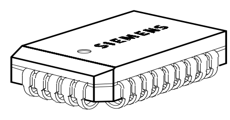
- Advanced Signal Processing Codec Filter SICOFI family based on DSP technique.
- Matching to different line conditions under complete software control (global line-card solution).
- Modular architecture (IOM-2/SLD compatible).
- Reduced line card wiring, per line structure avoids cross wiring.
- Optimized board controller family.
- Cost optimized design/high volume production.
- Effective application support tools (hardware/software).

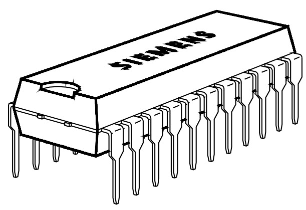
SIEMENS

Signal Processing Codec Filter (SICOFI®) — PEB 2060

Features — **CMOS IC**

- Single chip codec and filter
- Band limitation according to all CCITT and AT & T recommendations
- Digital Signal Processing techniques
- Digital voice transmission
  – PCM encoded (A-law or μ-law)
  – linear (16 bit 2's complement)
- Programmable digital filters for
  – impedance matching
  – transhybrid balancing
  – gain
  – frequency response correction
- Configurable three pin serial interface
  – 512-kHz-SLD-Bus (e.g. to PEB 2050/52)
  – burst mode with bit rates up to 4 Mbit/s
- Programmable signaling interface to peripherals (e.g. SLIC)
- High performance A/D and D/A conversion
- Programmable analog gain
- Advanced test capabilities
  – three digital loop back modes
  – two analog loop back modes
  – on chip tone generation
- No trimming or adjustments
- No external components
- Variable clock selection
- Signaling expansion possible
- Prepared for three-party conferencing
- Advanced low power 2μCMOS technology
- Power supply + / – 5 V
- Meets or exceeds CCITT and LSSGR recommendations


P-LCC-28-R


P-DIP-22

Type	Version	Ordering Code	Package
PEB 2060-N	V 4.4	Q67100-H8393	P-LCC-28-R (SMD)
PEB 2060-P	V 4.4	Q67100-Z170	P-DIP-22

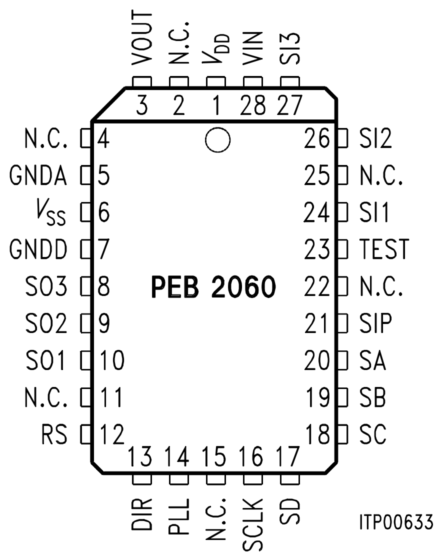
General Description

The Signal Processing Codec Filter (SICOFI) PEB 2060 is a fully integrated PCM codec (coder/decoder) and transmit/receive filter fabricated in advanced CMOS technology for applications in digital telecommunication systems. Based on a digital filter concept, the PEB 2060 provides improved transmission performance and high flexibility. The digital signal processing approach supports software controlled adjustment of the analog behavior, including attractive features such as programmable transhybrid balancing, impedance matching, gain and frequency response correction.

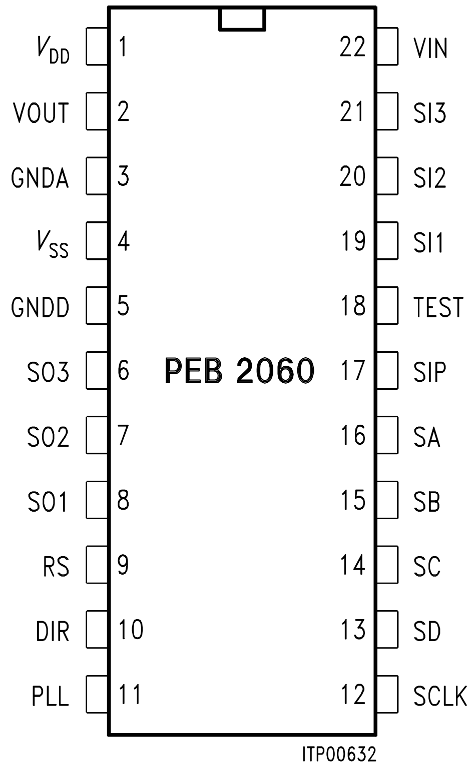
Pin Configuration

(top view)

P-LCC-28-R



P-DIP-22

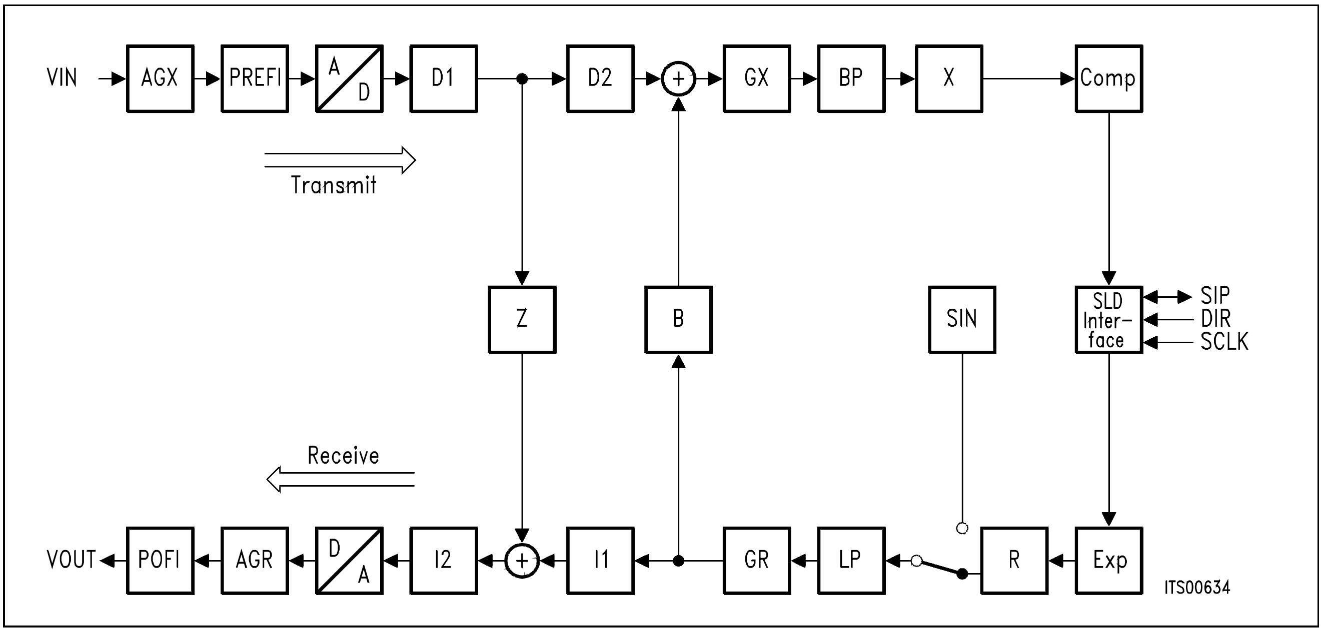


Pin Definitions and Functions

Pin No.		Symbol	Input (I) Output (O)	Function
P-LCC-28-R	P-DIP-22			
1	1	V_{DD}	I	+ 5 V power supply
6	4	V_{SS}	I	– 5 V power supply
5	3	GNDA	I	Ground analog, not internally connected to GNDD All analog signals are referred to this pin
7	5	GNDD	I	Ground digital, not internally connected to GNDA All digital signals are referred to this pin
28	22	VIN	I	Analog voice input to transmit path
3	2	VOUT	O	Analog voice output of the received digital voice
16	12	SCLK	I	Slave clock
13	10	DIR	I	Frame synchronisation signal (direction signal)
21	17	SIP	I/O	Serial interface port, bidirectional serial data port
12	9	RS		Reset input, RS forces the SICOFI to power down mode and initializes the configuration registers
23	18	TEST	I	Test input, normally connected to GNDD
14	11	PLL	I	Clock selection (see Appendix A)
24	19	SI1	I	Signaling inputs. Data present at SI is sampled and transmitted via the serial interface
26	20	SI2	I	
27	21	SI3	I	
10	8	SO1	O	Signaling outputs. Data received via the serial interface is latched and fed to these outputs
9	7	SO2	O	
8	6	SO3	O	
20	16	SA	I/O	Programmable I/O signaling pins. Each of these pins may be declared input individually with adequate SICOFI status settings. If 2 SICOFIs are connected to 1 serial interface, pin SA (high/low) assigns voice, control and signaling bytes
19	15	SB	I/O	
18	14	SC	I/O	
17	13	SD	I/O	

SICOFI® Principles

The SICOFI codec filter solution is a highly digital approach utilizing the advantages of digital signal processing such as excellent performance, high flexibility, easy testing, no sensitivity to fabrication and temperature variations, no problems with crosstalk and power supply rejection.



SICOFI® Signal Flow Graph

Transmit Direction

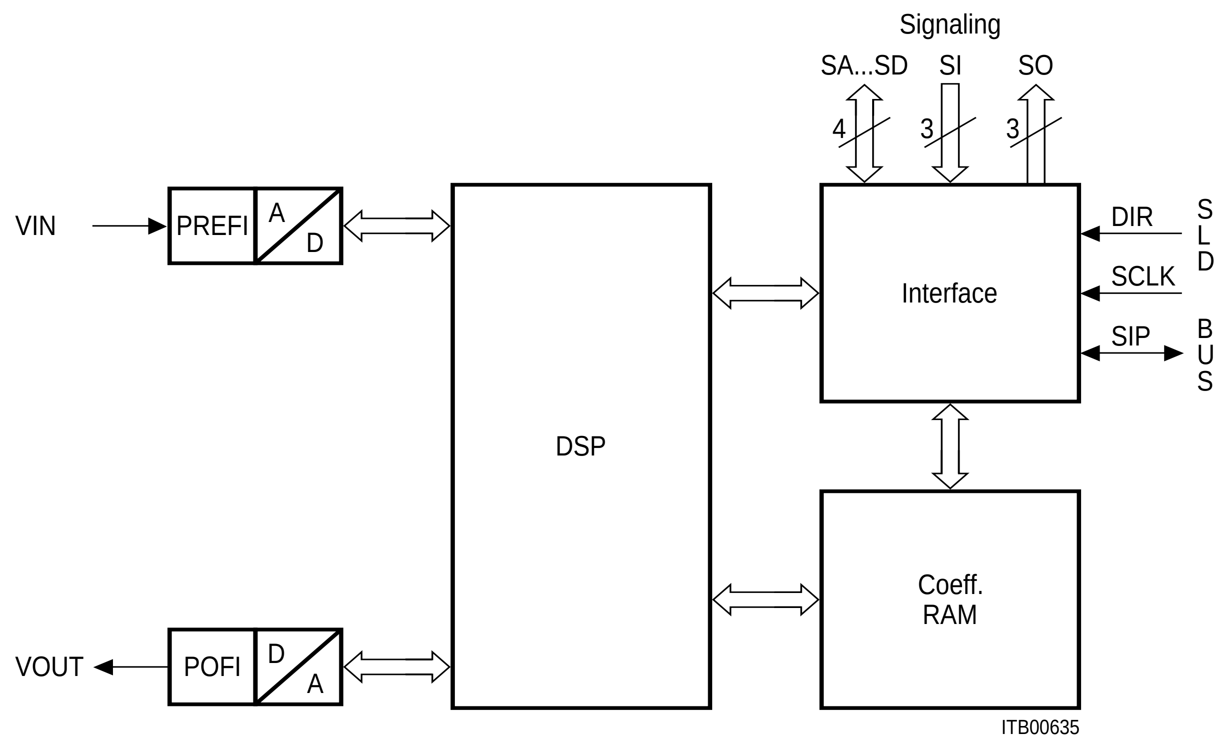
The analog input signal is A/D converted, digitally filtered and transmitted either PCM-encoded or linear. Antialiasing is done with a 2nd order Sallen-Key prefilter (PREFI). The A/D Converter (ADC) is a modified slopeadaptive interpolative sigmadelta modulator with a sampling rate of 128 kHz. Digital downsampling to 8 kHz is done by subsequent decimation filters D1 and D2 together with the PCM bandpass filter (BP).

Receive Direction

The digital input signal is received PCM-encoded or linear, digitally filtered and D/A converted to generate the analog output signal. Digital interpolation up to 128 kHz is done by the PCM lowpass filter (LP) and the interpolation filters I1 and I2. The D/A Converter (DAC) output is fed to the 2nd order Sallen-Key postfilter (POFI).

Programmable Functions

The high flexibility of the SICOFI is based on a variety of user programmable filters, which are analog gain adjustment AGR and AGX, digital gain adjustment GR and GX, frequency response adjustment R and X, impedance matching filter Z and the transhybrid balancing filter B.



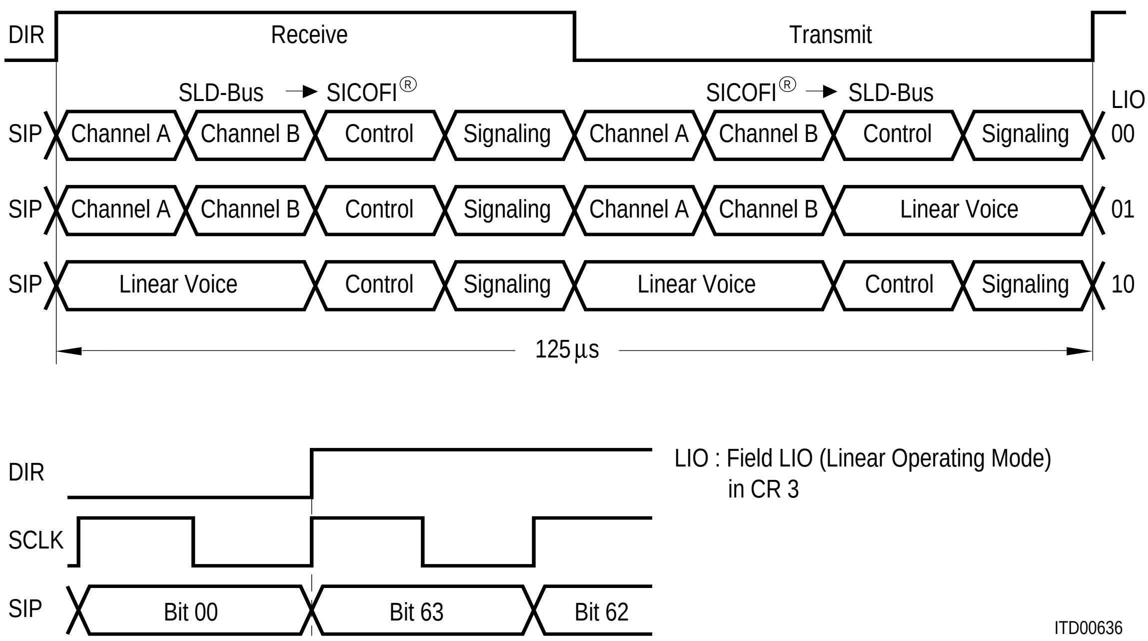
SICOFI® Block Diagram

The SICOFI bridges the gap between analog and digital voice signal transmission in modern telecommunication systems. High performance oversampling Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) provide the conversion accuracy required. An analog antialiasing prefilter (PREFI) and smoothing postfilter (POFI) is included. The dedicated on chip Digital Signal Processor (DSP) handles all the algorithms necessary, e.g. PCM bandpass filtering, sample rate conversion and PCM companding. The three pin serial SLD-Bus interface handles digital voice transmission and SICOFI feature control. Specific filter programming is done by downloading coefficients to the coefficient ram (CRAM).
The ten pin parallel Signaling Interface provides for a powerful per line SLIC control.

Serial Line Data Interface (SLD Interface)

The exchange of data on the SLD-Bus is based on a bidirectional, bitserial interface consisting of three pins: SIP, DIR and SCLK.
Data is written or read out on the Serial Interface Port SIP under control of the frame synchronization signal DIR with a period of 125 µs*). The interface clock frequency supplied at the Slave CLock pin SCLK is 512 kHz*). The rate of the serial data stream on the SIP pin is 512 kbit/s, that is 64 bits per each 8 kHz frame*).

Starting with the rising edge of DIR, four bytes of information are transferred on the SLD-Bus to the SICOFI, followed by four bytes from the SICOFI to the SLD-Bus. Bit 7 (MSB) is the first bit transferred and bit 0 (LSB) is the last one of each byte.



Byte Sequence and Timing at Serial Interface Port SIP

*) for applications with other clock rates see Appendix A

Programming

A message-orientated byte transfer is used, due to the fact that the SICOFI needs extended control information. One control byte per frame and direction is transferred. With the appropriate received commands, data can be written to the SICOFI or read from the SICOFI onto the SLD-bus.

Data transfer to the SICOFI starts with a write command, followed by up to 8 bytes of data. The SICOFI responds to a read command with the requested information, starting at the next transmission period. If no status modification or data exchange is required a NOP byte is transferred (**see Programming Procedure**).

Control Bytes

The 8-bit control bytes consist of either commands, status information or data. There are three different classes of SICOFI commands:

NOP **NO OPERATION:**
no status modification or data exchange

SOP **STATUS OPERATION:**
SICOFI status setting/monitoring

COP **COEFFICIENT OPERATION:**
filter coefficient setting/monitoring

The class of command is selected by Bit 2 and 3 of the control byte as shown below. Due to the extended SICOFI feature control facilities, SOP- and COP-commands contain additional information.

BIT	7	6	5	4	3	2	1	0
NOP	1	1	1	1	1	1	1	1
SOP					0	1		
COP					X	0		

X … don't care

NOP Command

If no status modification of the SICOFI or control data exchange is required, a No Operation Byte NOP is transferred.

BIT	7	6	5	4	3	2	1	0
	1	1	1	1	1	1	1	1

SOP Command

To modify or evaluate the SICOFI status, the contents of up to four configuration registers CR1, CR2, CR3 and CR4 may be transferred to or from the SICOFI. This is done by a SOP-Command (Status Operation Command).

BIT	7	6	5	4	3	2	1	0
	AD	R/W	PU	TR	0	1	LSEL	

AD	Address Information	AD = 0 AD = 1	A-SICOFI addressed B-SICOFI addressed This bit is evaluated if two SICOFIs are connected to one SLD-port. A SICOFI is accessed, if AD is consistent with the level at pin SA (**see Signaling Byte, Programming Procedure**).
R/W	Read/Write Information	R/W = 0 R/W = 1	Write to SICOFI Read from SICOFI Enables reading from the SICOFI or writing information to the SICOFI.
PU	Power Up/ Power Down (**see also CR3**)	PU = 1 PU = 0	sets the SICOFI to power-up mode (operating) resets the SICOFI to power-down (standby mode)
TR	Three Party Conference	TR = 1	The received voice bytes of channel A and channel B are added (A + B). The result is filtered, D/A converted and transferred to analog output VOUT (**see also CR3**).

LSEL Length Select Information, identifies the number of subsequent data bytes (**see also Programming Procedure**)

LSEL = 0 0	no byte following
LSEL = 1 1	CR1 is following
LSEL = 1 0	CR2 and CR1 are following
LSEL = 0 1	CR4, CR3, CR2 and CR1 are following in this case the PU and TR bits are not overwritten.

CR1 Configuration Register 1

This configuration register is used for enabling/disabling the programmable digital filters (DB ... RG) and for accessing testmodes (TM1).

BIT	7	6	5	4	3	2	1	0
	DB	RZ	RX	RR	RG		TM1	

DB	Disable B-Filter	DB = 0 DB = 1	B-Filter enabled B-Filter disabled
RZ	Restore Z-Filter	RZ = 0 RZ = 1	Z-Filter disabled Z-Filter enabled
RX	Restore X-Filter	RX = 0 RX = 1	X-Filter disabled X-Filter enabled
RR	Restore R-Filter	RR = 0 RR = 1	R-Filter disabled R-Filter enabled
RG	Restore GX-GR-Filter	RG = 0 RG = 1	GX-GR-Filter disabled GX-GR-Filter enabled

TM1	**TEST MODES**
0 0 0	No test mode
0 0 1	Analog loop back via Z-filter (H (Z) = 1)[1)]
0 1 0	Disable highpass filter (part of bandpass BP)
0 1 1	Cut off receive path
1 0 0	Initialize data ram with 0x0000
1 1 0	Digital loop back via B-filter (H (B) = 1)[2)]
1 1 1	Digital loop back via PCM-register[3)]

Other codes are reserved for future use.

1) Output of the interpolation filter I1 is set to 0.
Value of transfer function of the Z-filter is 1 (not programmable).

2) Output of the low pass decimation filter D2 is set to 0.
Value of transfer function of the B-filter is 1 (not programmable).

3) PCM in = PCM out. This testmode is also available in standby mode.

CR2 Configuration Register 2

BIT	7	6	5	4	3	2	1	0
	D	C	B	A	EL	AM	µ/A	PCS

The first four bits D ... A in this register, program the four bidirectional signaling pins SD ... SA. With two SICOFIs on one SLD-port only pin SD can be used, pin SA is always input in this case and indicates the address of the SICOFI.
SA = 0 : A-SICOFI, SA = 1 : B-SICOFI (**see also bit AD in SOP-command**).

D	Signaling Pin SD	D = 0 D = 1	SD is output SD is input
C	Signaling Pin SC	C = 0 C = 1	SC is output SC is input
B	Signaling Pin SB	B = 0 B = 1	SB is output SB is input
A	Signaling Pin SA	A = 0 A = 1	SA is output SA is input
EL	Signaling Expansion Logic	EL = 0 EL = 1	No expansion logic Expansion logic provided Signaling expansion logic is only possible with one SICOFI on port (**see also Signaling Byte**)
AM	Address Mode	AM = 0 AM = 1	Two SICOFIs on SLD port One SICOFI on SLD port The SICOFI access to the SLD-Bus voice channel is controlled by AM and TR.

		Receive (SLD-Bus ⇒ SICOFI)		**Transmit (SICOFI ⇒ SLD-Bus)**	
AM	**TR**	**SICOFI A**	**SICOFI B**	**SICOFI A**	**SICOFI B**
0	0	channel A	channel B	channel A	channel B
0	1	channel B	channel A	channel B	channel A
1	0	channel A	------	channel A, B[1)]	------
1	1	channel A + B[2)]	------	channel A, B[1)]	------

µ/A	PCM-law	µ/A = 0 µ/A = 1	A-law µ-law (µ255 PCM)
PCS	B-Filter Coefficients	PCS = 0 PCS = 1	Programmed coefficients Fixed coefficients

1) The SICOFI transmits the same byte in channel A and B.
2) Three Party Conference.

CR3 Configuration Register 3

BIT	7	6	5	4	3	2	1	0
	AGX		AGR		PU	TR	LIO	

AGX	Analog Gain Control Transmit-Path	
	AGX = 0 0	0 dB
	AGX = 0 1	6.03 dB amplification
	AGX = 1 0	12.06 dB amplification
	AGX = 1 1	14 dB amplification

AGR	Analog Gain Control Receive-Path	
	AGR = 0 0	0 dB
	AGR = 0 1	6.03 dB attenuation
	AGR = 1 0	12.06 dB attenuation
	AGR = 1 1	14 dB attenuation

PU	Power Up / Power Down[1]	
	PU = 0	Power Down (standby)
	PU = 1	Power Up (operating)

TR Three Party Conference/Reverse Operating Mode (**see CR2**)[1]

LIO	Linear Operating Mode (**see Serial Interface**)	
	LIO = 0 0	PCM mode
	LIO = 0 1	Linear mode 1[2]
	LIO = 1 0	Linear mode 2

(Change of linear mode becomes valid in the next DIR-cycle).

[1] The bits PU and TR may also be overwritten by a SOP Command with LSEL ≠ 0 1 (PU and TR are part of the SOP Command).
With LSEL = 0 1, the bits PU and TR in the SOP Command are ignored.

[2] Subsequent to a SOP/COP-read Command the control and signaling information is transmitted instead of linear voice.

CR4 Configuration Register 4

BIT	7	6	5	4	3	2	1	0
		TM3		0	0		TM4	

TM3	TEST MODES
0 0 0	No test mode
0 0 1	Additional + 6 dB digital gain in transmit direction (GX)
0 1 1	Additional + 12 dB digital gain in transmit direction (GX)
1 0 0	Enable on chip tone generation[1)]
1 1 0	Far analog loop back[2)]

TM4	TEST MODES
0 0 0	No test mode
1 0 0	Digital loop back via analog port (VIN = VOUT)

Other codes are reserved for future use.

1) With the R-filter disabled a 2 kHz, 0 dBm0 sinusoidal signal is fed to the input of the receive Lowpass Filter LP (other frequencies see Appendix B).
2) The output of the X-filter is fed to the input of the R-filter (8 kHz, 16 bit linear).

COP Command

BIT	7	6	5	4	3	2	1	0
	AD	R/W	CODE					

With a COP Command coefficients for the programmable filters can be written to the SICOFI coefficient ram or transmitted on the SLD-bus for verification.

AD Address Information
AD = 0 A-SICOFI addressed
AD = 1 B-SICOFI addressed
This bit is evaluated with two SICOFIs on one SLD-port only.
With two SICOFIs on port, a SICOFI is identified, if AD is consistent with the level at pin SA (**see Signaling Byte, Programming Procedure**).

R/W Read/Write Information
R/W = 0 Write to SICOFI
R/W = 1 Read from SICOFI
This bit indicates whether filter coefficients are written to the SICOFI or read from the SICOFI.

CODE		
0 0 0 0 1 1	B-Filter coefficients part 1	(followed by 8 bytes of data)
0 0 1 0 1 1	B-Filter coefficients part 2	(followed by 8 bytes of data)
0 1 0 0 1 1	Z-Filter coefficients	(followed by 8 bytes of data)
0 1 1 0 0 0	B-Filter delay coefficients	(followed by 4 bytes of data)
1 0 0 0 1 1	X-Filter coefficients	(followed by 8 bytes of data)
1 0 1 0 1 1	R-Filter coefficients	(followed by 8 bytes of data)
1 1 0 0 0 0	GX- and GR-Filter coefficients*)	(followed by 4 bytes of data)

Other codes are reserved for future use.

*) In the range – 8 dB to 8 dB gain adjustment is possible in steps ≤ 0.25 dB

Signaling Byte

The signaling interface of the SICOFI consists of 10 pins.
3 transmit signaling inputs: SI1, SI2 and SI3
3 receive signaling outputs: SO1, SO2 and SO3
4 bidirectional programmable signaling pins: SA, SB, SC and SD

Data present at SI1 … SI3 and possibly at some or all of SA … SD (if programmed as inputs) are sampled and transferred serially on SIP onto the SLD-bus. Data received serially on SIP from the SLD-Bus are latched and fed to SO1 … SO3 and possibly to some of SA … SD if programmed as output.

The signaling field format is generally:

in receive direction:

BIT	7	6	5	4	3	2	1	0
	SO1	SO2	SO3	SD	SC	SB	SA	SEL

in transmit direction:

BIT	7	6	5	4	3	2	1	0
	SI1	SI2	SI3	SD	SC	SB	SA	SEL

where SEL is the signaling expansion bit if EL = 1 in CR2.

For the different cases possible, the signaling byte format at SIP is

	Receive Signaling Byte								**Transmit Signaling Byte**							
Bit Case	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1	SO1	SO2	SO3	X	X	X	X	X	SI1	SI2	SI3	SD	SC	SB	SA	0
2	SO1	SO2	SO3	X	X	X	X	X	SI1	SI2	SI3	SD	SC	SB	SA	Z
3	SO1	SO2	SO3	SD	SC	SB	SA	X	SI1	SI2	SI3	0	0	0	0	0
4	SO1	SO2	SO3	SD	SC	SB	SA	X	SI1	SI2	SI3	Z	Z	Z	Z	Z
5 A-SIC	SO1	SO2	SO3	X	X	X	X	X	SI1	SI2	SI3	SD	Z	Z	Z	Z
B-SIC	X	X	X	X	SO1	SO2	SO3	X	Z	Z	Z	Z	SI1	SI2	SI3	SD
6 A-SIC	SO1	SO2	SO3	SD	X	X	X	X	SI1	SI2	SI3	0	Z	Z	Z	Z
B-SIC	X	X	X	X	SO1	SO2	SO3	SD	Z	Z	Z	Z	SI1	SI2	SI3	0

Z … high impedance, X … don't care

Cases

1 One SICOFI is connected to one SLD port, EL = 0 (no signaling expansion logic provided); SA … SD are programmed as transmit signaling inputs.

2 One SICOFI connected to one SLD port, EL = 1 (signaling expansion logic provided); SA … SD are programmed as transmit signaling inputs.

3 One SICOFI is connected to one SLD port; EL = 0 (no signaling expansion logic provided); SA … SD are programmed as receive signaling outputs.

4 One SICOFI is connected to one SLD port; EL = 1 (signaling expansion logic provided); SA … SD are programmed as receive signaling outputs.

If a signaling expansion logic is provided (see case 2 and 4), the signaling bits SA … SD which are programmed as signaling inputs or outputs can be used as additional expansion bits in receive or transmit direction, respectively. As far as SICOFI is concerned, SIP is in a high-impedance (Z) state or "don't care" (Y) state while these bits are transferred.

5 Two SICOFIs are connected to one SLD port; SD is programmed as transmit signaling input.

6 Two SICOFIs are connected to one SLD port; SD is programmed as receive signaling output.

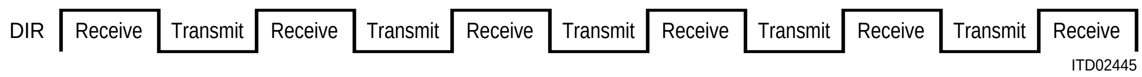
If two SICOFIs are connected to one SLD port, no signaling expansion logic is possible. SA is programmed as input automatically, and defines the addressed SICOFI:

SA = 0 : A-SICOFI
SA = 1 : B-SICOFI.

SB and SC are not usable with two SICOFIs on one SLD port.

Programming Procedure

The following table shows some control byte sequences. If the SICOFI has to be configured completely during initialization, up to 60 bytes will be transferred.



DIR

No Operation

	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP

SOP Write

LSEL = 00	SOP	NOP								
LSEL = 11	SOP	NOP	CR1	NOP						
LSEL = 10	SOP	NOP	CR2	NOP	CR1	NOP				
LSEL = 01	SOP	NOP	CR4	NOP	CR3	NOP	CR2	NOP	CR1	NOP

SOP Read

LSEL = 00	SOP	NOP								
LSEL = 11	SOP	CR1								
LSEL = 10	SOP	CR2	X	CR1						
LSEL = 01	SOP	CR4	X	CR3	X	CR2	X	CR1		

COP Write

4 Bytes	COP	NOP	DB4	NOP	DB3	NOP	DB2	NOP	DB1	NOP
8 Bytes	COP	NOP	DB8	NOP	DB7			NOP	DB1	NOP

COP Read

4 Bytes	COP	DB4	X	DB3		DB1	X	CR2	X	CR1
8 Bytes	COP	DB8	X	DB7		DB1	X	CR2	X	CR1

X … don't care

DB1, DB2 … DB8 … coefficient Data Byte 1 … 8

Operating Modes

Basic Setting

Upon initial application of V_{DD} or reseting pin RS to "1" while operating, the SICOFI enters a basic setting mode. Basic setting means, that the SICOFI configuration registers CR1 … CR4 are initialized. All CR1 bits are set to "0" (all programmable filters are disabled except the B-Filter where fixed coefficients are used, no test mode); CR2 is set to "1" (SA … SD are inputs, signaling expansion logic is provided, one SICOFI on SLD-port, μ-law chosen and fixed B-Filter coefficients used). All CR3 and CR4 bits are reset to "0" (no additional amplification or attenuation, no linear mode, power down, no test mode). Receive signaling registers are cleared. SIP is in high-impedance state, the analog output VOUT and the receive signaling outputs SO1 … SO3 are forced to ground.
The serial interface is active to receive commands starting with the next 8-kHz SLD-Bus frame. The serial interface port SIP remains in high-impedance state until CR2 has been defined.
If two SICOFIs are connected to one SLD port, both SICOFI's get the same SOP and CR2 information during initialization. The subsequent CR1 byte is assigned to the addressed SICOFI only. If the two SICOFI's need different CR2 information, the SOP-CR2 sequence has to be provided once again (each SICOFI knows its address now).

If any voltage is applied to any input before initial application of V_{DD}, the SICOFI may not enter the Basic Setting Mode. In this case it is necessary either to reset the SICOFI via the RS Pin or to initialize the configuration registers CR1, CR2, CR3, CR4.

Standby Mode

Upon reception of a SOP command to load CR2 from the basic setting, the SICOFI enters the standby mode (basic setting replaced by individual CR2). Being in the operating mode, the SICOFI is reset to standby mode with a Power-Up bit PU = 0 (in CR3 or in the SOP-command directly). The serial interface is active to receive and transmit new commands and data.

Operating Mode

From the standby mode, the operating mode is entered upon recognition of a Power-Up bit PU = 1 (in CR3 or in the SOP-command directly).

Transmission Characteristics

The target figures in this specification are based on the subscriber-line board requirements. The proper adjustment of the programmable filters (transhybrid balancing: B; impedance matching: Z; frequency-response correction: X, R) needs a complete knowledge of the SICOFIs analog environment. Unless otherwise stated, the transmission characteristics are guaranteed within the test condition below.

T_A = 0 °C to 70 °C; V_{DD} = 5 V ± 5 %; V_{SS} = – 5 V ± 5 %; GNDA = GNDD = 0 V
R_L > 10 kΩ; C_L < 50 pF; H(Z) = H(B) = 0; H(X) = H(R) = 1;
GX = 0 to 8 dB; GR = 0 to – 8 dB; AGX = 0, 6.03, 12.06, 14 dB;
AGR = 0, – 6.03, – 12.06, – 14 dB;
f = 1000 Hz; 0 dBm0; A-law or µ-law;

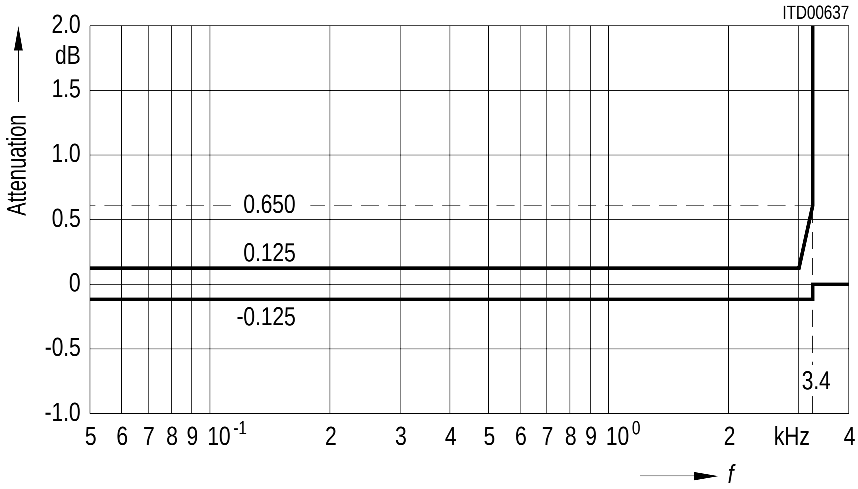
A 0 dBm0 signal is equivalent to 1.5763 [1.5710] Vrms. A 3.14 [3.17] dBm0 signal is equivalent to 2.263 Vrms which corresponds to the overload point of 3.2 V (A-law, [µ-law]).

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Gain (either value)[1)					
Gain absolute (AGR = AGX = 0)	G				
T_A = 25 °C, V_{DD} = 5 V, V_{SS} = – 5 V		– 0.2	± 0.06	0.2	dB
T_A = 0–70 °C, V_{DD} = 5 V ± 5%, V_{SS} = – 5 V ± 5%		– 0.3		0.3	dB
Gain absolute (AGR = 0 to 14 dB, AGX = 0 to 14 dB)	G				
T_A = 0–70 °C; V_{DD} = 5 V ± 5%, V_{SS} = – 5 V ± 5%		– 0.4	± 0.10	0.4	dB
Total harmonic distortion, 0 dBm0; f = 300 Hz to 3400 Hz	*THD*		– 50	– 44	dB
Intermodulation 2f1 – f2[2)	*IMD*			– 42	dB
2f1 – f2[3)				– 56	dB
Crosstalk 0 dBm0; f = 300 Hz to 3400 Hz					
Transmit to receive	CT_{XR}		– 85	– 80	dB
Receive to transmit	CT_{RX}		– 85	– 80	dB
Idle channel noise,					
transmit, psophometric, A-law VIN = 0 V	N_{TP}			– 67.4	dBm0p
transmit, C-message, µ-law VIN = 0 V	N_{TC}			17.5	dBrnc
receive, psophometric, A-law idle code + 0	N_{RP}		– 82	– 78	dBm0p
receive, C-message, µ-law idle code + 0	N_{RC}		8	12	dBrnc

1) R_L = 300 Ω causes an additional attenuation in the range between – 0.1 to 0 dB.
2) Equal input levels in the range between – 4 dBm0 and – 21 dBm0; different frequencies in the range between 300 Hz and 3400 Hz.
3) Input level – 9 dBm0, frequency range 300 Hz to 3400 Hz and – 23 dBm0, 50 Hz.

Attenuation Distortion

Attenuation deviations stay within the limits in the figures below.



Receive: Reference frequency 1 kHz, input signal level 0 dBm0

Transmit: Reference frequency 1 kHz, input signal level 0 dBm0

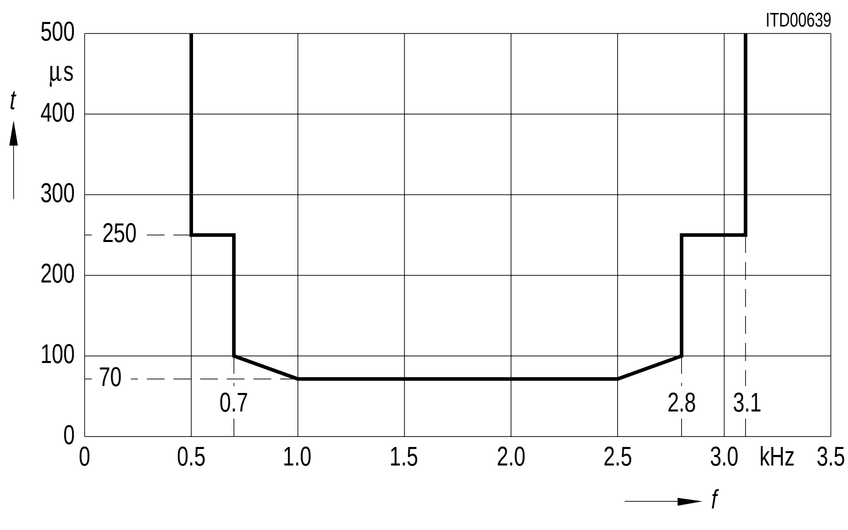
Group Delay

Maximum delays for operating the SICOFI with H(B) = H(Z) = 0 and H(R) = H(X) = 1, including delay through A/D- and D/A converters. Specific filter programming may cause additional group delays.

Group delay deviations stay within the limits in the figures below.

Group Delay Absolute Values: Input signal level 0 dBm0

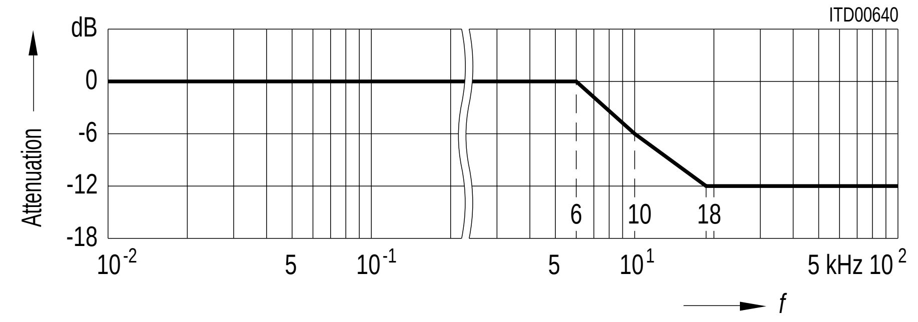
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Transmit Delay	D_{XA}			300	µs	f= 1.4 kHz
Receive Delay	D_{RA}			240	µs	f= 300 Hz

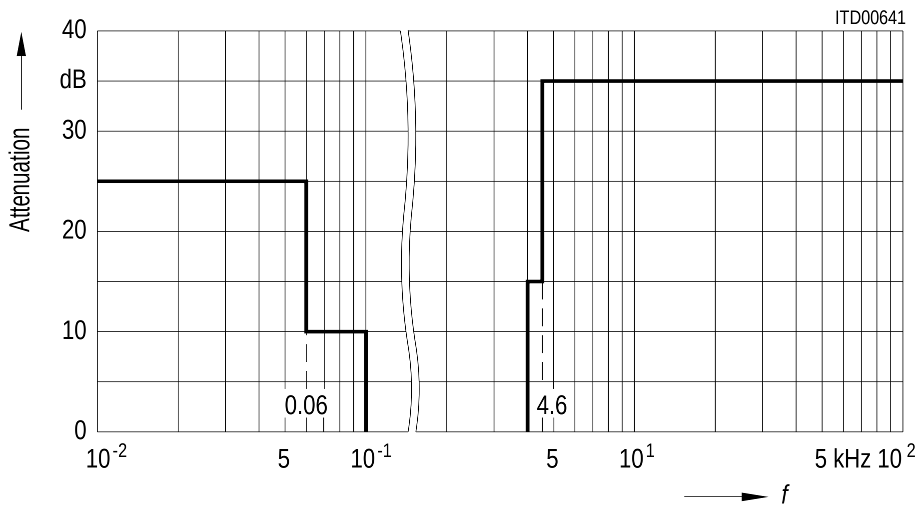


Group Delay Distortion: Input signal level 0 dBm0, reference frequency = 1.4 kHz

Out-of-Band Signals at Analog Input

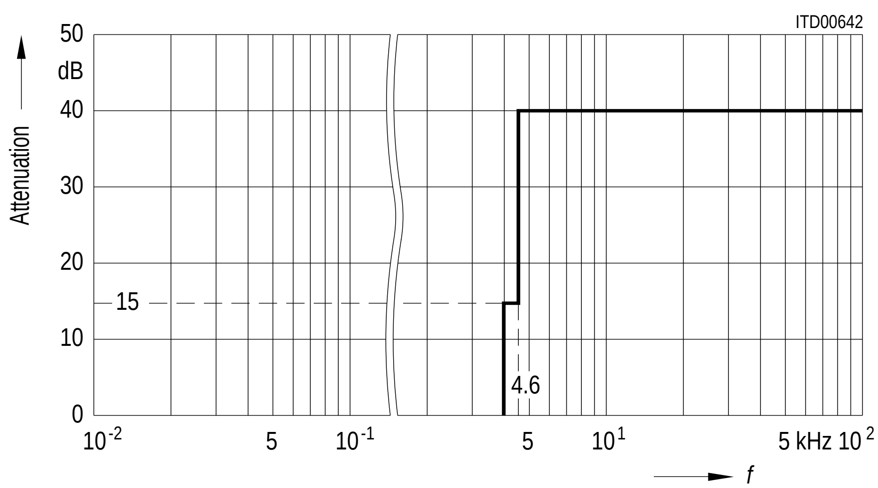
With an out-of-band sine wave signal with frequency *f* and level A applied to the analog input, the level of any resulting frequency component at the digital output will stay at least X dB below level A.





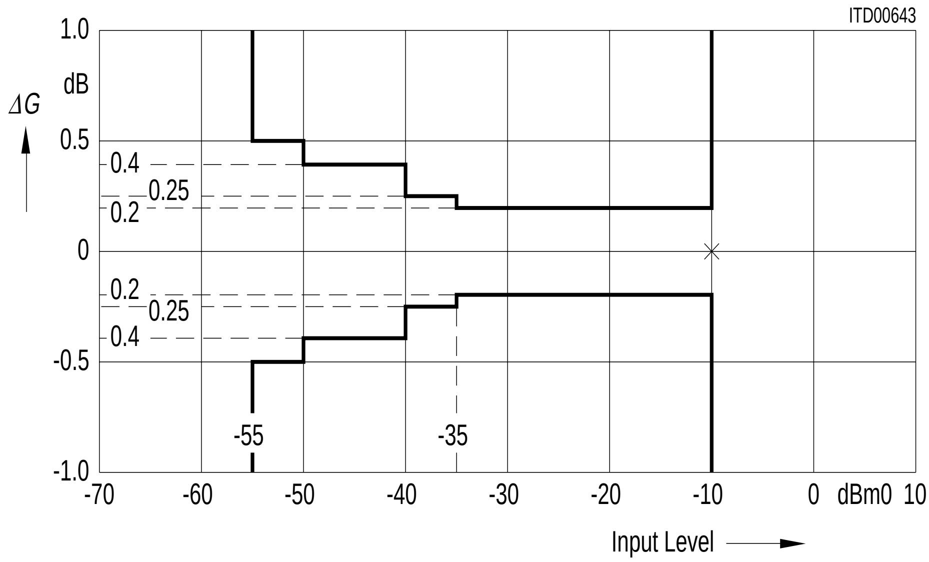
Out-of-Band Signals at Analog Output

With a 0 dBm0 sine wave of frequency *f* applied to the digital input, the level of any resulting out-of-band signal at the analog output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog output.

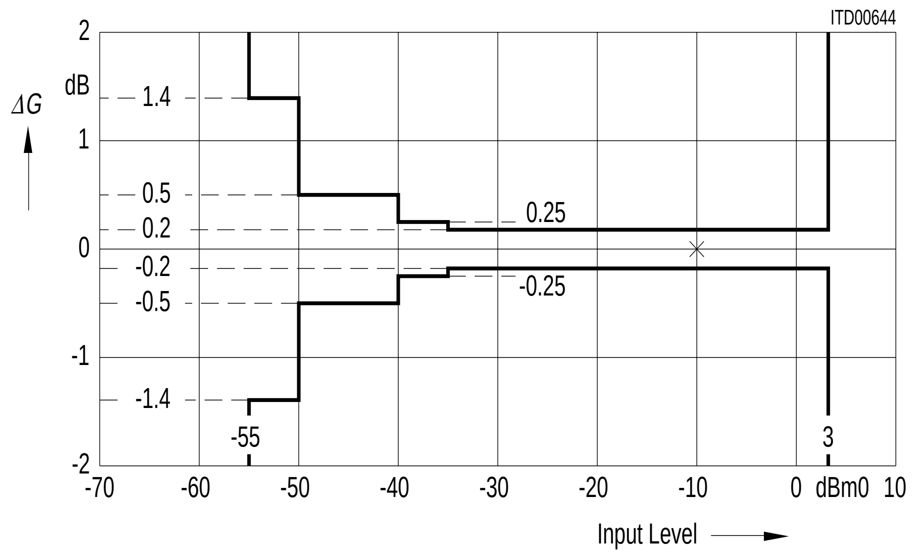


Gain Tracking (Receive and Transmit)

The gain deviations stay within the limits in the figures below



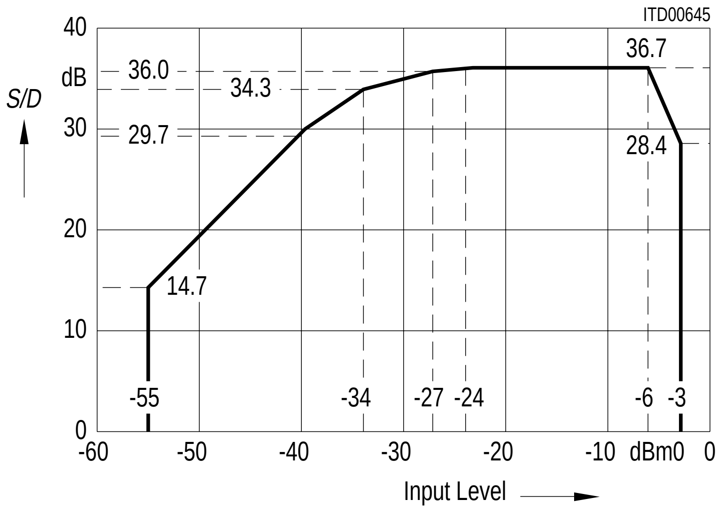
Gain Tracking: Measured with noise signal according to CCITT recommendations, reference level is – 10 dBm0, AGX = AGR = 0



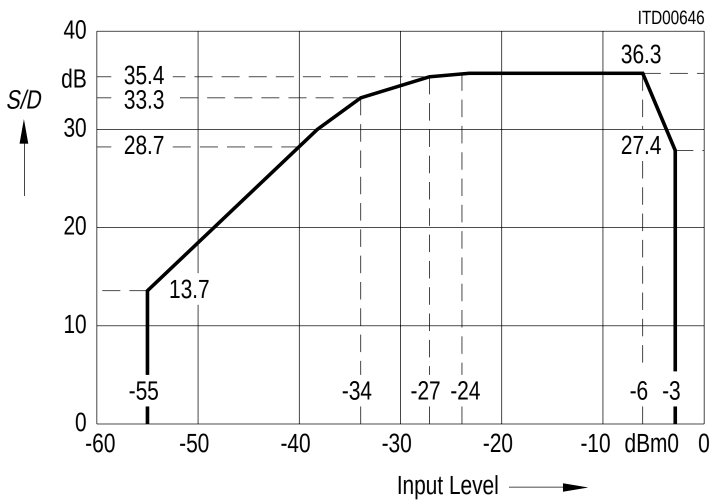
Gain Tracking: Measured with sine wave in the range 700 to 1100 Hz, reference level is – 10 dBm0, AGX = AGR = 0

Total Distortion

The signal-to-distortion ratio exceeds the limits in the following figures.

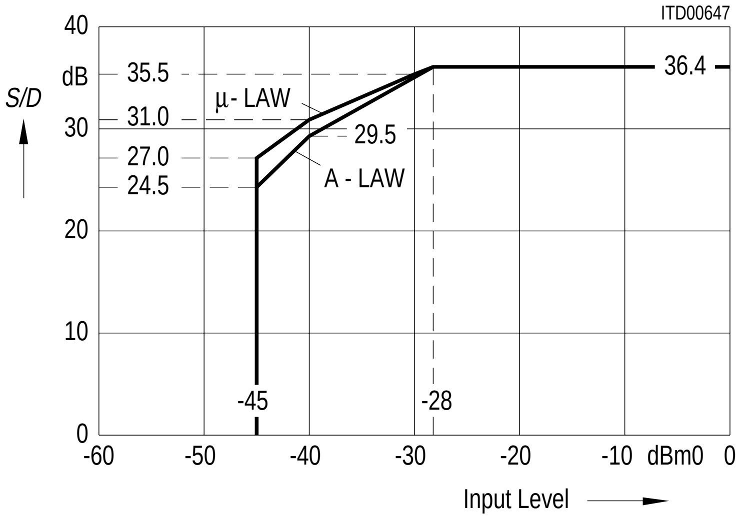


Receive: Measured with noise signal according to CCITT recommendations



Transmit: Measured with noise signal according to CCITT recommendations

The signal to distortion ratio exceeds the limits in the following figures.



Receive & Transmit: Measured with sine wave in the range 700 to 1100 Hz excluding submultiples of 8 kHz

Signal to Total Distortion CCITT Noise Signal Digital-Digital (A-law and μ-law)

Parameter			Total Distortion	
	Input Level	Unit	min.	Unit
Digital Loop Back via B-Filter or Digital Loop Back via Analog port	0	dBm0	31	dB
	– 30	dBm0	31	dB
	– 40	dBm0	25	dB
	– 45	dBm0	20	dB

Transhybrid Loss

The quality of transhybrid-balancing is very sensitive to deviations in gain and group delay – deviations inherent to the SICOFI A/D- and D/A-converters as well as to all external components used on a line card (SLIC, OP's etc.)

The SICOFI transhybrid loss is measured in the following way: A sine wave signal with level 0 dBm0 and a frequency in the range of 300 – 3400 Hz is applied to the digital input. The resulting analog output signal at pin VOUT is directly connected to VIN, e.g. with the SICOFI testmode "Digital Loop Back via Analog Port" (**see CR4**). The programmable filters R, GR, X, GX and Z are disabled, the balancing filter B is enabled with coefficients optimized for this configuration ($V_{OUT} = V_{IN}$).

The resulting echo measured at the digital output is at least X dB below the level of the digital input signal as shown in the table below.

B-filter coefficients recommended for transhybrid loss measurement with $V_{OUT} = V_{IN}$

	COP-Write	Coefficients							
B-filter part 1	(83)	FD	29	FB	38	A1	A0	3C	42
B-filter part 2	(8B)	00	AF	62	2B	CF	D1	CA	A4
B-filter delay	(98)	19	19	11	19				

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	typ.		
Transhybrid loss at 500 Hz Transhybrid loss at 2500 Hz Transhybrid loss at 3000 Hz	THL_{500} THL_{2500} THL_{3000}	33 29 27	45 40 35	dB dB dB	T_A = 25 °C, V_{DD} = 5 V, V_{SS} = – 5 V, AGR = AGX = 0 dB
Transhybrid loss at 500 Hz Transhybrid loss at 2500 Hz Transhybrid loss at 3000 Hz	THL_{500} THL_{2500} THL_{3000}	29 27 25	40 35 30	dB dB dB	T_A = 0 to 70 °C, V_{DD} = 5 V ± 5 %, V_{SS} = 5 V ± 5 %, AGR = AGX = 0 dB
Transhybrid loss at 500 Hz Transhybrid loss at 2500 Hz Transhybrid loss at 3000 Hz	THL_{500} THL_{2500} THL_{3000}	27 25 23	40 35 30	dB dB dB	T_A = 0 to 70 °C, V_{DD} = 5 V ± 5 %, V_{SS} = – 5 V ± 5 %, AGR = AGX = 6.03, 12.06, 14.00 dB

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
V_{DD} referred to GNDD		– 0.3	5.5	V
V_{SS} referred to GNDD		– 5.5	0.3	V
GNDA to GNDD		– 0.6	0.6	V
Analog input and output voltage referred to V_{DD} = 5 V, V_{SS} = – 5 V referred to V_{SS} = – 5 V, V_{DD} = 5 V	 V_{IN} V_{IN}	 – 10.3 – 0.3	 0.3 10.3	 V V
All digital input voltages referred to GNDD = 0 V, V_{DD} = 5 V referred to V_{DD} = 5 V, GNDD = 0 V	 V_{IN} V_{IN}	 – 0.3 – 5.3	 5.3 0.3	 V V
DC input and output current at any input or output pin	I_{DC}		10	mA
Storage temperature	T_{stg}	– 60	125	°C
Ambient temperature under bias	T_A	– 10	80	°C
Power dissipation	P_D		1	W

Operating Range

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5%; V_{SS} = – 5 V ± 5%; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
V_{DD} supply current stand by operating	I_{DD}		 2.1 8	 4 12	 mA mA	
V_{SS} supply current stand by operating	I_{SS}		 1.7 5	 3 8	 mA mA	
Power supply rejection (of either supply/direction)	$PSRR$	30	44		dB	1 kHz 80 mVrms ripple
Power dissipation stand by Power dissipation operating	P_{Ds} P_{Do}		20 70	37 105	mW mW	

Electrical Characteristics

Digital Interface

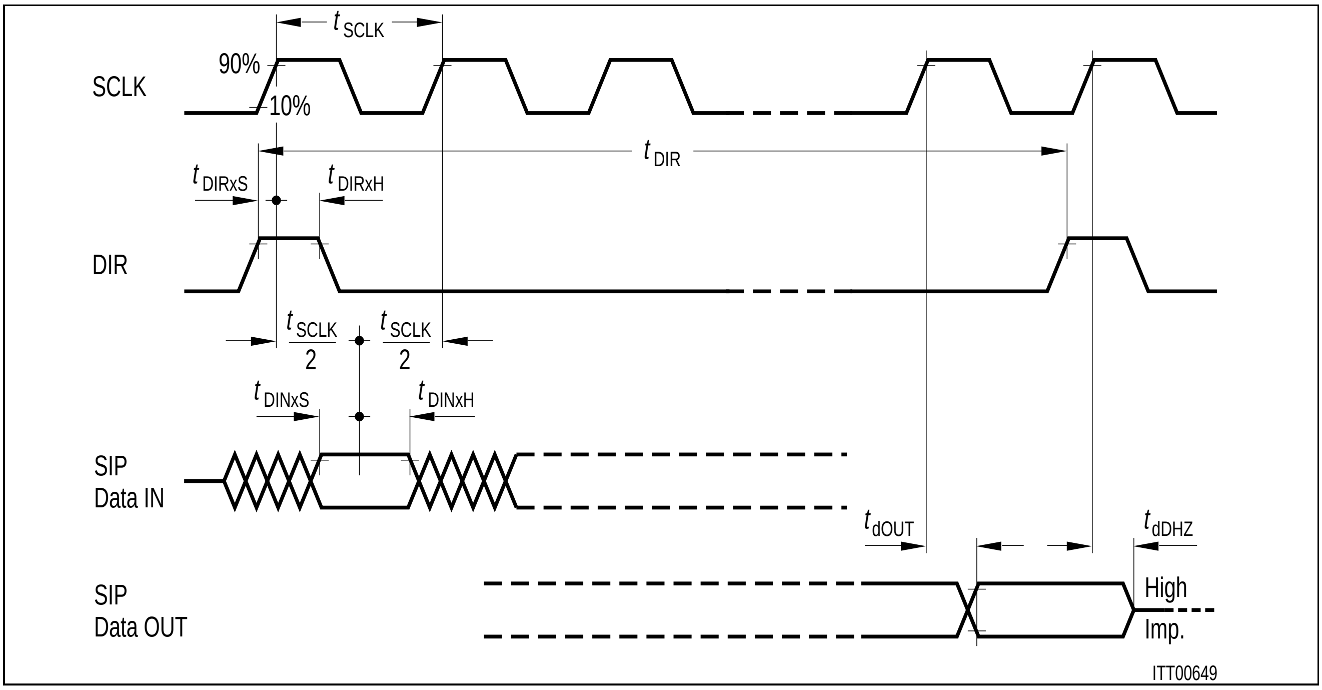
T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %; V_{SS} = – 5 V ± 5%; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
L-input voltage	V_{IL}	– 0.3	0.8	V	
H-input voltage	V_{IH}	2.0		V	
L-output voltage	V_{OL}		0.45	V	I_0 = – 2 mA
H-output voltage	V_{OH}	2.4		V	I_0 = 400 µA
Input leakage current	I_{IL}		± 1	µA	– 0.3 ≤ V_{IN} ≤ V_{DD}

Analog Interface

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5%; V_{SS} = – 5 V ± 5%; GNDD = 0 V; GNDA = 0 V

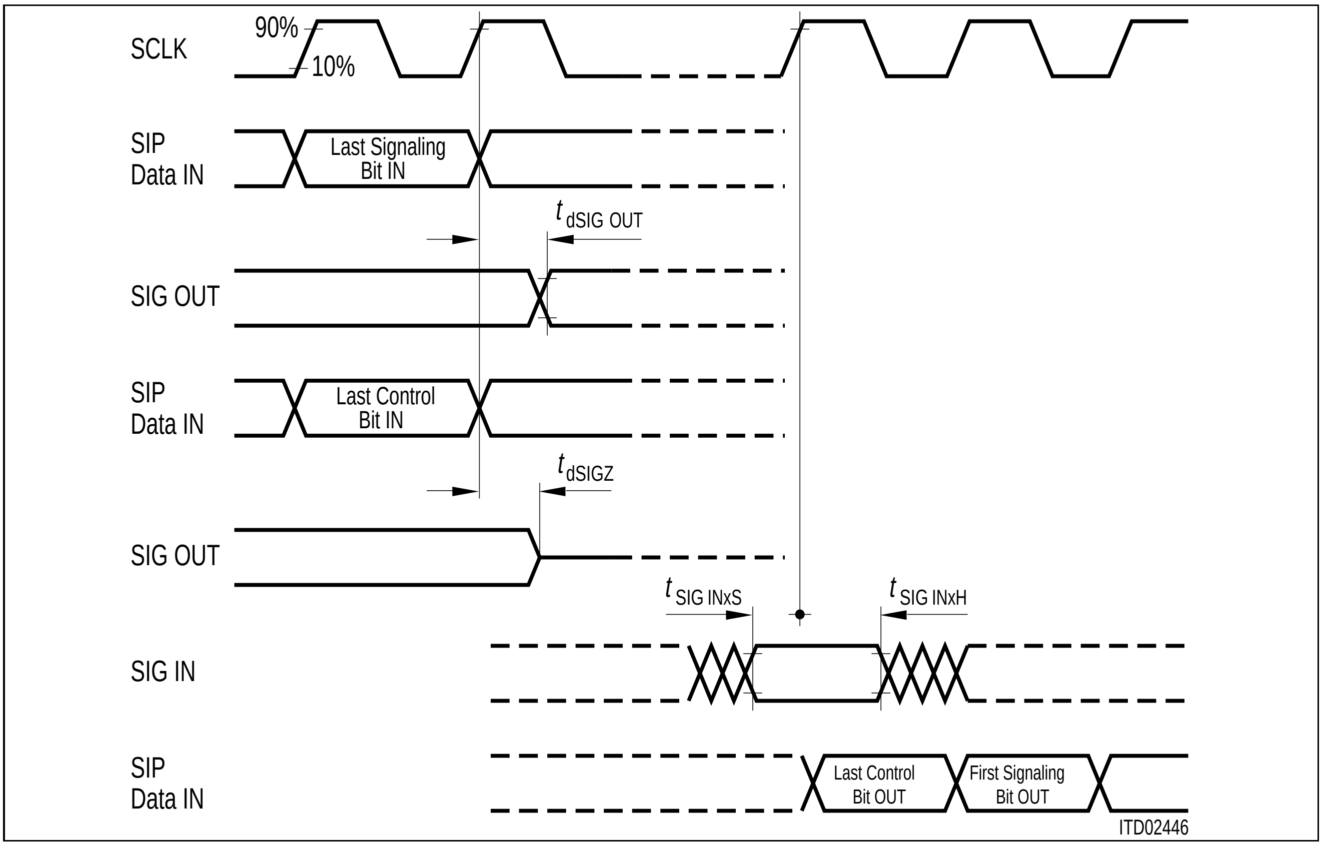
Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input resistance	R_I	10		MΩ	
Analog output resistance	R_O		10	Ω	
Input offset voltage	V_{IO}		± 50	mV	
Output offset voltage	V_{OO}		± 50	mV	
Input voltage range	V_{IR}		± 3.2	V	
Output voltage range	V_{OR}	± 3.1		V	R_L ≥ 300 Ω; C_L ≤ 50 pF



SIP Interface Timing (SLD-Bus)

Switching Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period SCLK	t_{SCLK}		1/512 kHz		
Duty cycle		20	50	80	%
Period DIR	t_{DIR}		125		µs
DIR setup time	$t_{DIR \times S}$	20	0	– 80	ns
DIR hold time	$t_{DIR \times H}$	250			ns
SIP data in setup time	$t_{DIN \times S}$	20			ns
SIP data in hold time	$t_{DIN \times H}$	100			ns
SIP data out delay	t_{dDOUT}		150	250	ns
SIP data out high impedance delay vs. SCLK	t_{dDHZ}		50	70	ns



Signaling Interface Timing

Switching Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Delay signaling out vs. SCLK[1]	$t_{dSIGOUT}$		250	350	ns
Delay signaling high impedance vs. SCLK	t_{dSIGZ}		150	200	ns
SIG in setup time[2]	$t_{SIGIN \times S}$	50			ns
SIG in hold time[2]	$t_{SIGIN \times H}$	100			ns
Reset pulse width[3]	t_{RES}	500			ns

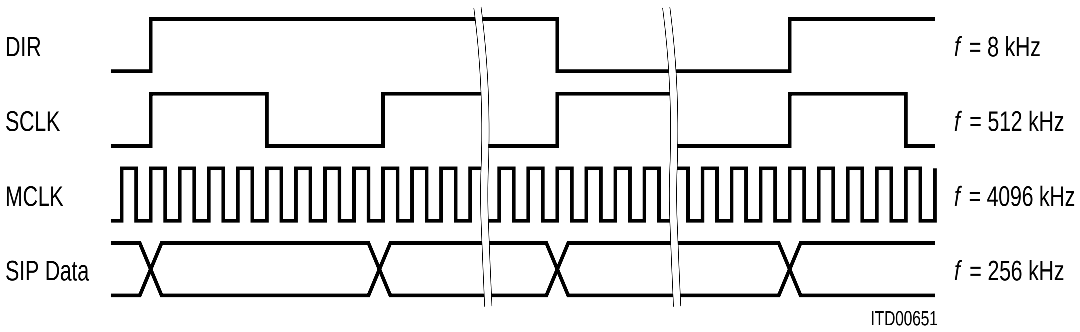
[1] Pins SO1 … SO3; Pins SA … SD as output
[2] Pins SI1 … SI3; Pins SA … SD as input
[3] SICOFI is ready to accept SOP/COP commands in the next DIR Cycle.
Spikes shorter than 244 ns will be ignored.

Appendix A

Specific Interface Types

The SICOFI can be used with three different SLD-bus type interfaces. A specific interface type is selected with three pins: TEST, SI3 and PLL.

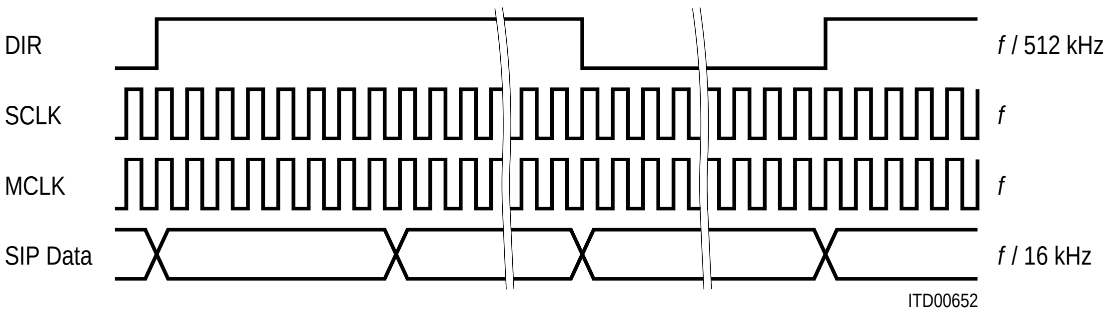
TEST	SI3	PLL
0	X	X



1) SLD-Bus Interface[1)]

TEST	SI3*)	PLL
1	0	0

*) SI3 cannot be used as Signaling Pin



2) SLD-Bus Interface with Variable Clock Frequencies[2)]

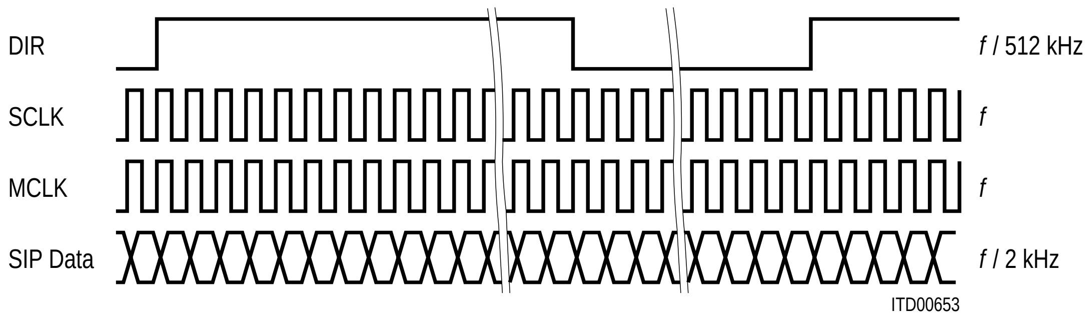
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1) 4096-kHz Masterclock MCLK is generated from 512-kHz SCLK by on chip PLL

2) Maximum MCLK-frequency = 8 MHz

TEST	SI3*)	PLL
1	0	1

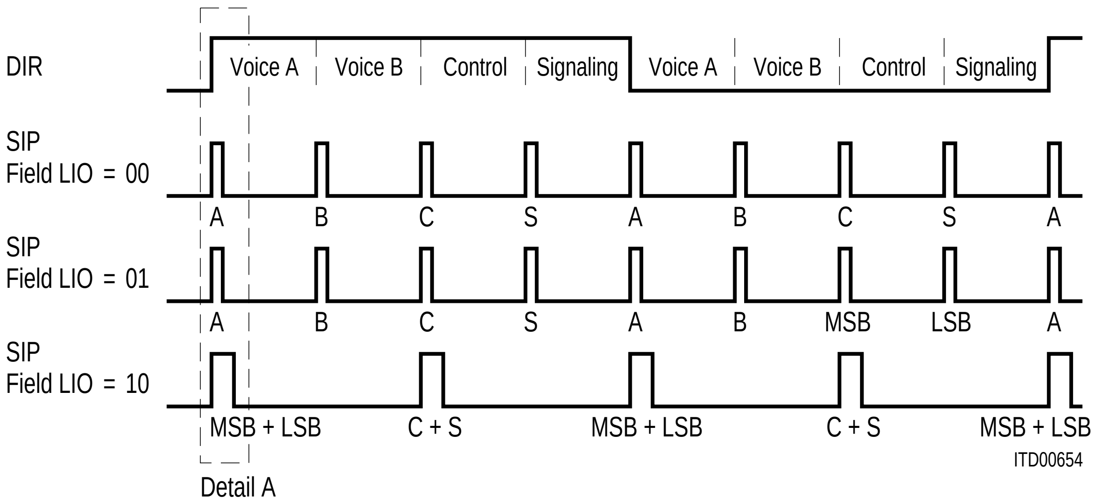
*) SI3 cannot be used as Signaling Pin

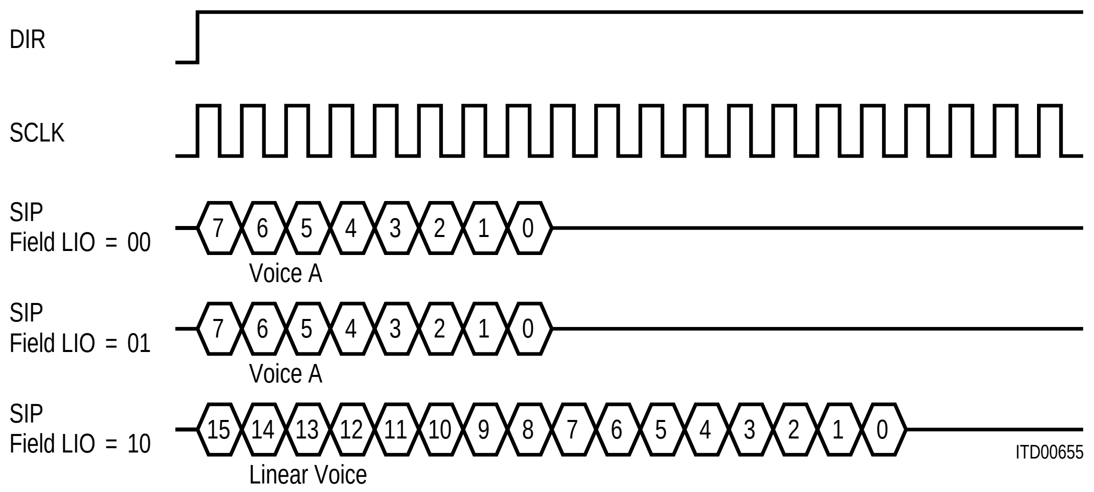


3) Burst Mode Interface[1]

1) Maximum MCLK-frequency = 8 MHz

In burst-mode 8- or 16-bit bursts are received or transmitted, depending on the linear mode selected (**see** field LIO in **CR3**).





Detail A

A …	voice A	C … control
B …	voice B	S … signaling
MSB …	bit 15-8 of linear in- or output	
LSB …	bit 7-0 of linear in- or output	

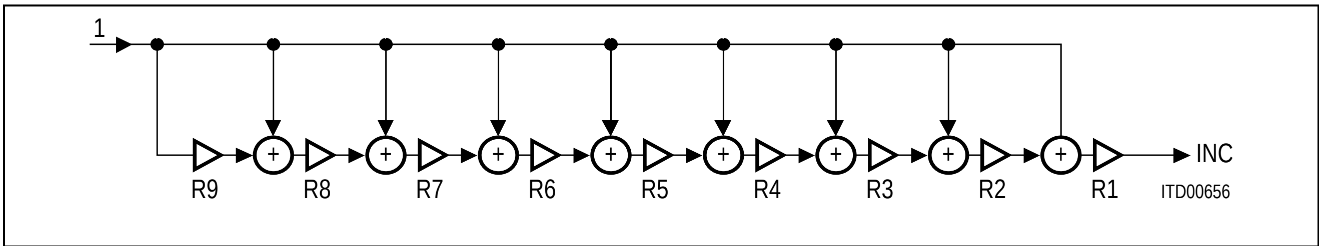
Appendix B

On Chip Tone Generation

By setting field TM3 in CR4 to ’100’ the on-chip tone generator is activated with a fixed frequency of 2 kHz. The frequency f_{TONE} may be programmed via the R-filter coefficients (R-filter enabled) in the range of 0 to 4 kHz. The gain may be adjusted with the programmable GR-filter.
The trapezoidal tone generation algorithm used, provides for a harmonic distortion better than 27 dB.

Calculation of the R-filter Coefficients:

f_{TONE} : = 8192 $\times$ INC/f_{MCLK} with f_{MCLK}, f_{TONE} [kHz]
INC : = $S_{R1} \times 2^{-EXP_{R1}} \times (1 + S_{R2} \times 2^{-EXP_{R2}} \times (1 + S_{R3} \times 2^{-EXP_{R3}} \times (\ldots(\ldots(1 + S_{R9} \times 2^{-EXP_{R9}})\ldots))$
S … SIGN, EXP … EXPONENT



A_1 : = INC
FOR i : = 1 TO 9 DO
FIND S_i, EXP_i: FOR ($|A_i - S_i \times 2^{-EXP_i}|$) = MIN; $S_i \in (-1, 1)$, $EXP_i \in (0 \ldots 7)$
A_{i+1} : = $(A_i / S_i \times 2^{-EXP_i}) - 1$
R_i : = [$(-S_i + 1)/2$), BIN(EXP_i)] (to be transferred to the SICOFI)
NEXT i

Programming Byte Sequence for Selected Frequencies

Coefficients		Frequency Hz										
		2000	**1000**	**800**	**697**	**770**	**852**	**941**	**1209**	**1336**	**1477**	**1633**
COP write*)		2B/AB	2B/AB	2B/AB	2B/AB	2B/AB	2B/AB	2B/AB	2B/AB	2B/AB	2B/AB	2B/AB
X	X	00	00	00	00	00	00	00	00	00	00	00
X	X	00	00	00	00	00	00	00	00	00	00	00
X	X	00	00	00	00	00	00	00	00	00	00	00
*R*1	X	00	10	10	20	10	10	10	10	10	10	00
*R*3	*R*2	8F	8F	AA	A1	CA	3B	CC	B2	22	D1	1B
*R*5	*R*4	8F	8F	AA	2B	32	C1	BB	22	A1	C1	5C
*R*7	*R*6	8F	8F	AA	4B	2D	BB	12	5F	5F	BB	CA
*R*9	*R*8	8F	8F	AA	B1	B3	12	DA	8F	1B	12	13

X don’t care
*) 2B for SICOFI A, AB for SICOFI B.

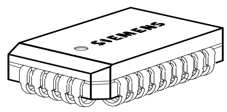
SIEMENS

Dual Channel Codec Filter (SICOFI®-2)

PEB 2260
PEF 2260

CMOS IC

Features



P-LCC-28-R

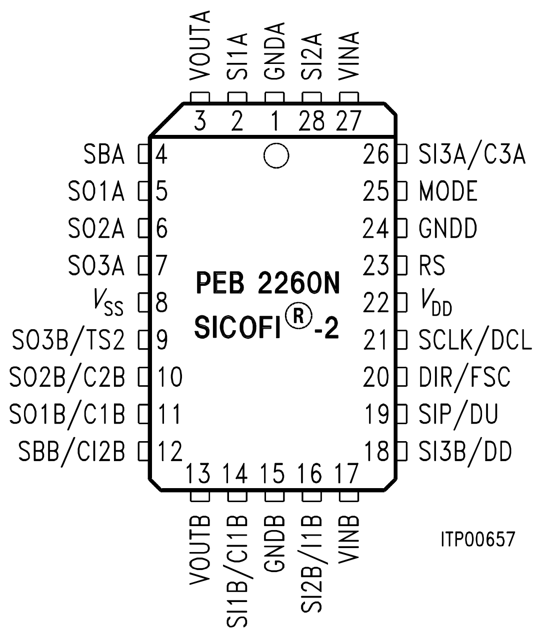
- Dual channel single chip codec and filter
- Band limitation according to all CCITT and AT&T recommendations
- Digital signal processing techniques
- PCM encoded digital voice transmission (A-law or μ-law)
- Programmable digital filters for
  - impedance matching
  - transhybrid balancing
  - gain
  - frequency response correction
- Two digital Interfaces
  - three pin serial SLD Interface (eg. to PEB 2050/52)
  - four pin serial IOM®-2 Interface with two different clock-frequencies and time-slot assignment (e.g. to PEB 2055/56)
- Programmable signaling interface to peripherals (e.g. SLIC)
- High performance A/D and D/A conversion
- Programmable analog gain adjustment
- Advanced test capabilities
  - three digital loop back modes
  - two analog loop back modes
  - two programmable tone generators
- No trimming or adjustments
- No external components
- Advanced low power 2μCMOS technology
- Power supply + / – 5 V
- Meets or exceeds CCITT and LSSGR recommendations
- Two types are available:
  - PEB 2260 with standard temperature range 0...70°C
  - PEF 2260 with extended temperature range -40...85°C

Type	Version	Ordering Code	Package
PEB 2260-N	V 2.0	Q67100-H6191	P-LCC-28-R (SMD)
PEF 2260-N	V 2.0	Q67100-H6261	P-LCC-28-R (SMD)

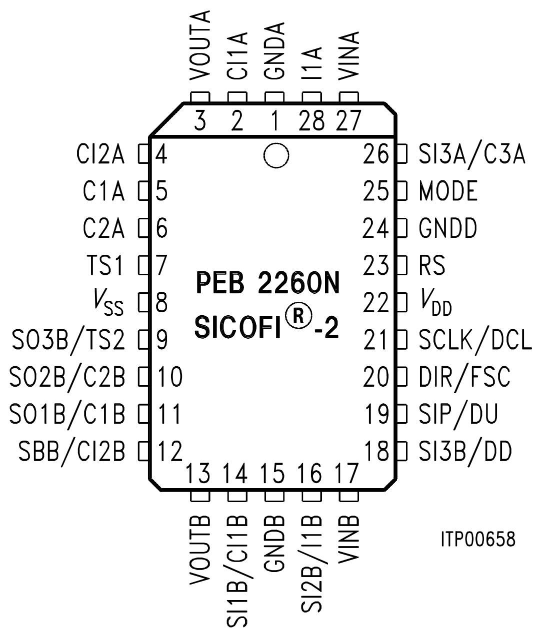
General Description

The Dual Channel Codec Filter PEB 2260 (SICOFI®-2) is a fully integrated PCM codec and filter fabricated in low power 2µCMOS technology for applications in digital communication systems. Based on an advanced digital filter concept, the PEB 2260 provides excellent transmission performance and high flexibility. The digital signal processing approach includes attractive programmable features such as transhybrid balancing, impedance matching, gain and frequency response correction.

Pin Configuration for SLD Mode
(top view)



Pin Configuration for IOM®-2 Mode
(top view)



Pin Definitions and Functions for SLD Interface Mode

Pin No.	Symbol	Input (I) Output (O)	Function
22	V_{DD}	I	+ 5 V power supply
8	V_{SS}	I	– 5 V power supply
24	GNDD	I	Ground digital. Not internally connected to GNDA or GNDB. All digital signals are referred to this pin
1	GNDA	I	Ground analog channel A. Not internally connected to GNDD or GNDB. All channel A analog signals are referred to this pin
15	GNDB	I	Ground analog channel B. Not internally connected to GNDD or GNDA. All channel B analog signals are referred to this pin
27	VINA	I	Channel A analog voice input
3	VOUTA	O	Channel A analog voice output
17	VINB	I	Channel B analog voice input
13	VOUTB	O	Channel B analog voice output
25	MODE	I	Operating mode selection, SLD or IOM-2 Interface: connected to '0' for SLD interface mode
21	SCLK	I	Slave clock, 512 kHz
20	DIR	I	Direction Signal, 8-kHz frame synchronisation
19	SIP	I/O	Serial interface port, bidirectional serial data port
23	RS	I	Reset input, RS forces the SICOFI-2 to basic setting mode
2	SI1A	I	Signaling inputs: data present at SI1A ... SI3B are sampled and transmitted via the serial interface
28	SI2A	I	
26	SI3A	I	
14	SI1B	I	
16	SI2B	I	
18	SI3B	I	

Pin Definitions and Functions for SLD Interface Mode (continued)

Pin No.	Symbol	Input (I) Output (O)	Function
5	SO1A	O	Signaling outputs: data received via the serial interface are latched and fed to SO1A ... SO3B
6	SO2A	O	
7	SO3A	O	
11	SO1B	O	
10	SO2B	O	
9	SO3B	O	
4	SBA	I/O	Bidirectional signaling pins: SBA, SBB pins may be programmed as input or output individually with adequate SICOFI-2 status settings
12	SBB	I/O	

Pin Definitions and Functions for IOM®2 Interface Mode

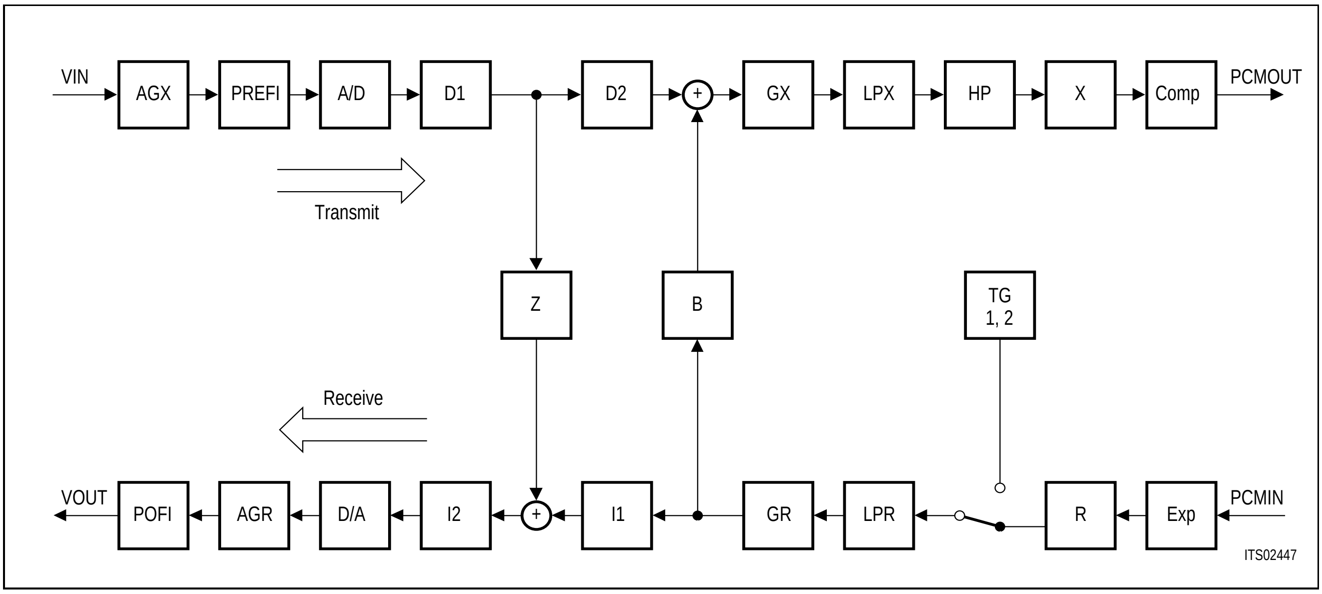
Pin No.	Symbol	Input (I) Output (O)	Function
22	V_{DD}	I	+ 5 V power supply
8	V_{SS}	I	– 5 V power supply
24	GNDD	I	Ground digital. Not internally connected to GNDA or GNDB. All digital signals are referred to this pin
1	GNDA	I	Ground analog channel A. Not internally connected to GNDD or GNDB. All channel A analog signals are referred to this pin
15	GNDB	I	Ground analog channel B. Not internally connected to GNDD or GNDA. All channel B analog signals are referred to this pin
27	VINA	I	Channel A analog voice input
3	VOUTA	O	Channel A analog voice output
17	VINB	I	Channel B analog voice input
13	VOUTB	O	Channel B analog voice output
25	MODE	I	Operating mode selection, SLD or IOM-2 Interface: connected to '1' for IOM-2 interface mode

Pin Definitions and Functions for IOM®2 Interface Mode (continued)

Pin No.	Symbol	Input (I) Output (O)	Function
21	DCL	I	Data clock, 512 kHz or 4096 kHz
20	FSC	I	Frame synchronisation clock, 8 kHz
19	DU	O	Data upstream
18	DD	I	Data downstream
23	RS	I	Reset input, RS forces the SICOFI-2 to basic setting mode
28	I1A	I	Indication inputs: data present at I1A ... I1B are sampled and transmitted via the serial interface
16	I1B	I	
5	C1A	O	Command outputs: data received via the serial interface are latched and fed to C1A ... C3A and C1B ... C2B
6	C2A	O	
26	C3A	O	
11	C1B	O	
10	C2B	O	
2	CI1A	I/O	Bidirectional command/indication pins: CI1A ... CI2B may be programmed as input or output individually with adequate SICOFI-2 status settings
4	CI2A	I/O	
14	CI1B	I/O	
12	CI2B	I/O	
7	TS1	I	Time-slot selection pins 1 ... 2 with ternary logic
9	TS2	I	

SICOFI®-2 Principles

The SICOFI-2 codec filter solution is a highly digital approach utilizing the advantages of digital signal processing such as excellent performance, high flexibility, easy testing, no sensitivity to fabrication and temperature variations, no problems with crosstalk and power supply rejection.



SICOFI®-2 Signal Flow Graph (for either channel)

Transmit Direction

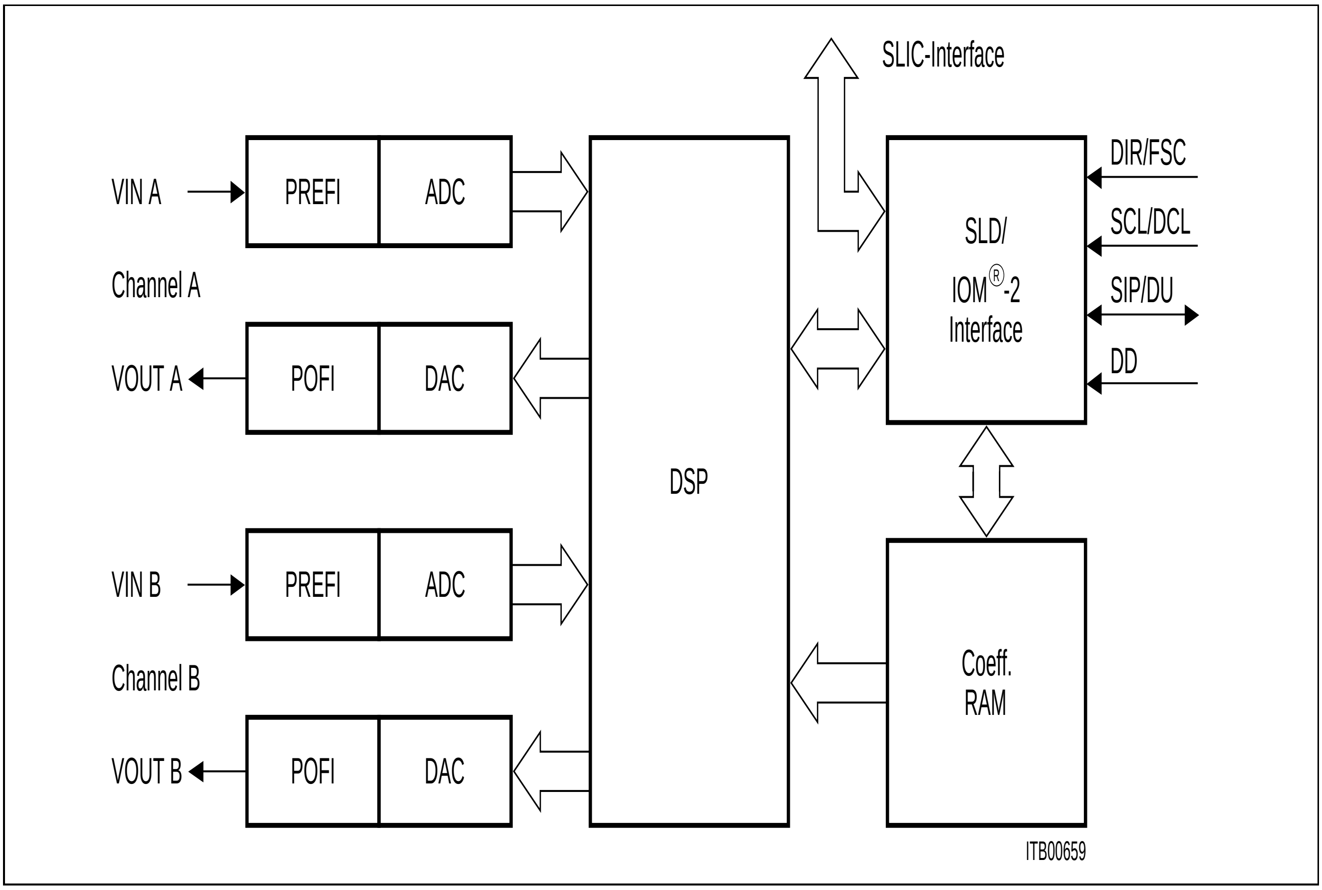
The analog input signal is A/D converted, digitally filtered and transmitted PCM-encoded. Antialiasing is done with a 2nd order Sallen-Key prefilter (PREFI). The A/D Converter (ADC) is a modified slopeadaptive interpolative sigma-delta modulator with a sampling rate of 128 kHz. Digital downsampling to 8 kHz is done by subsequent decimation filters D1 and D2 together with the transmit PCM lowpass filter (LPX).

Receive Direction

The digital input signal is received PCM-encoded, digitally filtered and D/A converted to generate the analog output signal. Digital interpolation up to 128 kHz is done by the receive PCM lowpass filter (LPR) and the interpolation filters I1 and I2. The D/A Converter (DAC) output is fed to the 2nd order Sallen-Key postfilter (POFI).

Programmable Functions

The high flexibility of the SICOFI-2 is based on a variety of user programmable filters, which are analog gain adjustment AGR and AGX, digital gain adjustment GR and GX, frequency response adjustment R and X, impedance matching filter Z and the transhybrid balancing filter B.



SICOFI®-2 Block Diagram

The SICOFI-2 bridges the gap between analog and digital voice signal transmission in modern telecommunication systems.

High performance oversampling Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) provide the conversion accuracy required. Analog antialiasing prefilters (PREFI) and smoothing postfilters (POFI) are included. The dedicated on chip Digital Signal Processor (DSP) handles all the algorithms necessary, e.g. PCM bandpass filtering, sample rate conversion and PCM companding. The SLD or IOM-2 Interface handles digital voice transmission, SICOFI-2 feature control and access to the SICOFI-2 signaling pins. Specific filter programming is done by downloading coefficients to the coefficient ram (CRAM).

SICOFI®-2 Digital Interfaces

The SICOFI-2 digital interface section consists of a serial interface bus which can be configured to be compatible to SLD or the IOM-2 standard (with two different data clock frequencies), and a powerful signaling interface.

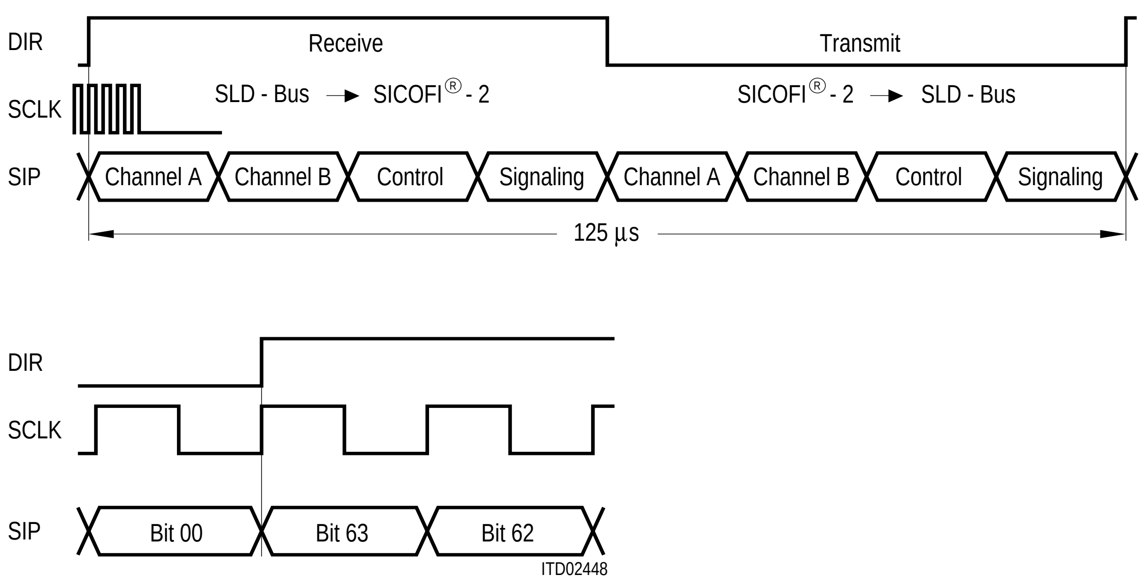
Selecting between the IOM-2 and SLD interfacing mode is simply performed by strapping the MODE pin.

MODE = ’0’ : SLD Interface
MODE = ’1’ : IOM-2 Interface

For better understanding, pin names are quoted with their interface specific name. E.g. pin SIP/DU: SIP for SLD interface mode, DU for IOM-2 interface mode.

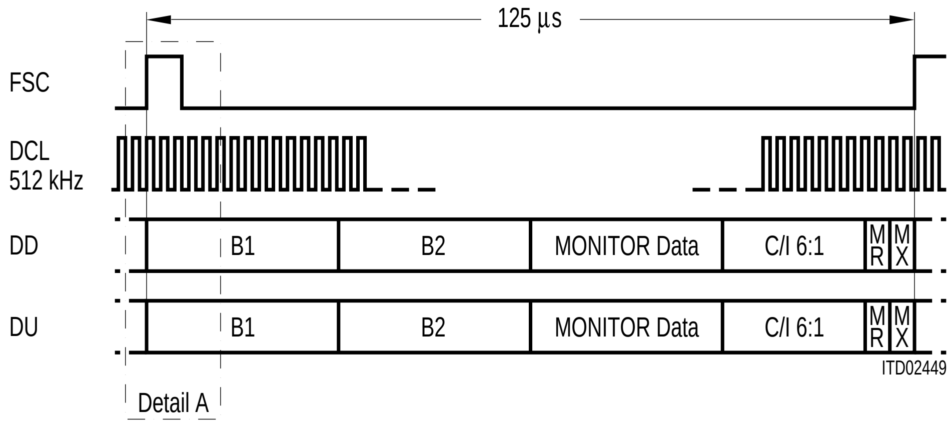
SLD Interface

The SLD serial interface consists of a bidirectional pin SIP, a data clock input SCLK, and a synchronization input DIR. Data bits are loaded or read out by the serial interface pin SIP. Bits are clocked in at the falling edge and clocked out at the rising edge of the slave clock pin SCLK (512 kHz). DIR and SCLK inputs must be phase locked. A SLD frame lasts 125 µs and consists of 32 bits transferred to the SICOFI-2 followed by 32 bits transferred from the SICOFI-2 to the SLD bus. The SLD interface thus provides a full duplex 256 kbit/s communication channel. This channel is subdivided in two 64 kbit/s voice/data channels, a 64 kbit/s feature control channel and an other 64 kbit/s signaling channel per direction. Bytes in all channels are serialized MSB first.

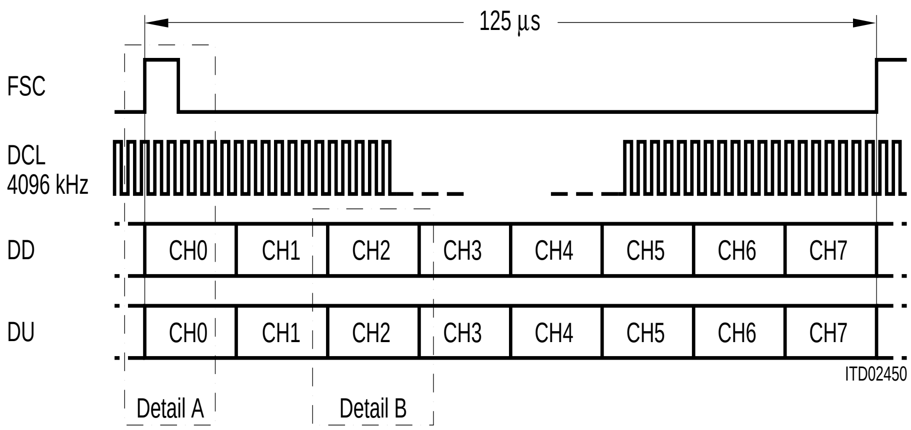


IOM®-2 Interface

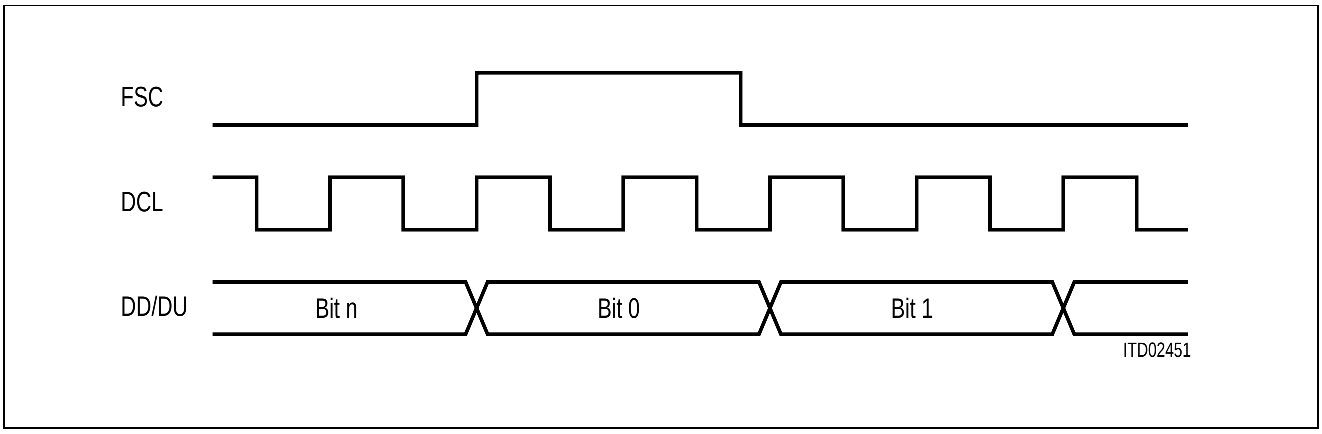
The IOM-2 interface consists of two data lines and two clock lines. DU (data upstream) carries data from the SICOFI-2 to a master device. DD (data downstream) carries data from the master device to the SICOFI-2. A 8 kHz FSC (frame synchronization clock) signal as well as a 512 kHz or 4096 kHz DCL (data clock) signal is supplied. The SICOFI-2 implements all functions for analogue devices as described in the IOM-2 specification.



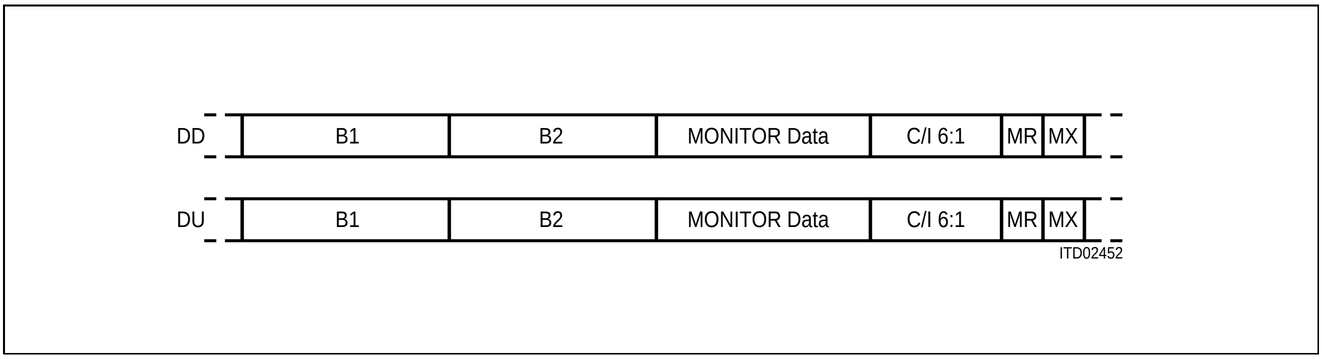
IOM®-2 Interface, DCL = 512 kHz (one channel per frame)



IOM®-2 Interface, DCL = 4096 kHz (eight channels per frame)



Detail A



Detail B

With a DCL frequency of 4096 kHz assignment of 8 time slots is possible. The IOM-2 operating mode and time-slot selection is set completely by pin-strapping of two pins TS1 and TS2, which work with ternary logic (– 5 V [N], 0 V [0] and + 5 V [P]).

TS2	TS1	IoM-2 Operating Mode
N	N	IOM-2, DCL = 512 kHz
0	0	IOM-2, DCL = 4096 kHz, time slot 0
N	0	IOM-2, DCL = 4096 kHz, time slot 1
0	P	IOM-2, DCL = 4096 kHz, time slot 2
N	P	IOM-2, DCL = 4096 kHz, time slot 3
P	0	IOM-2, DCL = 4096 kHz, time slot 4
0	N	IOM-2, DCL = 4096 kHz, time slot 5
P	P	IOM-2, DCL = 4096 kHz, time slot 6
P	N	IOM-2, DCL = 4096 kHz, time slot 7

IOM®-2 MONITOR Channel Data Structure

The MONITOR channel is used for the transfer of maintenance information between two functional blocks. By use of two MONITOR control bits (MR and MX) per direction, the data are transferred in a complete handshake procedure.

The messages transmitted in the MONITOR channel may have different kinds of data structures. Therefore, the first byte of the message is used to indicate the structure of the following data.

Messages to and from the SICOFI-2 are started with the following byte:

BIT	7	6	5	4	3	2	1	0
	1	0	0	0	0	0	0	1

Thus providing information for two analog lines, the SICOFI-2 is one device on one IOM-2 channel. MONITOR data for a specific analog channel is selected by the SICOFI-2 specific command following.

For more details on IOM-2 MONITOR channel data structure, and an IOM-2 specific identification command **see Appendix B**.

Programming

A message oriented byte transfer is used, due to the fact that the SICOFI-2 needs extended control information. With the appropriate commands, data can be written to the SICOFI-2 or read from the SICOFI-2 via the SLD or via the IOM-2 interface monitor channel.

Data transfer to the SICOFI-2 starts with a write command, followed by up to 8 bytes of data. The SICOFI-2 responds to a read command with the requested information, that is up to 8 bytes of data. (**see Programming procedure**).

The same command structure is used both in SLD and IOM-2 interface mode. If the SICOFI-2 is operating in IOM-2 interface mode, any new command sequence starts with a SICOFI-2 specific address-byte. The following command is the same in SLD and IOM-2 mode. If the command requests an answer, in SLD mode the SICOFI-2 will start immediately (next transmission period) with the requested data. In IOM-2 mode the SICOFI-2 specific address byte will be sent first, followed by the requested data.

Attention: In IOM-2 mode, each byte on the monitor channel, is sent twice at least.

Example for a programming sequence in SLD and IOM-2 interface mode:

SLD Interface		IOM-2 Interface	
Receive	**Transmit**	**Receive**	**Transmit**
		Address	
SOP-Write		SOP-Write	
CR2		CR2	
CR1		CR1	
SOP-Read	CR2	SOP-Read	
	CR1		Address
			CR2
			CR1

Control Bytes

The 8-bit control bytes consist of either commands, status information or data. There are three different classes of SICOFI-2 commands:

NOP	**NO OPERATION:**	no status modification or data exchange
SOP	**STATUS OPERATION:**	SICOFI-2 status setting/monitoring
COP	**COEFFICIENT OPERATION:**	filter coefficient setting/monitoring

The class of command is selected by bit 3 and 2 of the control byte as shown below.

BIT	7	6	5	4	3	2	1	0
NOP					1	1		
SOP					0	1		
COP					X	0		

X … don't care

Due to the extended SICOFI-2 feature control facilities, SOP and COP commands contain additional information for programming and verifying the SICOFI-2.

Programmable Devices

3 configuration registers per channel:	CR1, CR2, CR3
1 coefficient ram per channel:	CRAM
1 common configuration register:	CR4 is only available in IOM-2 mode the contents of CR4 is valid for both channels

To obtain more clarity, bit fields containing different informations for SLD and IOM-2 interface are high lighted in subsequent chapters.

NOP Command

If no status modification of the SICOFI-2 is required, a no operation byte NOP may be transferred.

NOP receive, not useful in IOM-2 interface mode

BIT	7	6	5	4	3	2	1	0
	X	X	X	X	1	1	X	X

NOP transmit, only available in SLD interface mode

BIT	7	6	5	4	3	2	1	0
	1	1	PDA	PDB	VERSION			

PDA	PDA = 1	if channel A is in power-down mode
	PDA = 0	if channel A is in power-up mode
PDB	PDB = 1	if channel B is in power-down mode
	PDB = 0	if channel B is in power-up mode
VERSION	Four bit SICOFI-2 version identification	
	VERSION = 1111 for PEB2260 V1.X, V2.0	

SOP Command

To modify or evaluate the SICOFI-2 status, the contents of up to three (four) configuration registers CR1, CR2, CR3 (and CR4) may be transferred to or from the SICOFI-2. This is done by a SOP-Command (status operation command). In SLD interface mode three configuration registers per channel are accessible. If the SICOFI-2 is operating with IOM-2 interface an additional fourth configuration register (CR4) can be written or read.

BIT	7	6	5	4	3	2	1	0
	AD	R/W	PU	RST	0	1	LSEL	

AD Address Information

AD = 0	channel A is addressed with this command
AD = 1	channel B is addressed with this command

R/W Read/Write Information: Enables reading from the SICOFI-2 or writing information to the SICOFI-2.

R/W = 0	Write to SICOFI-2
R/W = 1	Read from SICOFI-2

PU Power Up/Power Down

PU = 1	sets the assigned channel (see bit AD) of SICOFI-2 to power-up mode (operating)
PU = 0	resets the assigned channel of SICOFI-2 to power-down (standby mode)

RST Reset SICOFI-2

RST = 1	forces SICOFI-2 to enter the Basic Setting Mode (**see Operating Modes**).

LSEL Length select information (**see also Programming Procedure**)
This two bit field identifies the number of subsequent data bytes

	LSEL = 0 0	no byte following
	LSEL = 1 1	CR1 is following
	LSEL = 1 0	CR2 and CR1 are following
⇒	LSEL = 0 1	CR3, CR2 and CR1 are following in SLD interface mode
⇒		CR4*), CR3, CR2, CR1 are following in IOM-2 interface mode

*) Commands concerning CR4 are independent of bit AD in SOP command.

CR1 Configuration Register 1

Configuration register CR1 defines the basic SICOFI-2 settings, which are: enabling/disabling the programmable digital filters, programming of signaling pins, and selection of the PCM companding characteristics.

BIT	7	6	5	4	3	2	1	0
	B	Z	X	R	GX	GR	SB/C3A	LAW

B	Enable B - filter	
	B = 0	B - filter disabled, H(B) = 0
	B = 1	B - filter enabled
Z	Enable Z - filter	
	Z = 0	Z - filter disabled, H(Z) = 0
	Z = 1	Z - filter enabled
X	Enable X - filter	
	X = 0	X - filter disabled, H(X) = 1
	X = 1	X - filter enabled
R	Enable R - filter	
	R = 0	R - filter disabled, H(R) = 1
	R = 1	R - filter enabled
GR	Enable GR - filter	
	GR = 0	GR - filter disabled, H(GR) = 1
	GR = 1	GR - filter enabled
GX	Enable GX - filter	
	GX = 0	GX - filter disabled, H(GX) = 1
	GX = 1	GX - filter enabled
SB/C3A	SLD Interface mode: program bidirectional signaling pin SBA or SBB	
⇒	SB = 0	programmable signaling pin SBx is input
⇒	SB = 1	programmable signaling pin SBx is output
SB**/C3A**	IOM-2 interface mode: operation mode of pin C3A*)	
⇒	C3A = 0	pin C3A is programmed as command output
⇒	C3A = 1	pin C3A is detector select output (**see CR4**)
LAW	PCM - Law selection	
	LAW = 0	A - law
	LAW = 1	µ - law (µ255 PCM)

*) Setting bit C3A to '1' for either channel forces pin C3A to be detector select output.

CR2 Configuration Register 2

Configuration register CR2 sets analog gain control and enables two on-chip tone- generators. In IOM-2 operating mode two bidirectional command/indication pins are controlled.

BIT	7	6	5	4	3	2	1	0
	AGR		AGX		TG2	TG1	0/CI1	O/CI2

AGR Analog gain control receive-path

AGR = 0 0	0 dB
AGR = 0 1	6 dB attenuation
AGR = 1 0	11.95 dB attenuation
AGR = 1 1	13.9 dB attenuation

AGX Analog gain control transmit-path

AGX = 0 0	0 dB
AGX = 0 1	6 dB amplification
AGX = 1 0	11.95 dB amplification
AGX = 1 1	13.9 dB amplification

TG2 Enable on chip tone generation 2
With the R-filter disabled a 1 kHz, – 6 dBm0 sinusoidal signal is fed to the input of the receive lowpass filter LP. Frequency and gain can be set, by programming the R and GR-filter.

TG2 = 0	On chip tone generator 2 disabled
TG2 = 1	On chip tone generator 2 enabled

TG1 Enable on chip tone generation 1
With the R-filter disabled a 2 kHz, – 6 dBm0 sinusoidal signal is fed to the input of the receive lowpass filter LP. Frequency and gain can be set, by programming the R and GR-filter.

TG1 = 0	On chip tone generator 1 disabled
TG1 = 1	On chip tone generator 1 enabled

0/CI1 SLD Interface mode: this bit is reserved for future use and has to be set to '0'

0/**CI1** IOM-2 Interface mode: Command/indication pin CI1A or CI1B

⇒	CI1 = 0	Programmable signaling pin CI1x is indication input
⇒	CI1 = 1	Programmable signaling pin CI1x is command output

0/CI2 SLD Interface mode: this bit is reserved for future use and has to be set to '0'

0/**CI2** IOM-2 Interface mode: Command/indication pin CI2A or CI2B

⇒	CI1 = 0	Programmable signaling pin CI2x is indication input
⇒	CI1 = 1	Programmable signaling pin CI2x is command output

CR3 Configuration Register 3

This register is for accessing testmodes only

BIT	7	6	5	4	3	2	1	0
	SWP	DHP	COR	DTS	ALB		DLB	

SWP Swap channels[1)]

SWP = 0	VOUTA and VINA are assigned to SLD/IOM-2 channel A VOUTB and VINB are assigned to SLD/IOM-2 channel B
SWP = 1	VOUTA and VINA are assigned to SLD/IOM-2 channel B VOUTB and VINB are assigned to SLD/IOM-2 channel A

DHP Disable transmit highpass

DHP = 0	Highpass enabled
DHP = 1	Highpass disabled

COR Cut off receive path (analog voice output VOUTA or VOUTB is set to ’0’)

COR = 0	receivepath enabled
COR = 1	Analog voice output is set to ’0’

DTS Disable transmit signaling[1)]

DTS = 0	Transmission of signaling/indication data (on SIP/DU) is enabled
DTS = 1	Transmission of signaling/indication data (on SIP/DU) is disabled. SIP/DU is in high impedance state.

ALB Analog loop back[2)]

ALB = 0 0	No analog loop back established
ALB = 0 1	Analog loop back via Z-filter. H(Z) = 1 if Z-filter is disabled
ALB = 1 1	Far analog loop back (via 8 kHz, 16 bit linear)

DLB Digital loop back

DLB = 0 0	No digital loop back established
DLB = 0 1	Digital loop back via PCM-register (via 8 kHz, PCM)
DLB = 1 0	Digital loop back via B-filter (via 16 kHz), H(B) = 1 if B-filter is disabled
DLB = 1 1	Digital loop back via analog port (VIN = VOUT)

1) Setting bits SWP, DTS to ’1’ for either channel enables the function.
2) All other codes are reserved for future use.

CR4 Configuration Register 4 (available in IOM®-2 interface mode only)

Register CR4 configures the data-upstream command/indication channel. The content of CR4 is valid for both channels A and B.

BIT	7	6	5	4	3	2	1	0
	N				T			

Upstream Update Interval N

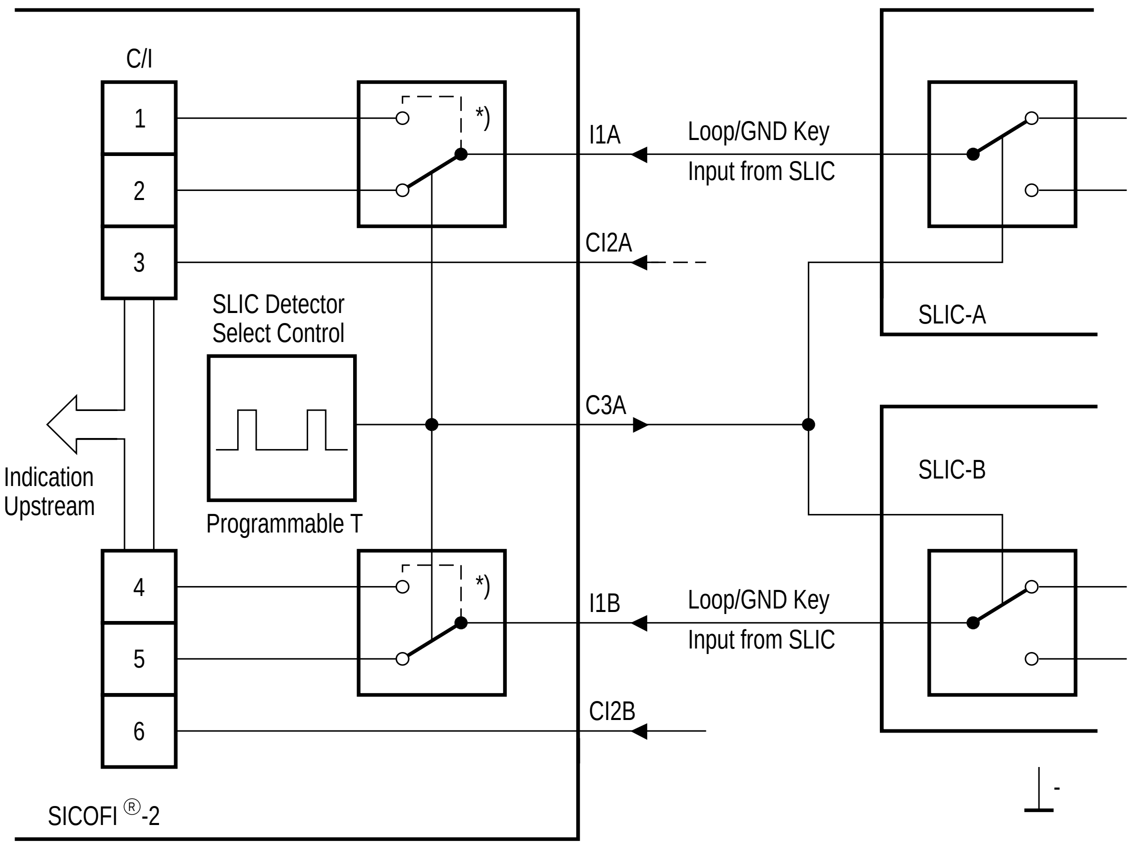
To restrict the rate of upstream C/I-bit changes, persistance checking of the status information from the SLIC may be applied.

New status information will be transmitted upstream, after it has been stable for N milliseconds. N is programmable in the range of 1 to 15 ms in steps of 1 ms, with N = 0 the persistance checking is disabled.

Field N				Update Interval Time
0	0	0	0	Persistance checking is disabled
0	0	0	1	Upstream transmission after 1 ms
0	0	1	0	Upstream transmission after 2 ms
. .	. .	. .	. .	. .
1	1	1	0	Upstream transmission after 14 ms
1	1	1	1	Upstream transmission after 15 ms

Detector Select Sampling Interval T

SLICs with multiplexed loop- and ground-key-status, which have a single status output pin for carrying the loop- and ground-key-status information, need a special detector select input
.



*) Connection available with 512-kHz IOM®-2 Interface only

SICOFI-2 pin C3A can be programmed as detector select output in CR1.
This command output pin is normally set to logical ’0’, such that the SLIC outputs loop status, which is passed to C/I-bits 1 and 4 via indication pins I1A and I1B.
Every T microseconds, the detector select output changes to logical ’1’ for a time of 15.63 µs. During this time the ground key status is read from the SLIC and transferred upstream using C/I-bits 2 and 5 via indication pins I1A and I1B.
The time interval T is programmable from 250 µs to 1.875 ms in 125 µs steps. It is possible to program the output to be permanently logical ’0’ or ’1’.

Field T				**Time Interval T Between Detector Select High States**
0	0	0	0	Detector select output C3A is programmed to ’0’ permanently
0	0	0	1	Time interval T is 250 µs
0	0	1	0	Time interval T is 375 µs
. .	. .	. .	. .	. .
1	1	1	0	Time interval T is 1.875 ms
1	1	1	1	Detector select output C3A is programmed to ’1’ permanently

COP Command

With a COP Command coefficients for the programmable filters can be written to the SICOFI-2 coefficient ram or transmitted on the SLD or IOM-2 interface for verification

BIT	7	6	5	4	3	2	1	0
	AD	R/W	CODE					

AD Address information
AD = 0 channel A is addressed with this command
AD = 1 channel B is addressed with this command

R/W Read/write information
This bit indicates whether filter coefficients are written to the SICOFI-2 or read from the SICOFI-2.
R/W = 0 Write to SICOFI-2
R/W = 1 Read from SICOFI-2

CODE		
0 0 0 0 1 1	B-Filter coefficients part 1	(followed by 8 bytes of data)
0 0 1 0 1 1	B-Filter coefficients part 2	(followed by 8 bytes of data)
0 1 0 0 1 1	Z-Filter coefficients	(followed by 8 bytes of data)
0 1 1 0 0 0	B-Filter delay coefficients	(followed by 4 bytes of data)
1 0 0 0 1 1	X-Filter coefficients	(followed by 8 bytes of data)
1 0 1 0 1 1	R-Filter coefficients	(followed by 8 bytes of data)
1 1 0 0 0 0	GX-Filter coefficients	(followed by 4 bytes of data)*)
1 1 1 0 1 0	GR-Filter coefficients	(followed by 2 bytes of data)*)

All other codes are reserved for future use.

*) In the range of 0 to 8 dB (0 to – 8 dB) gain adjustment is possible in steps ≤ 0.25 dB

SLIC Interface

The connection between SICOFI-2 and a SLIC is performed by the SICOFI-2 signaling and command/indication pins.
In SLD interface mode, the receive signaling byte is transferred to the signaling output pins. Data present at signaling input pins are transferred to the transmit signaling byte. Operating the SICOFI-2 with IOM-2 interface, data received from the downstream C/I byte are transferred to command output pins (C, C/I). Data on input pins (I, C/I) are transferred to the upstream C/I-byte.

SLD Interface Signaling Byte

The SICOFI-2 offers a 7 pin parallel signaling interface per channel.

Channel A:	SI1A, SI2A, SI3A	signaling input pins
	SO1A, SO2A, SO3A	signaling output pins
	SBA	programmable bidirectional signaling pin.
Channel B:	SI1B, SI2B, SI3B	signaling input pins
	SO1B, SO2B, SO3B	signaling output pins
	SBB	programmable bidirectional signaling pin.

Data present at SI1A ... SI3B and SBA, SBB (if programmed as input) are sampled and transferred to the SLD bus. Data received from the SLD bus are latched and fed to SO1A ... SO3B and SBA, SBB (if programmed as output).

Signaling byte format in receive direction:

BIT	7	6	5	4	3	2	1	0
	SBB[1)]	SO3B	SO2B	SO1B	SBA[1)]	SO3A	SO2A	SO1A

Signaling byte format in transmit direction:

BIT	7	6	5	4	3	2	1	0
	SBB[2)]	SI3B	SI2B	SI1B	SBA[2)]	SI3A	SI2A	SI1A

1) Don’t care, if pin programmed as input (**see CR1**).
2) ’0’, if pin programmed as output (**see CR1**).

The four possible cases of the signaling byte format are listed below.

Case	**Receive Signaling Byte**							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1	SBB	SO3B	SO2B	SO1B	SBA	SO3A	SO2A	SO1A
2	X	SO3B	SO2B	SO1B	SBA	SO3A	SO2A	SO1A
3	SBB	SO3B	SO2B	SO1B	X	SO3A	SO2A	SO1A
4	X	SO3B	SO2B	SO1B	X	SO3A	SO2A	SO1A

X ... don't care

Case	**Transmit Signaling Byte**							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1	0	SI3B	SI2B	SI1B	0	SI3A	SI2A	SI1A
2	SBB	SI3B	SI2B	SI1B	0	SI3A	SI2A	SI1A
3	0	SI3B	SI2B	SI1B	SBA	SI3A	SI2A	SI1A
4	SBB	SI3B	SI2B	SI1B	SBA	SI3A	SI2A	SI1A

Case 1: SBA and SBB are programmed as signaling outputs
Case 2: SBA is programmed as output, SBB is programmed as signaling input
Case 3: SBB is programmed as output, SBA is programmed as signaling input
Case 4: SBA and SBB are programmed as signaling inputs

IOM®-2 Interface Command/Indication Byte

The SICOFI-2 offers a 11 pin parallel command/indication SLIC interface

Indication input pins:	I1A	(associated with channel A)
	I1B	(associated with channel B)
Command output pins:	C1A, C2A	(associated with channel A)
	C1B, C2B	(associated with channel B)
	C3A	
Programmable command/indication pins:	CI1A, CI2A	(associated with channel A)
	CI1B, CI2B	(associated with channel B)

Data present at I1A, I1B and CI1A ... CI2B (if programmed as input) are sampled and transferred upstream. Data received downstream from IOM-2 interface are latched and fed to C1A ... C2B and CI1A ... CI2B (if programmed as output).

Data-downstream C/I channel byte format (receive):

BIT	6	5	4	3	2	1
	ADR	C3A[2]	CI2A/B[1]	CI1A/B[1]	C2A/B	C1A/B

In data-downstream direction, the 6 bit C/I field is split into an address bit and a 5 bit data-word. Depending on the ADR bit, data are transmitted to pins associated to channel A or channel B, and to pin C3A in either case.

Data-upstream C/I channel byte format (transmit):

BIT	6	5	4	3	2	1
	CI2B[3]	CI1B[3]	I1B	CI2A[3]	CI1A[3]	I1A

In data-upstream direction, the 6 bit C/I field is partioned in two 3 bit fields. The three bits C/I 1 ... 3 and 4 ... 6 contain the command/indication data associated with an analogue channel.

Typical examples for the C/I byte are listed below.

Case	Data-Downstream (Receive) Byte					
	6	**5**	**4**	**3**	**2**	**1**
1	ADR	C3A	CI2A/B[4]	CI1A/B[4]	C2A/B[4]	C1A/B[4]
2	ADR	C3A	CI2A/B[4]	X	C2A/B[4]	C1A/B[4]
3	ADR	C3A	X	CI1A/B[4]	C2A/B[4]	C1A/B[4]
4	ADR	C3A	X	X	C2A/B[4]	C1A/B[4]

X ... don't care

Case	Data-Upstream (Transmit) Byte					
	6	**5**	**4**	**3**	**2**	**1**
1	1	1	I1B	1	1	I1A
2	1	CI1B	I1B	1	CI1A	I1A
3	CI2B	1	I1B	CI2A	1	I1A
4	CI2B	CI1B	I1B	CI2A	CI1A	I1A

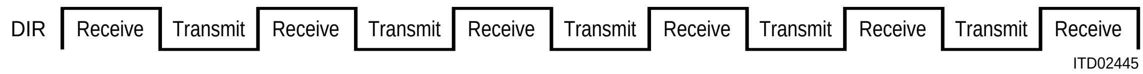
Case 1: CI2A/B and CI1A/B are programmed as command outputs
Case 2: CI2A/B is programmed as output, CI1A/B is programmed as indication input
Case 3: CI2A/B is programmed as input, CI1A/B is programmed as command output
Case 4: CI2A/B and CI1A/B are programmed as indication inputs

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[1] Don't care, if pin programmed as input (**see CR2**)
[2] Don't care, if pin C3A is programmed as detector select output (**see CR1**)
[3] '0', if pin programmed as output (**see CR2**)
[4] A for ADR = 0, B for ADR = 1

SLD Interface Programming Procedure

The following table shows typical control byte sequences. If the SICOFI-2 has to be configured completely during initialization, up to 60 bytes will be transferred.



DIR

No Operation

	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP

SOP Write

LSEL = 00	SOP	NOP								
LSEL = 11	SOP	NOP	CR1	NOP						
LSEL = 10	SOP	NOP	CR2	NOP	CR1	NOP				
LSEL = 01	SOP	NOP	CR3	NOP	CR2	NOP	CR1	NOP		

SOP Read

LSEL = 00	SOP	NOP								
LSEL = 11	SOP	CR1								
LSEL = 10	SOP	CR2	X	CR1						
LSEL = 01	SOP	CR3	X	CR2	X	CR1				

COP Write

4 Bytes	COP	NOP	DB4	NOP	DB3	NOP	DB2	NOP	DB1	NOP
8 Bytes	COP	NOP	DB8	NOP	DB7			NOP	DB1	NOP

COP Read

4 Bytes	COP	DB4	X	DB3		DB1	X	CR2	X	CR1
8 Bytes	COP	DB8	X	DB7		DB1	X	CR2	X	CR1

DB1 ... DB8 coefficient data byte 1 ... 8
X don’t care

IOM®-2 Interface Programming Procedure

Example for a typical IOM-2 interface programming procedure, consisting of identification request and answer, a SOP write command with four byte following, and SOP read to verify the programming.

Frame	Data Down		Data Up	
	Monitor	MR/MX	Monitor	MR/MX
1	11111111	11	11111111	11
2	IDRQT.1st byte	10	11111111	11
3	IDRQT.1st byte	10	11111111	01
4	IDRQT.2nd byte	11	11111111	01
5	IDRQT.2nd byte	10	11111111	11
6	11111111	11	11111111	01
7	11111111	11	IDANS.1st byte	10
8	11111111	01	IDANS.1st byte	10
9	11111111	01	IDANS.2nd byte	11
10	11111111	11	IDANS.2nd byte	10
11	11111111	01	11111111	11
12	Address	10	11111111	11
13	Address	10	11111111	01
14	SOP Write	11	11111111	01
15	SOP Write	10	11111111	11
16	CR4	11	11111111	01
17	CR4	10	11111111	11
18	CR3	11	11111111	01
19	CR3	10	11111111	11
20	CR2	11	11111111	01
21	CR2	10	11111111	11
22	CR1	11	11111111	01
23	CR1	10	11111111	11
24	SOP Read	11	11111111	01
25	SOP Read	10	11111111	11
26	11111111	11	11111111	01
27	11111111	11	Address	10
28	11111111	01	Address	10
29	11111111	01	CR4	11
30	11111111	11	CR4	10
31	11111111	01	CR3	11
32	11111111	11	CR3	10
33	11111111	01	CR2	11
34	11111111	11	CR2	10
35	11111111	01	CR1	11
36	11111111	11	CR1	10
37	11111111	01	11111111	11

IDRQT ... identification request (80_H, 00_H)
IDANS ... answer to identification request (80_H, 80_H)
Address ... SICOFI-2 specific address byte (81_H)
CRx ... Data for/of configuration register x.

Operating Modes

Basic Setting Mode

Upon initial application of V_{DD} or resetting pin RS to ’1’ during operation, or by software-reset (**see SOP Command**), the SICOFI-2 enters a basic setting mode. Basic setting means, that the SICOFI-2 configuration registers CR1 ... CR4 are initialized to ’0’ for both channel A and B.

All programmable filters are disabled, A-law is chosen, all programmable signaling or command/indication pins are inputs. Analog gains are set to 0 dB amplification or attenuation respectively. The two tone-generators as well as any testmodes are disabled. There is no persistance checking and pin C3A is programmed command output if IOM-2 mode is selected.

Receive signaling registers are cleared. SIP/DU is in high impedance state, the two analog outputs VOUTA and VOUTB and the receive signaling outputs are forced to ground.

The serial SLD or IOM-2 interface is ready to receive commands, starting with the next 8 kHz frame. In SLD interface mode the serial interface port SIP remains in high impedance state, until reception of a valid SOP or COP command.

If any voltage is applied to any input-pin before initial application of V_{DD}, the SICOFI-2 may not enter the basic setting mode. In this case it is necessary to reset the SICOFI-2 or to initialize the SICOFI-2 configuration registers to ’0’.

Standby Mode

The SICOFI-2 is forced to standby mode with a power-down command by the 1st SOP-byte. Both channels A and B must be programmed separately. During standby mode the serial SICOFI-2 interface is ready to receive and transmit commands and data.

Operating Mode

The operating mode for any of the two channels is entered upon recognition of a power-up bit ’1’ in a SOP command for the specific channel.

Transmission Characteristics

The target figures in this specification are based on the subscriber-line board requirements. The proper adjustment of the programmable filters (transhybrid balancing, impedance matching, frequency-response correction) needs a complete knowledge of the SICOFI-2's analog environment. Unless otherwise stated, the transmission characteristics are guaranteed within the test condition below.

T_A = 0 to 70 °C (PEB 2260); T_A = -40 to 85 °C (PEF 2260); V_{DD} = 5 V ± 5 %;
V_{SS} = – 5 V ± 5 %; GNDA = GNDB = GNDD = 0 V
R_L > 10 kΩ; C_L < 50 pF; H(Z) = H(B) = 0; H(X) = H(R) = 1;
GX = 0 to 8 dB; GR = 0 to – 8 dB;
AGX = 0, 6.00, 11.95, 13.90 dB; AGR = 0, – 6.00, – 11.95, – 13.90 dB;
f= 1000 Hz; 0 dBm0; A-law or µ-law;

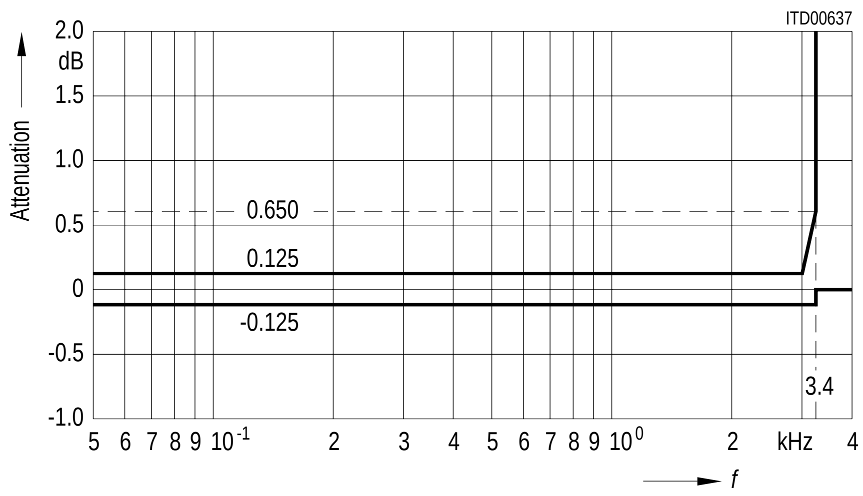
A 0 dBm0 signal is equivalent to 1.5763 [1.5710] Vrms. A 3.14 [3.17] dBm0 signal is equivalent to 2.263 Vrms which corresponds to the overload point of 3.2 V (A-law, [µ-law]).

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Gain (either value)[1)] Gain absolute (AGR = AGX = 0) T_A = 25 °C, V_{DD} = 5 V, V_{SS} = – 5 V T_A = 0 – 70 °C, V_{DD} = 5 V ± 5%, V_{SS} = – 5 V ± 5%	 G	 – 0.20 – 0.30	 ± 0.06	 0.20 0.30	 dB dB
Gain absolute (AGR = 0 to 13.9o dB, AGX = 0 to 13.90 dB) T_A = 0 – 70 °C, V_{DD} = 5 V ± 5%, V_{SS} = – 5 V ± 5%	G	– 0.40		0.40	dB
Total harmonic distortion, 0 dBm0, f= 1000 Hz; 2nd, 3rd order	THD		– 50	– 44	dB
Intermodulation 2f1 – f2[2)] 2f1 – f2[3)]	IMD			– 42 – 56	dB dB
Crosstalk 0 dBm0, f= 300 Hz to 3400 Hz Transmit to receive Receive to transmit	 CT_{XR} CT_{RX}		 – 85 – 85	 – 80 – 80	 dB dB
Idle channel noise, transmit, A-law, psophometric V_{IN} = 0 V transmit, µ-law, C-message V_{IN} = 0 V receive, A-law, psophometric idle code + 0 receive, µ-law, C-message idle code + 0	 N_{TP} N_{TC} N_{RP} N_{RC}		 – 85 5	 – 67.4 17.5 – 78.0 12.0	 dBm0p dBrnc dBm0p dBrnc

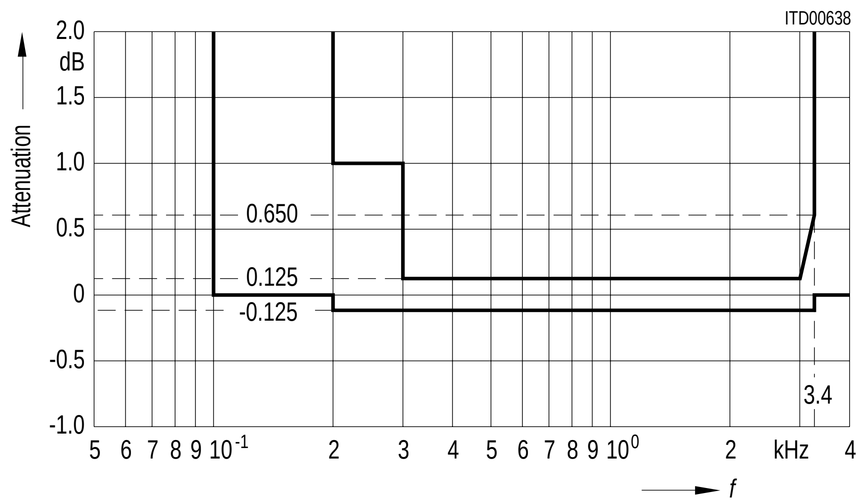
1) R_L = 300 Ω causes an additional attenuation in the range between – 0.1 to 0 dB.
2) Equal input levels in the range between – 4 dBm0 and – 21 dBm0; different frequencies in the range between 300 Hz and 3400 Hz.
3) Input level – 9 dBm0, frequency range 300 Hz to 3400 Hz and – 23 dBm0, 50 Hz.

Attenuation Distortion

Attenuation deviations stay within the limits in the figures below.



Receive: Reference frequency 1 kHz, input signal level 0 dBm0



Transmit: Reference frequency 1 kHz, input signal level 0 dBm0

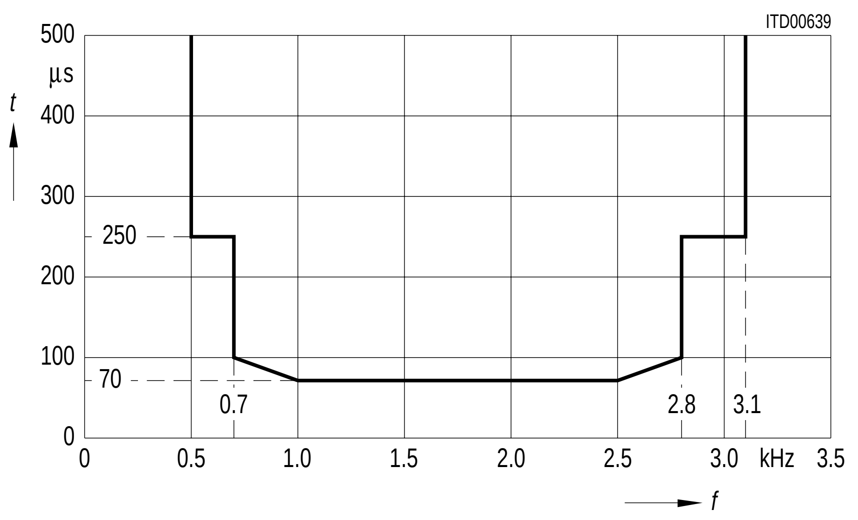
Group Delay

Maximum delays for operating the SICOFI-2 with H(B) = H(Z) = 0 and H(R) = H(X) = 1 including delay through A/D- and D/A converters. Specific filter programming may cause additional group delays.

Group delay deviations stay within the limits in the figures below.

Group Delay Absolute Values: Input signal level 0 dBm0

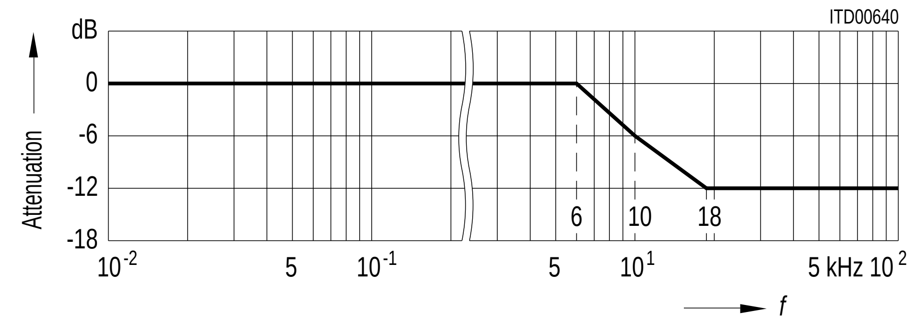
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Transmit Delay	D_{XA}			300	µs	f= 1.4 kHz
Receive Delay	D_{RA}			240	µs	f= 300 Hz

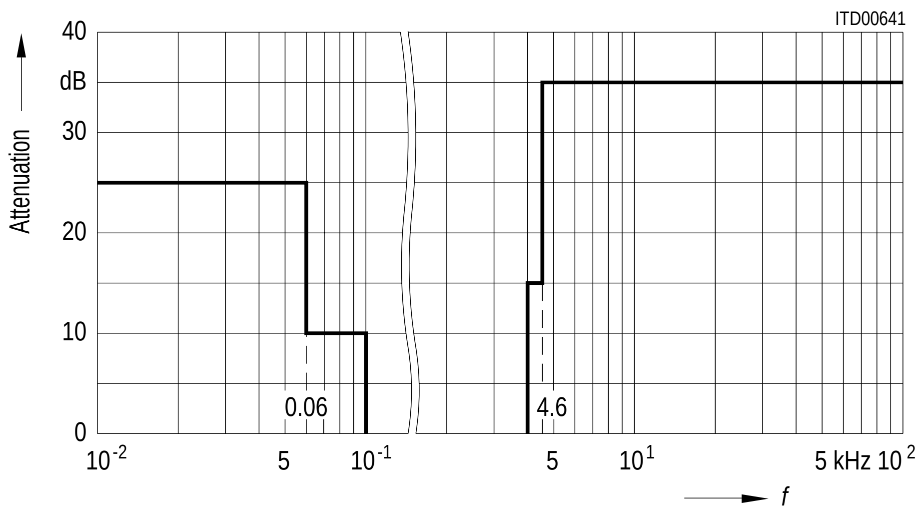


Group Delay Distortion: Input signal level 0 dBm0, reference frequency = 1.4 kHz

Out-of-Band Signals at Analog Input

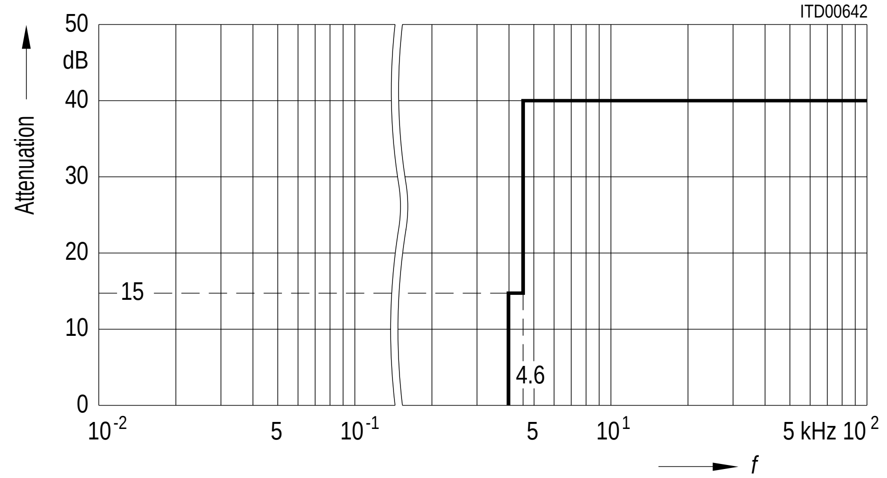
With an out-of-band sine wave signal with frequency *f* and level A applied to the analog input, the level of any resulting frequency component at the digital output will stay at least X dB below level A.





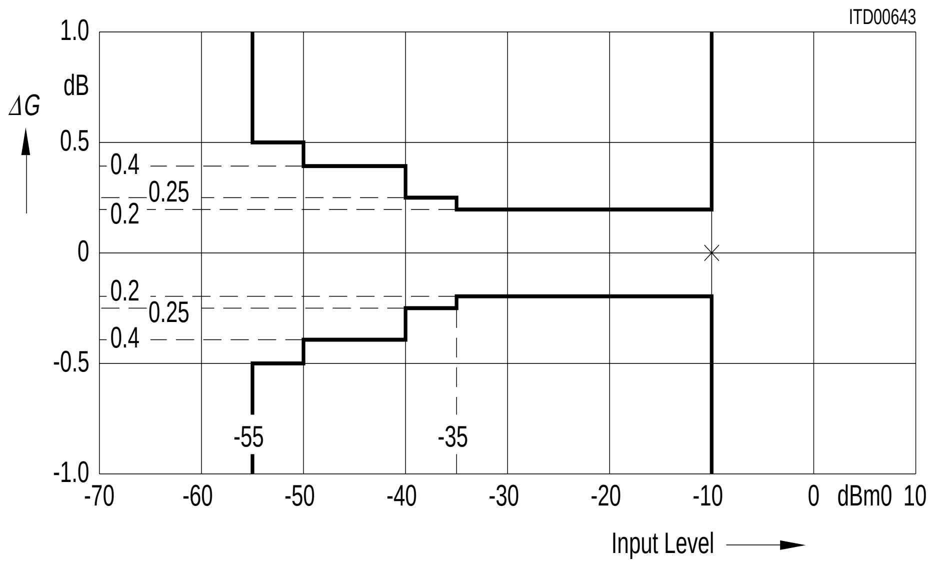
Out-of-Band Signals at Analog Output

With a 0 dBm0 sine wave of frequency *f* applied to the digital input, the level of any resulting out-of-band signal at the analog output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog output.

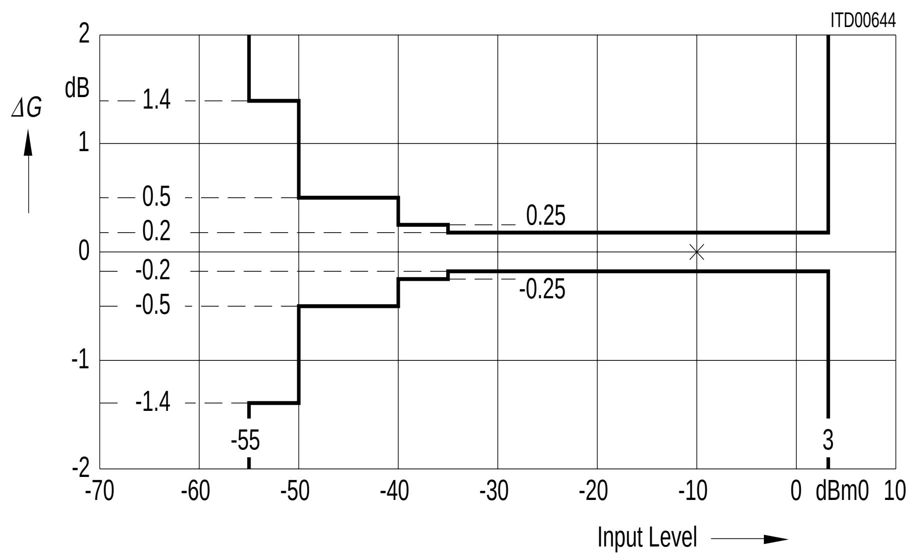


Gain Tracking (Receive and Transmit)

The gain deviations stay within the limits in the figures below



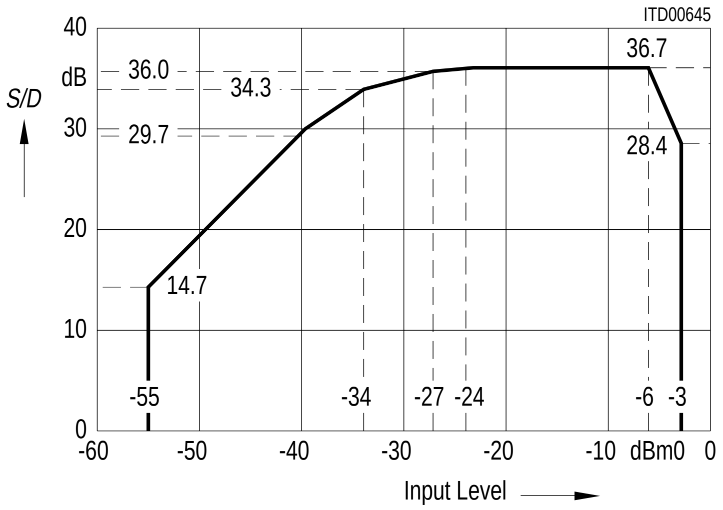
Gain Tracking: Measured with noise signal according to CCITT recommendations, reference level is – 10 dBm0, AGX = AGR = 0



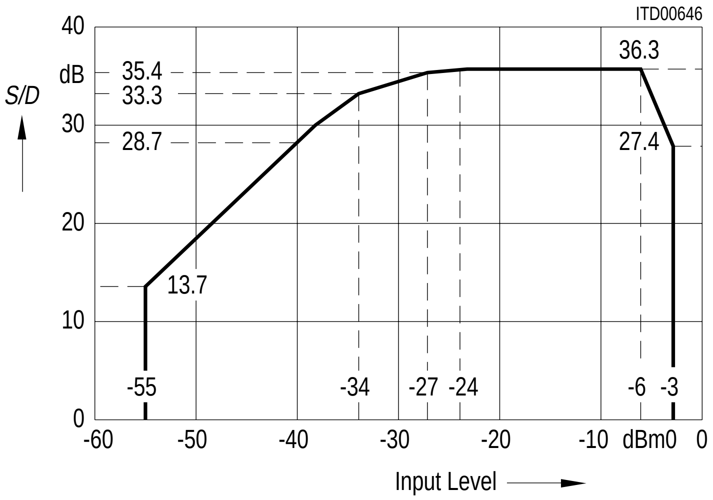
Gain Tracking: Measured with sine wave in the range 700 to 1100 Hz, reference level is – 10 dBm0, AGX = AGR = 0

Total Distortion

The signal-to-distortion ratio exceeds the limits in the following figures.

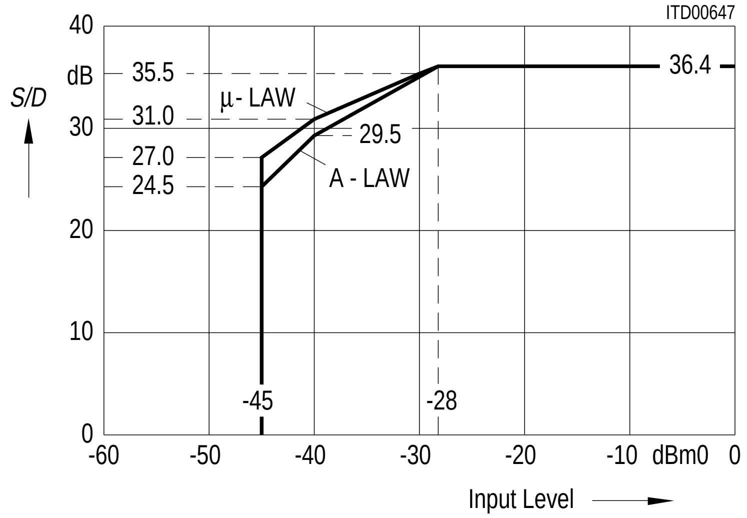


Receive: Measured with noise signal according to CCITT recommendations



Transmit: Measured with noise signal according to CCITT recommendations

The signal to distortion ratio exceeds the limits in the following figure.



Receive & Transmit: Measured with sine wave in the range 700 to 1100 Hz excluding submultiples of 8 kHz

Parameter				Total Distortion	
		Input Level	**Unit**	**min.**	**Unit**
Digital loop	back via B-filter or digital loop back via analog port	0 – 30 – 40 – 45	dBm0 dBm0 dBm0 dBm0	31 31 25 20	dB dB dB dB

Transhybrid Loss

The quality of transhybrid-balancing is very sensitive to deviations in gain and group delay – deviations inherent to the SICOFI-2 A/D- and D/A-converters as well as to all external components used on a line card (SLIC, OP's etc.)

The SICOFI-2 transhybrid loss is measured the following way: A sine wave signal with level 0 dBm0 and a frequency in the range of 300 – 3400 Hz is applied to the digital input. The resulting analog output signal at pin VOUT is directly connected to VIN, e.g. with the SICOFI-2 testmode "Digital Loop Back via Analog Port" (**see CR3**). The programmable filters R, GR, X, GX and Z are disabled, the balancing filter B is enabled with coefficients optimized for this configuration (VOUT = VIN).

The resulting echo measured at the digital output is at least X dB below the level of the digital input signal as shown in the table below.

B-filter coefficients recommended for transhybrid loss measurement with VOUT = VIN

	COP-Write	Coefficients							
B-filter part 1	(03)/(83)	FD	29	FB	38	A1	A0	3C	42
B-filter part 2	(0B)/(8B)	00	AF	62	2B	CF	D1	CA	A4
B-filter delay	(18)/(98)	19	19	11	19				

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	typ.		
Transhybrid loss at 500 Hz Transhybrid loss at 2500 Hz Transhybrid loss at 3000 Hz	THL_{500} THL_{2500} THL_{3000}	33 29 27	45 40 35	dB dB dB	T_A = 25 °C; V_{DD} = 5 V, V_{SS} = – 5 V; AGR = AGX = 0 dB
Transhybrid loss at 500 Hz Transhybrid loss at 2500 Hz Transhybrid loss at 3000 Hz	THL_{500} THL_{2500} THL_{3000}	29 27 25	40 35 30	dB dB dB	T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %; V_{SS} = – 5 V ± 5 %; AGR = AGX = 0 dB
Transhybrid loss at 500 Hz Transhybrid loss at 2500 Hz Transhybrid loss at 3000 Hz	THL_{500} THL_{2500} THL_{3000}	27 25 23	40 35 30	dB dB dB	T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %; V_{SS} = – 5 V ± 5 %; AGR = AGX = 6.03, 12.06, 14.00 dB
Transhybrid loss at 500 Hz Transhybrid loss at 2500 Hz Transhybrid loss at 3000 Hz	THL_{500} THL_{2500} THL_{3000}	29 17 15	40 25 20	dB dB dB	T_A = 0 to 85 °C; V_{DD} = 5 V ± 5 %; V_{SS} = – 5 V ± 5 %; AGR = AGX = 0 dB
Transhybrid loss at 500 Hz Transhybrid loss at 2500 Hz Transhybrid loss at 3000 Hz	THL_{500} THL_{2500} THL_{3000}	27 15 13	40 25 20	dB dB dB	T_A = 0 to 85 °C; V_{DD} = 5 V ± 5 %; V_{SS} = – 5 V ± 5 %; AGR = AGX = 6.03,12.06, 14.00 dB

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
V_{DD} referred to GNDD		– 0.3	5.5	V
V_{SS} referred to GNDD		– 5.5	0.3	V
GNDA to GNDD		– 0.6	0.6	V
Analog input and output voltage referred to V_{DD} = 5 V; V_{SS} = – 5 V referred to V_{SS} = – 5 V; V_{DD} = 5 V	 V_{IN} V_{IN}	 – 10.3 – 0.3	 0.3 10.3	 V V
All digital input voltages referred to GNDD = 0 V; V_{DD} = 5 V referred to V_{DD} = 5 V; GNDD = 0 V	 V_{IN} V_{IN}	 – 0.3 – 5.3	 5.3 0.3	 V V
DC input and output current at any input or output pin	I_{DC}		10	mA
Storage temperature	T_{stg}	– 60	125	°C
Ambient temperature under bias	T_A	– 10	80	°C
Power dissipation	P_D		1	W

Operating Range

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %; V_{SS} = – 5 V ± 5 %; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
V_{DD} supply current standby operating	I_{DD}		 0.5 22	 0.8 28	 mA mA	
V_{SS} supply current standby operating	I_{SS}		 0.05 12	 0.08 18	 mA mA	
Power supply rejection (of either supply/direction)	$PSRR$	30			dB	1 kHz 80 mVrms ripple
Power dissipation standby Power dissipation operating Power dissipation operating	P_{Ds} P_{Do1} P_{Do2}		2.75 110 170	4.4 150 230	mW mW mW	 1 channel 2 channels

T_A = 0 to 85 °C; V_{DD} = 5 V ± 5 %; V_{SS} = – 5 V ± 5 %; GNDD = 0 V; GNDA = 0 V

V_{DD} supply current standby operating	I_{DD}		 0.6/0.65 26/28	 0.95/1.1 34/37	 mA mA	 -25°C/-40°C -25°C/-40°C
V_{SS} supply current standby operating	I_{SS}		 0.06/0.065 14/16	 0.08 18	 mA mA	
Power supply rejection (of either supply/direction)	$PSRR$	30			dB	1 kHz 80 mVrms ripple
Power dissipation standby Power dissipation operating Power dissipation operating	P_{Ds} P_{Do1} P_{Do2}		3.3/3.6 132/143 200/220	5.2/6.1 180/195 280/305	mW mW mW	 1 channel 2 channels

Electrical Characteristics

Digital Interface

T_A = 0 to 70 °C (PEB 2260); T_A = -40 to 85 °C (PEF 2260); V_{DD} = 5 V ± 5 %;
V_{SS} = – 5 V ± 5 %; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
L-input voltage	V_{IL}	– 0.3	0.8	V	
H-input voltage	V_{IH}	2.0		V	
Negative-input voltage	V_{IN}	– 3.5		V	
L-output voltage	V_{OL}		0.45	V	I_0 = – 2 mA
H-output voltage	V_{OH}	2.4		V	I_0 = 400 µA
Input leakage current	I_{IL}		± 1	µA	– 0.3 ≤ V_{IN} ≤ V_{DD}

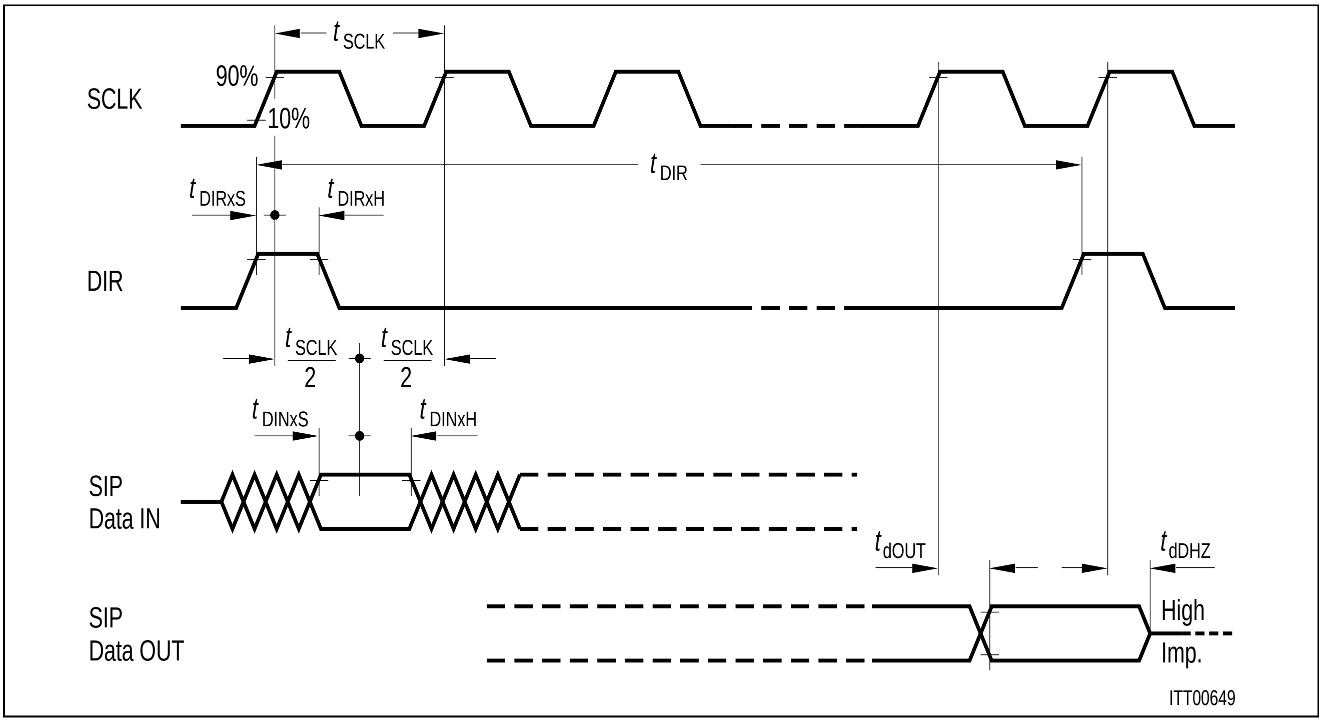
Analog Interface

T_A = 0 to 70 °C (PEB 2260); T_A = -40 to 85 °C (PEF 2260); V_{DD} = 5 V ± 5 %;
V_{SS} = – 5 V ± 5 %; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input resistance	R_I	10		MΩ	
Analog output resistance	R_O		10	Ω	
Input offset voltage	V_{IO}		± 50	mV	
Output offset voltage	V_{OO}		± 50	mV	
Input voltage range	V_{IR}		± 3.2	V	
Output voltage range	V_{OR}	± 3.1		V	R_L ≥ 300 Ω, C_L ≤ 50 pF

Reset Timing

To reset the SICOFI-2 to basic setting mode, positive pulses applied to pin RS have to be longer than 2 × t_{SCLK} for SLD Interface mode, or 2 × t_{DCL} for IOM-2 Interface mode. The SICOFI-2 is resetted, if a clock is applied at pin 21 (SCLK/DCL). Spikes shorter than t_{SCLK} (t_{-DCL}) will be ignored.

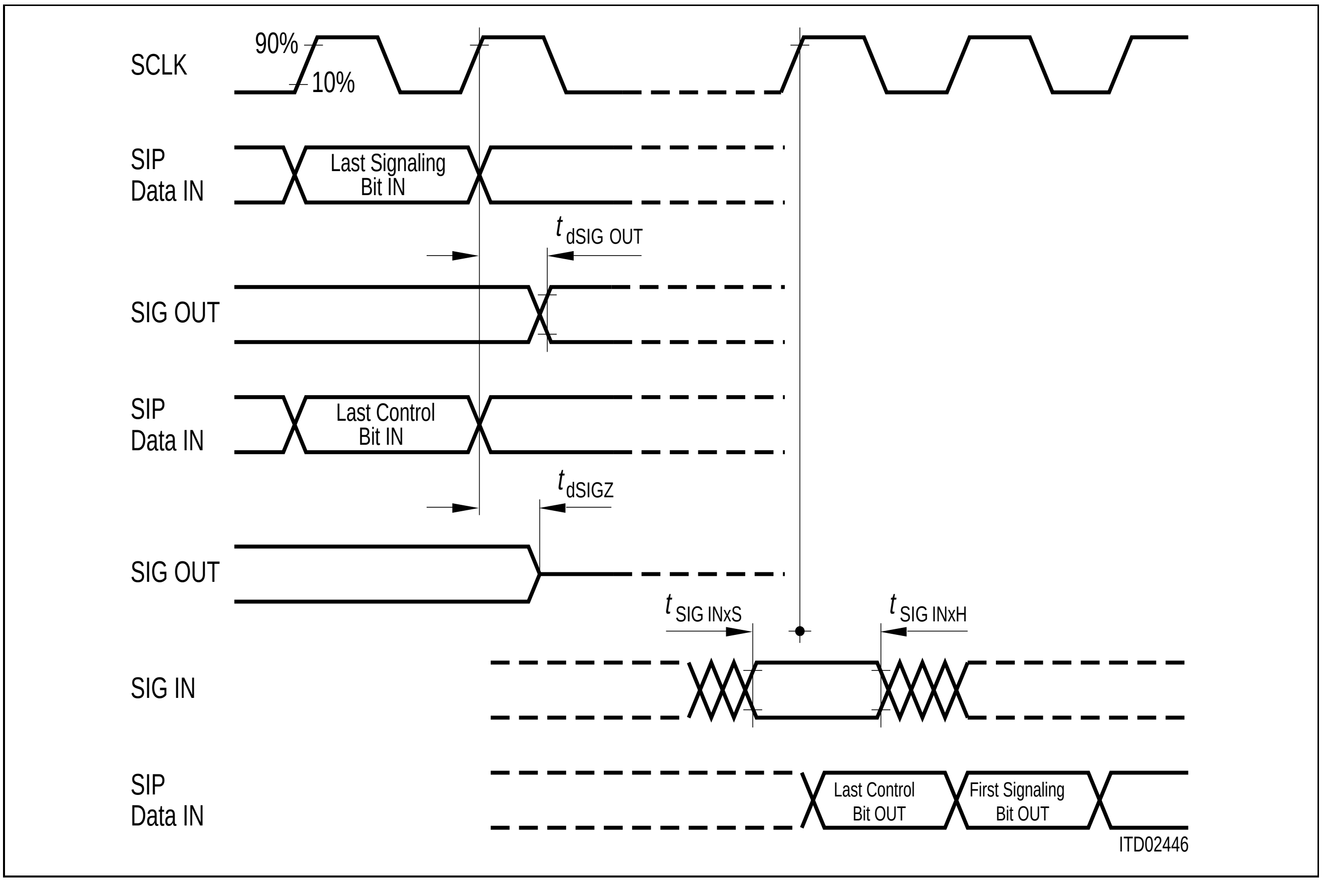


SIP Interface Timing (SLD)

Switching Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period SCLK*)	t_{SCLK}		1/512 kHz		
SCLK duty cycle		20	50	80	%
Period DIR*)	t_{DIR}		125		µs
DIR setup time	$t_{DIR \times S}$	40	t_{SCLKh}		ns
DIR hold time	$t_{DIR \times H}$	250			ns
SIP data in setup time	$t_{DIN \times S}$	20			ns
SIP data in hold time	$t_{DIN \times H}$	100			ns
SIP data out delay	t_{dDOUT}		150	250	ns
SIP data out high impedance delay	t_{dDHZ}		50	70	ns

*) $t_{DIR} = 64 \times t_{SCLK}$

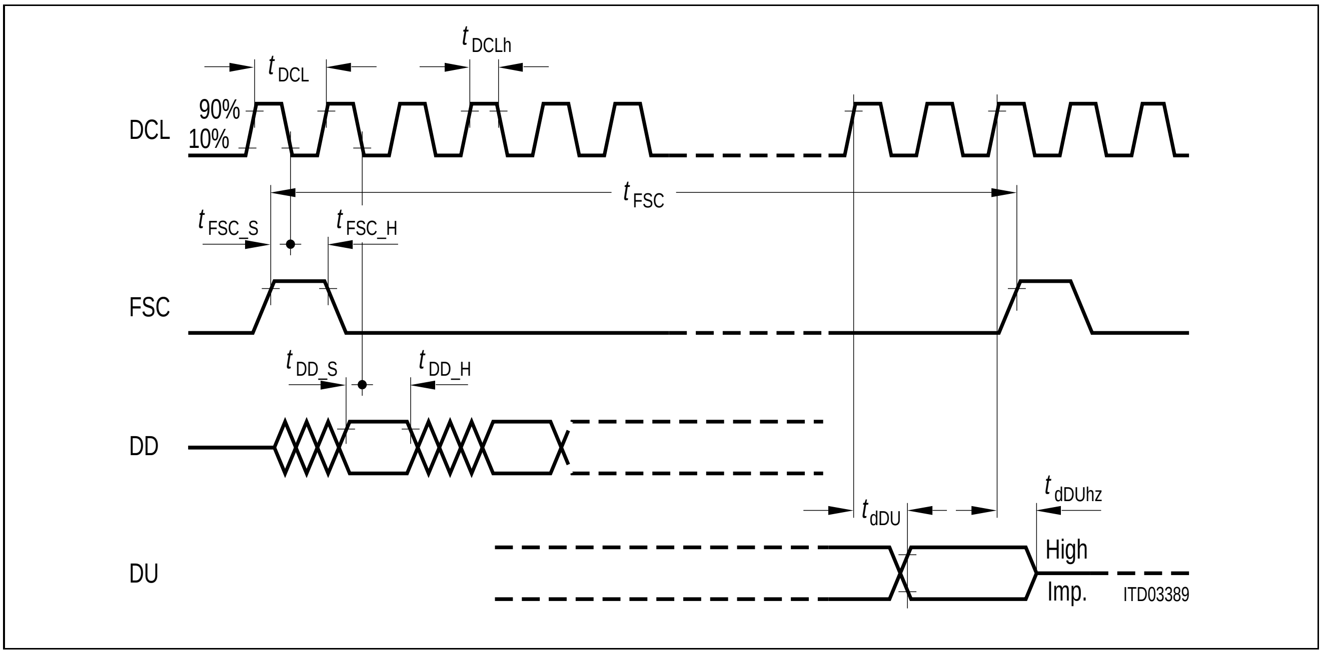


Signaling Interface Timing (SLD)

Switching Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Delay signaling out	$t_{dSIGOUT}$		250	350	ns
Delay signaling high impedance	t_{dSIGZ}		150	200	ns
Delay signaling active	t_{dSIGA}		150	200	ns
SIG in setup time	$t_{SIGIN \times S}$	50			ns
SIG in hold time	$t_{SIGIN \times H}$	100			ns

1) Pins SO1 … SO3; Pins SA … SD as output
2) Pins SI1 … SI3; Pins SA … SD as input
3) For programmable signaling pins SBA/SBB



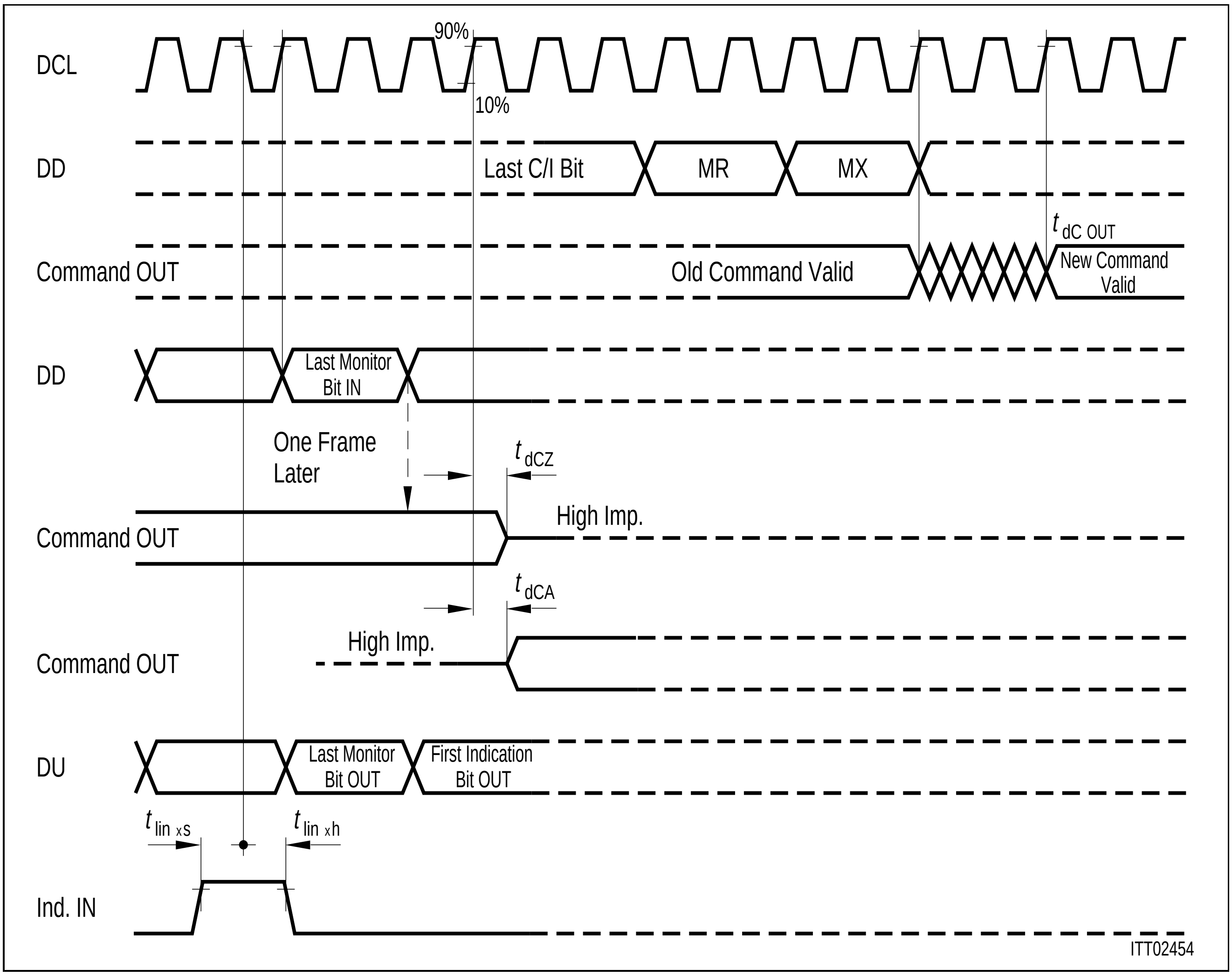
IOM®-2 Interface Timing

Switching Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period DCL 'slow' mode[1]	t_{DCL}		1/512 kHz		
Period DCL 'fast' mode[1]	t_{DCL}		1/4096 kHz		
DCL duty cycle		40		60	%
Period FSC[1]	t_{FSC}		125		µs
FSC setup time	$t_{FSC \times S}$	70	t_{DCLH}		ns
FSC hold time	$t_{FSC \times H}$	40			ns
DD data in setup time	$t_{DD \times S}$	20			ns
DD data in hold time	$t_{DD \times H}$	50			ns
DU data out delay	t_{dDU}		150[2]	250	ns

[1] IOM-2 interface mode, DCL = 512 kHz: $t_{FSC} = 64 \times t_{DCL}$
IOM-2 interface mode, DCL = 4096 kHz: $t_{FSC} = 512 \times t_{DCL}$

[2] Depending on pull up resistor (typical 10 kΩ)

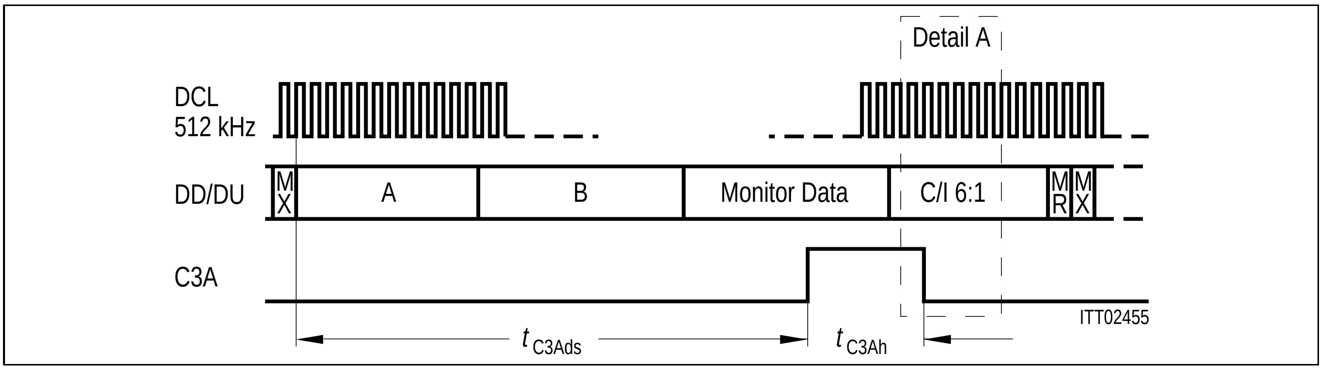


IOM®-2 Command/Indication Interface Timing

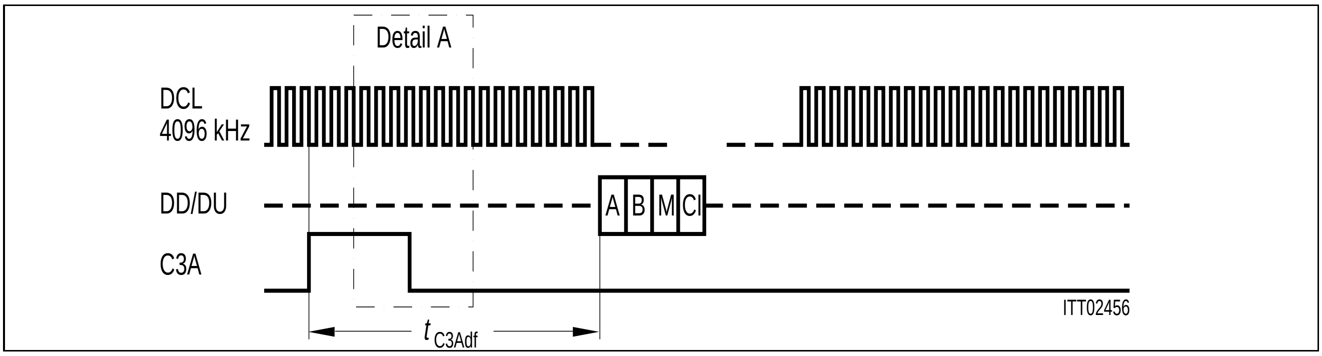
Switching Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Command out delay	t_{dCout}			0	ns
Command out high impedance	t_{dCZ}		150	200	ns
Command out active	t_{dCA}		150	200	ns
Indication in setup time	$t_{lin \times S}$	50			ns
Indication in hold time	$t_{lin \times H}$	100			ns

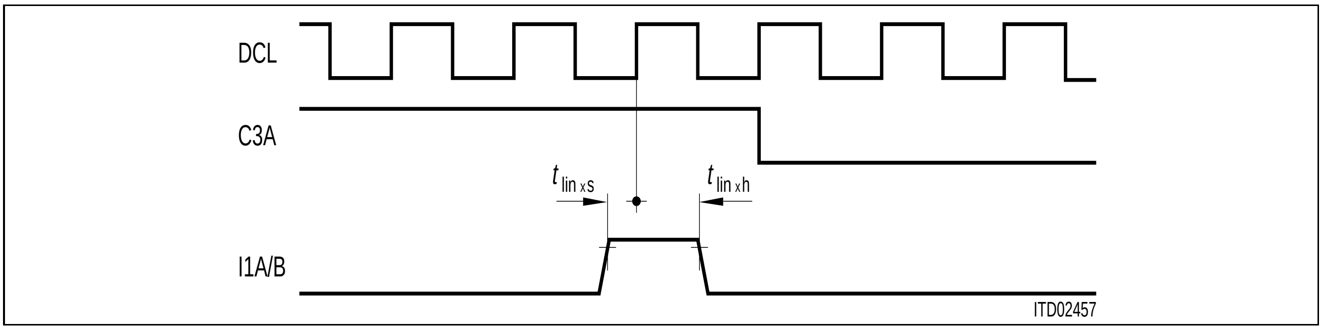
Detector Select Timing



IOM®-2 Interface, DCL = 512 kHz (one channel per frame)



IOM®-2 Interface, DCL = 4096 kHz (eight channels per frame)



Detail A

Switching Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Detector select high time	t_{C3Ah}		15.6		µs
Detector select delay, 'slow' mode	t_{C3Ads}		82.0		µs
Detector select delay, 'fast' mode	t_{C3Adf}		– 46.8		µs
Indication in setup time	$t_{lin \times s}$	50			ns
Indication in hold time	$t_{lin \times h}$	100			ns

Appendix A

On Chip Tone Generation

With bit TG2, TG1 in configuration register CR2 two tone generators per channel can be activated in receive direction; the R-filter output is set to ’0’ with any tone generator activated. Each tone generator frequency and amplitude is programmable individually via R-filter coefficients.

Every byte sequence is started with 2B/AB depending on the channel to be programmed

TG1		**TG2**		**Byte Sequence**							
				TG1-Coefficient				**TG2-Coefficient**			
F[HZ]	**Gain [dB]**	**F[HZ]**	**Gain [dB]**	**Frequency**			**Gain**	**Frequency**			**Gain**
2000	0	2000	0	01	11	11	01	01	11	11	01
1000	0	1000	0	01	11	12	01	01	11	12	01
800	0	800	0	AA	AA	A1	01	AA	AA	A1	01
697	0	770	0	B2	BA	12	01	D3	2C	A1	01
852	0	941	0	BC	13	B1	01	2B	BC	C1	01
1209	0	1336	0	F2	2B	21	01	FA	12	21	01
1477	0	1633	0	BC	1D	11	01	A5	C1	B0	01
2000	0	1000	0	01	11	11	01	01	11	12	01
1000	0	500	0	01	11	12	01	01	11	13	01
1000	– 2.5	500	+ 3.5	01	11	12	11	01	11	13	10
1000	– 6	500	+ 6	01	11	12	02	01	11	13	00
1000	– 5	500	+ 6	01	11	12	31	01	11	13	00
1000	– 4.1	500	+ 3.5	01	11	12	21	01	11	13	10
1000	– 2.5	500	1.9	01	11	12	11	01	11	13	20
1000	– 1.5	500	1	01	11	12	B0	01	11	13	30

Note: The generated tones are sinewaves with harmonic distortion < – 25 dB

Appendix B

IOM®-2 Interface MONITOR Transfer Protocol

The MONITOR channel is used for the transfer of maintenance information between two functional blocks. By use of two MONITOR control bits (MR and MX) per direction, the data are transferred in a complete handshake procedure.

The MR and MX bits in the fourth octet (the control channel) of the IOM-2 frame are used for the handling of the MONITOR channel.

- A pair of MR and MX in the inactive state for two or more consecutive frames indicates an idle state on the MONITOR channel and the end of message (EOM)
- A start of transmission is initiated by the transmitter with the transmission of the MX bit form the inactive state to the active state together with the first byte sent on the MONITOR channel. The receiver acknowledges the first byte by setting the MR bit in the other direction to active and keeping it active for at least one more frame.
- The same byte is sent continuously in each frame until either a new byte is transmitted, the end of message or an abort
- Flow control, in the form of transmission delay, can only take place when the transmitters MX and the receivers MR bit are in active state.
- Any false MX or MR bit received by the receiver or transmitter leads to a request for abort or abort, respectively.
- Since the receiver is able to receive the MONITOR data at least twice (in two consecutive frames), it is able to check for data errors. If two different bytes are received the receiver will wait for the receipt of two identical successive bytes (last look function).
- A collision resolution mechanism is implemented in the transmitter. This is done by looking for the idle phase of the MX-bit and making a per bit collision check on the transmitted MONITOR data.
- Any abort leads to a reset of the SICOFI-2 command stack, the device is ready to receive new commands.
- To obtain a maximum speed data transfer, the transmitter anticipates the falling edge of the receivers acknowledgement.
- Due to the inherent SLD-programming structure, duplex operation is not possible.

Identification Command

In order to be able to unambiguously identify different devices by software, a two byte identification command is defined for analog line IOM-2 devices.

1	0	0	0	0	0	0	0

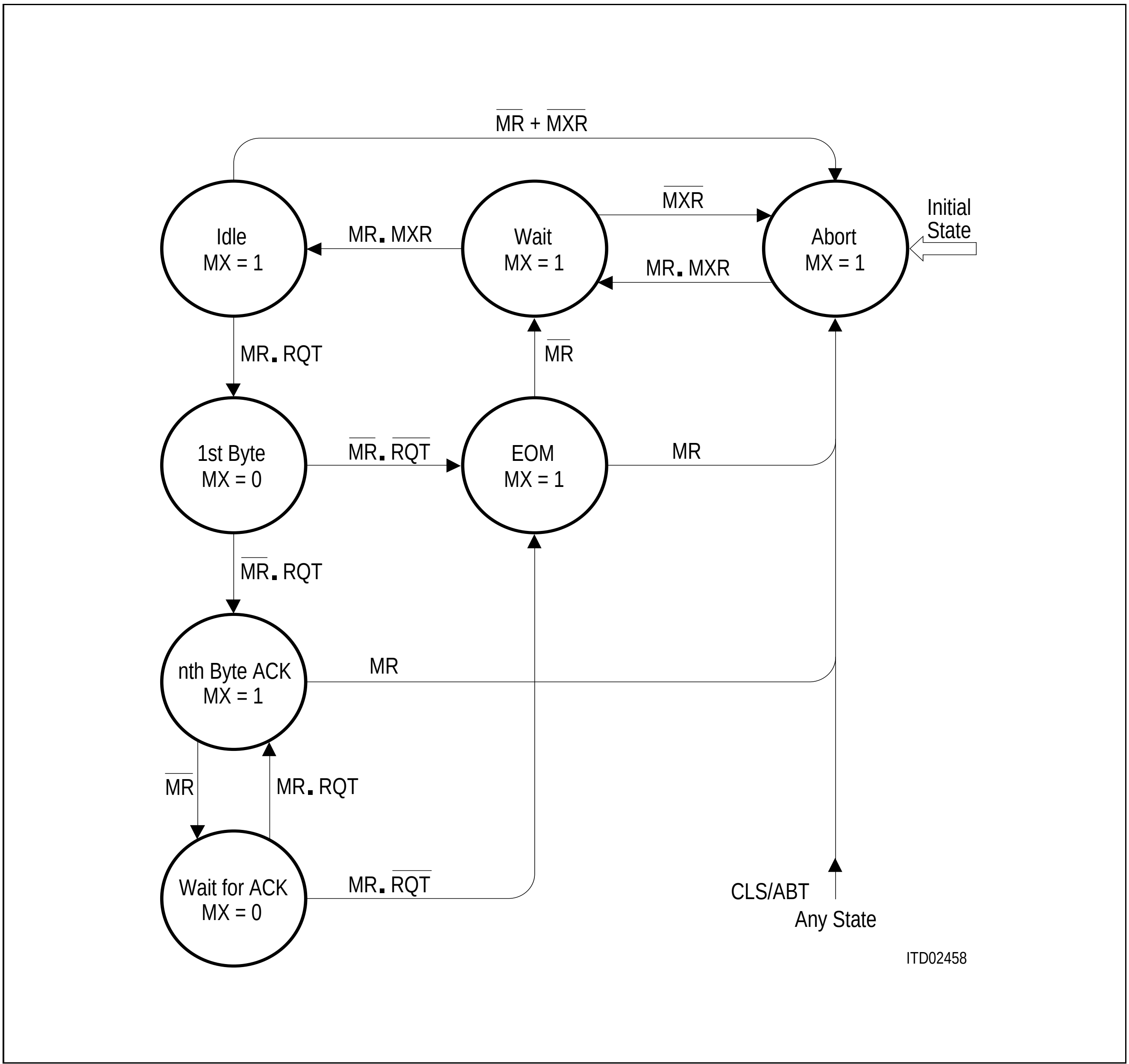
0	0	0	0	0	0	0	0

Each device will then respond with its specific identification code. For the SICOFI-2 this two byte identification code is:

1	0	0	0	0	0	0	0

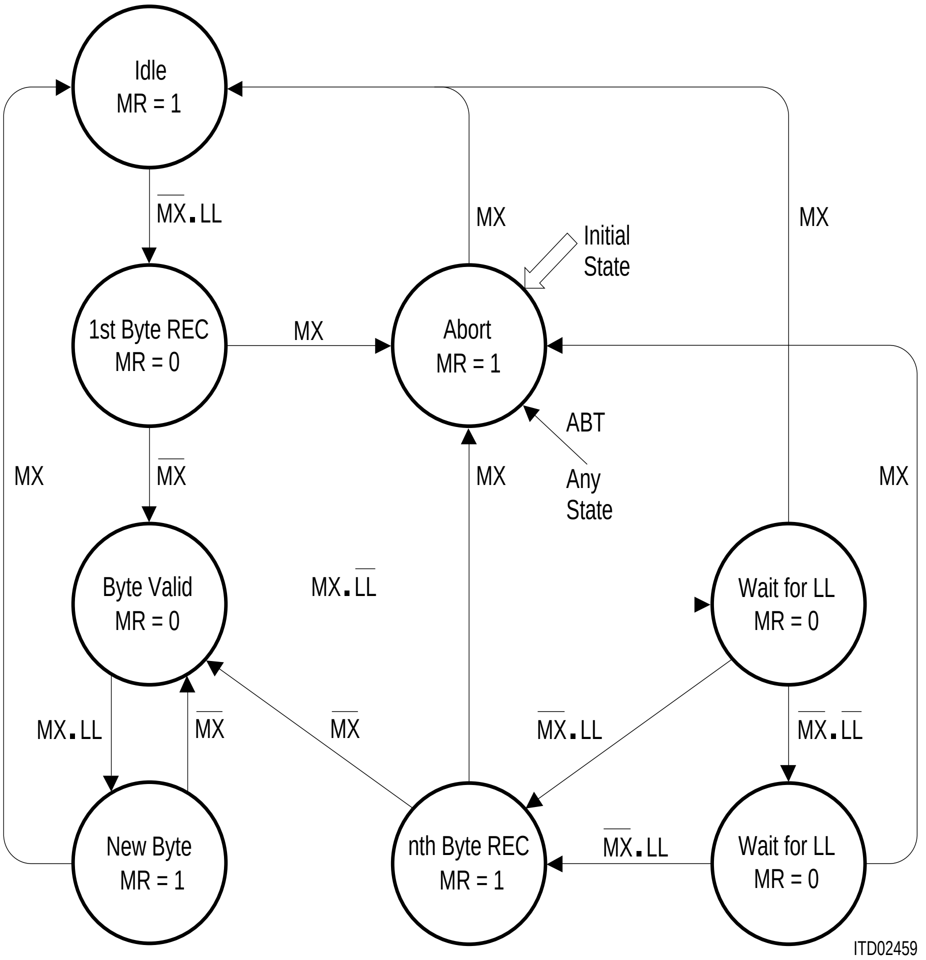
1	0	0	0	0	0	0	0

Each byte is transferred at least twice (in two consecutive frames).



State Diagram of the SICOFI®-2 MONITOR Transmitter

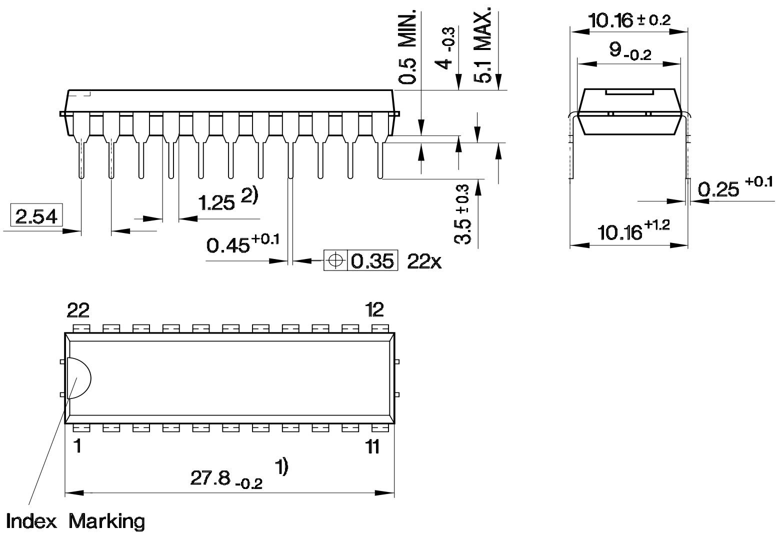
MR	...	MR-bit received
MX	...	MX-bit calculated and expected on DU-line
MXR	...	MX-bit sampled on DU-line
CLS	...	Collision within the MONITOR data byte
RQT	...	Request for transmission form internal source
ABT	...	Abort request/indication



State Diagram of the SICOFI®-2 MONITOR Receiver

MR	...	MR-bit transmitted on DU-line
MX	...	MX-bit received data downstream
LL	...	Last lock of MONITOR byte received
ABT	...	Abort indication to internal source

Plastic Dual-in-Line Package, P-DIP-22

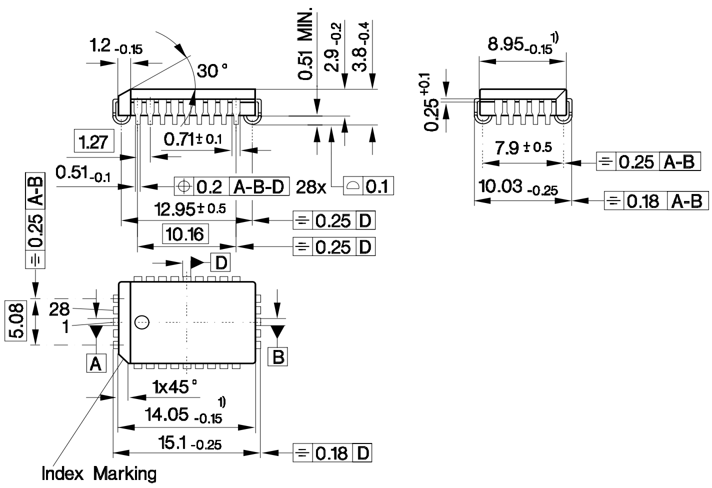


1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion of 0,15 max. per side

Approx. weight 2.1 g

SICOFI®

Plastic-Leaded Chip Carrier, P-LCC-28-R (SMD)



1) Does not include plastic or metal protrusion of 0.15 max. per side

Dimensions in mm

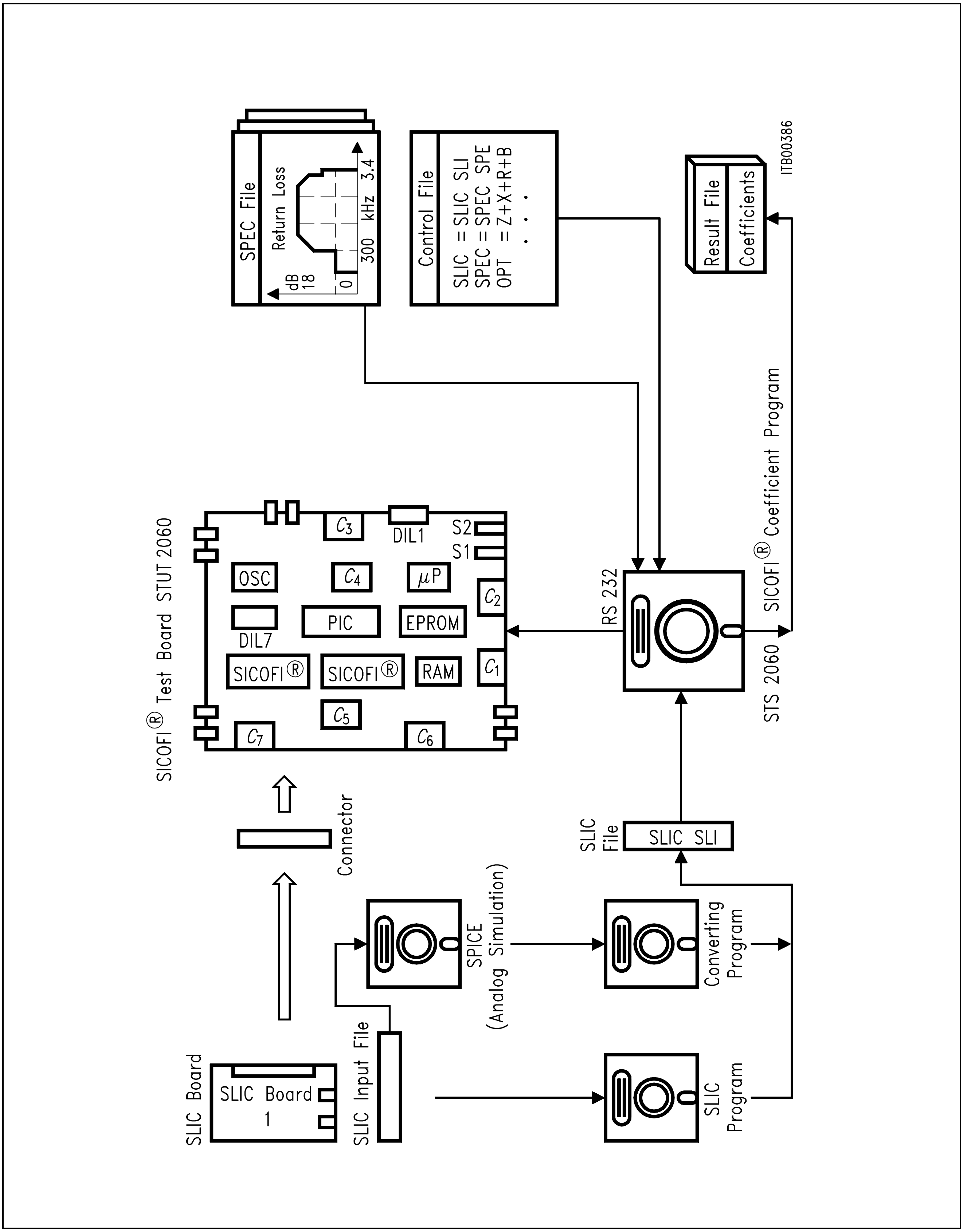
SICOFI®, SICOFI®-2

SMD = Surface Mounted Device

1 General Overview on Hardware / Software Tools

	Designation	Ordering Code	Software	Hardware
User Boards				
SICOFI Testboard	STUT 2060	Q67100-H6058	–	A
SICOFI-2 Module[1)]	SIPB 5135	Q67100-H6149	–	A
SLIC Boards				
HARRIS HC 5502/5504	STUS 5502	Q67100-H6175	A	A
HARRIS HC 5509	STUS 5509	Q67100-H6270	A	A
STM L3000 + L3030	STUS 3030	Q67100-H6178	A	A
STM L3000 + L3090	STUS 3090	Q67100-H6179	A	A
ERICSSON PBL 3762	STUS 3762	Q67100-H6180	A	A
ERICSSON PBL 3736	STUS 3736	Q67100-H6181	A	U
Transformer Series Feeding	STUS 1000	Q67100-H6176	A	U
Transformer Transverse Feeding	STUS 1001	Q67100-H6177	A	A
Software				
SICOFI Coefficient and Simulation Program for PEB 2060/PEB2260	STS 2060		A	–
Related Boards[1)]				
Main Board	SIPB 5000	Q67100-H8647	A[2)]	A
IOM-2 Line Card Module	SIPB 5121	Q67100-H8656	–	A
PCM4 Digital Adaptor	SIPB 5311	Q67100-H6126	–	A

1) for the ISDN PC Userboard System (SIPB)
2) Mainboard Firmware and Menu Software
A = available
U = under development


SPEC File
Return Loss
dB
18
0
300
kHz
3.4
Control File
SLIC = SLIC SLI
SPEC = SPEC SPE
OPT = Z+X+R+B
Result File
Coefficients
ITB00386
SICOFI® Test Board STUT 2060
OSC
C3
C4
DIL1
S2
S1
μP
C2
DIL7
PIC
EPROM
SICOFI®
SICOFI®
RAM
C1
C5
C7
C6
RS 232
SICOFI® Coefficient Program
STS 2060
Connector
SLIC File
SLIC SLI
SPICE (Analog Simulation)
Converting Program
SLIC Board
SLIC Board 1
SLIC Input File
SLIC Program

2 SICOFI® Coefficients Program (STS 2060)

2.1 Features

- Coefficients program available on floppy disk for PC AT or compatible
- Calculates the coefficients for all digital filters in SICOFI PEB 2060/PEB 2260 (Z, R, X, B, GR, GX)
- Menu driven program surface
- Graphic screen output for various SLIC/SICOFI transfer functions
- Direct programming of SICOFI testboard STUT 2060
- SLIC program parts for various standard SLICs included
- Analog simulation program for modelling new user specific SLICs included

2.2 General Overview

The high flexibility of the SICOFI is based on a variety of user programmable filters, which consist of analog gain adjustment AGR and AGX, digital gain adjustment GR and GX, frequency response adjustment R and X, impedance matching filter Z and the transhybrid balancing filter B.

To gain an optimum result within a given environment while observing existing prescriptions, Siemens offers to the SICOFI user the software packet STS 2060, which performs the calculation of the filter coefficients by using an overall optimizing approach.

Because of the modularity of the SICOFI software program, it is possible to use the SICOFI together with
– transformer SLICs with series or transverse feeding
– fixed electronic SLICs (Boards and SLIC program parts are available from Siemens Semiconductor)
– new user specific SLICs

The STS 2060 software runs on any IBM-AT compatible PC under MD-DOS Version 3.0 or later providing 640 Kbyte available RAM, a 1.2 Mbyte floppy disk drive, and the math coprocessor 80287 (optional).

The STS 2060 software consists of the two major sections: SLIC program (SLIC.EXE) and SICOFI program (SICOFI.BAT). A transfer file (SLIC.SLI) provides the interface between these two programs. Instead of SLIC.EXE it is possible to use a special analog simulation program (S.BAT) for modelling new user specific SLICs.

All the specific values concerning the SLIC and its external circuitry (physical data, filter dimensions, ...) are gathered in an input file SLIC.INP.

The SLIC program SLIC.EXE models the SLIC and its external circuitry in order to create a file SLIC.SLI which contains their transmission characteristics.

SLIC.SLI is a transfer file (output/input file) between the SLIC program and the SICOFI program to introduce the SLIC circuit data into the SICOFI program.

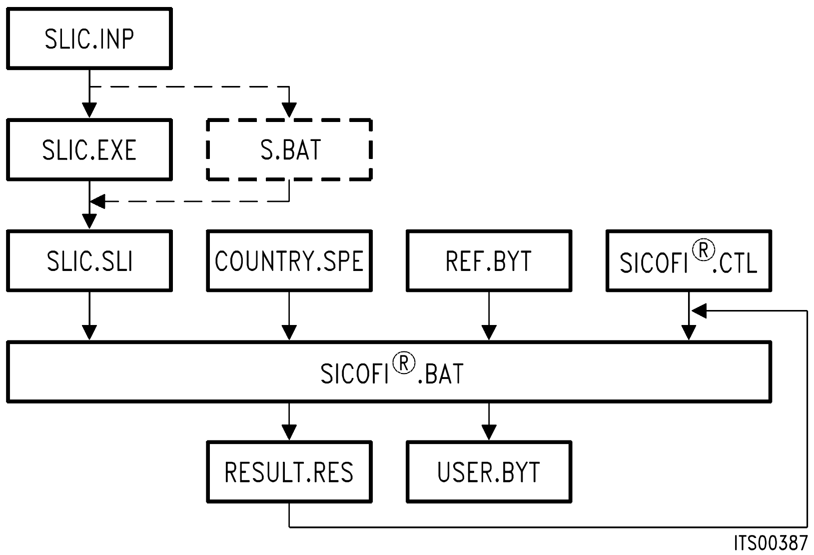
COUNTRY.SPE is an input file of the SICOFI program describing the customer's specification (CCITT etc ...) and measurement configuration parameters (e.g. termination impedance).

REF.BYT is an optional input file of the SICOFI program. It is a reference file which defines a frame in which the program can write the calculated coefficients with some predefined commands. These commands are the macrocommands necessary to send the SICOFI coefficients from the PBC/PIC (PEB 2050/52) to the SICOFI (PEB 2060/2260) by means of the SLD-bus control byte. After a calculation the actual SICOFI coefficients may be stored in an output file called e.g. USER.BYT. This file contains the commands from the REF.BYT file together with updated coefficients.

SICOFI.CTL is the control file of the SICOFI program. It contains the data controlling the optimization and simulation processes.

SICOFI.BAT is the SICOFI batch program which starts an execution program to generate the SICOFI coefficients and calculate the theoretical transfer functions of the set of SLIC-SICOFI.

RESULT.RES is the output file of SICOFI.BAT. It contains the coefficients for programming the SICOFI according to the SLIC used. The calculated results corresponding to various measurements to be taken on the set SICOFI + SLIC are listed. (e.g. return loss, frequency response, echo return loss, etc.) This result file can also be used as control file of SICOFI.BAT.



SICOFI® Software Structure

3 SICOFI® Test Board (STUT 2060)

3.1 Features

- Two SICOFI PEB 2060 and one PBC PEB 2050 or PIC PEB 2052 onboard
- SAB 8031 microprocessor system
- Serial interface
- Two interfaces for connecting customer specific SLIC boards
- Adapter for connecting SICOFI-2 PEB 2260 included

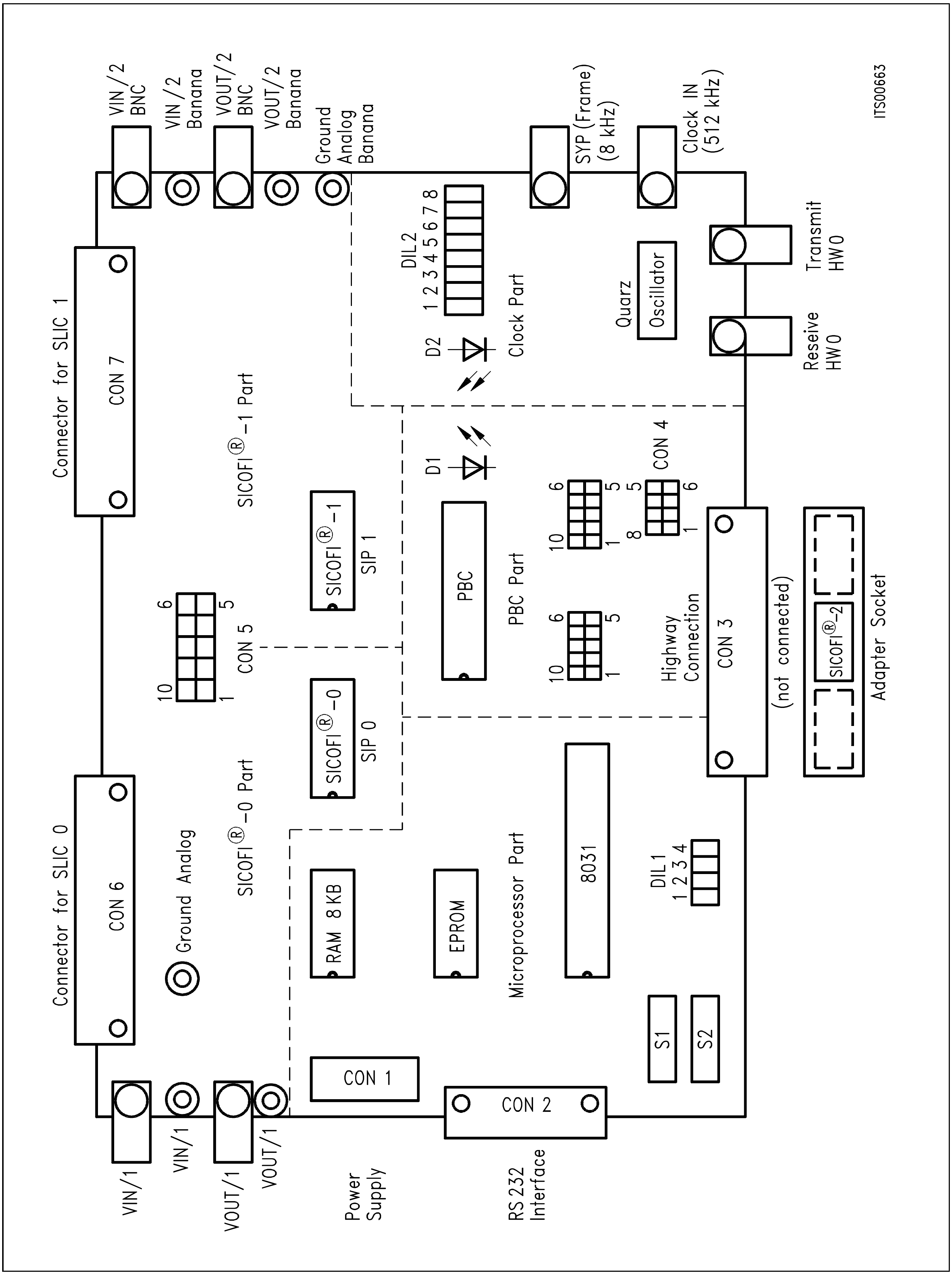
3.2 General Overview

The SICOFI® test board STUT 2060 is a stand alone board which offers the possibility of connecting any external customer specific SLICs with the SICOFI for evaluation of customer specific combinations of SLIC and SICOFI. This setup allows measurements and tests covering the transfer functions of the complete subscriber line module.

The board is programmable via an RS 232 interface by a terminal or PC. The registers of the PBC or PIC and SICOFI can be accessed and therefore the SLIC can be programmed.

Different customer specific SLICs or ready designed SLIC boards available from Siemens Semiconductor may be connected to the SICOFI testboard STUT 2060 via a 64-pin connector. With this setup it is possible to make the following investigations:

- to test the SLIC hardware
- to verify the programmed coefficients, which are calculated with the SICOFI coefficients program
- to measure many different SLICs in a short time


VIN/2 BNC
VIN/2 Banana
VOUT/2 BNC
VOUT/2 Banana
Ground Analog Banana
SYP (Frame) (8 kHz)
Clock IN (512 kHz)
ITS00663
Connector for SLIC 1
CON 7
SICOFI®-1 Part
DIL 2
1 2 3 4 5 6 7 8
D2
Clock Part
Quarz
Oscillator
Transmit HW0
Reseive HW0
D1
CON 4
SICOFI®-1
SIP 1
PBC
PBC Part
CON 5
Highway Connection
CON 3
(not connected)
SICOFI®-2
Adapter Socket
SICOFI®-0
SIP 0
Connector for SLIC 0
CON 6
Ground Analog
SICOFI®-0 Part
8031
DIL 1
1 2 3 4
RAM 8 KB
EPROM
Microprocessor Part
S1
S2
CON 1
CON 2
VIN/1
VIN/1
VOUT/1
VOUT/1
Power Supply
RS 232 Interface

4 SICOFI®-2 Module (SIPB 5135)

4.1 Features

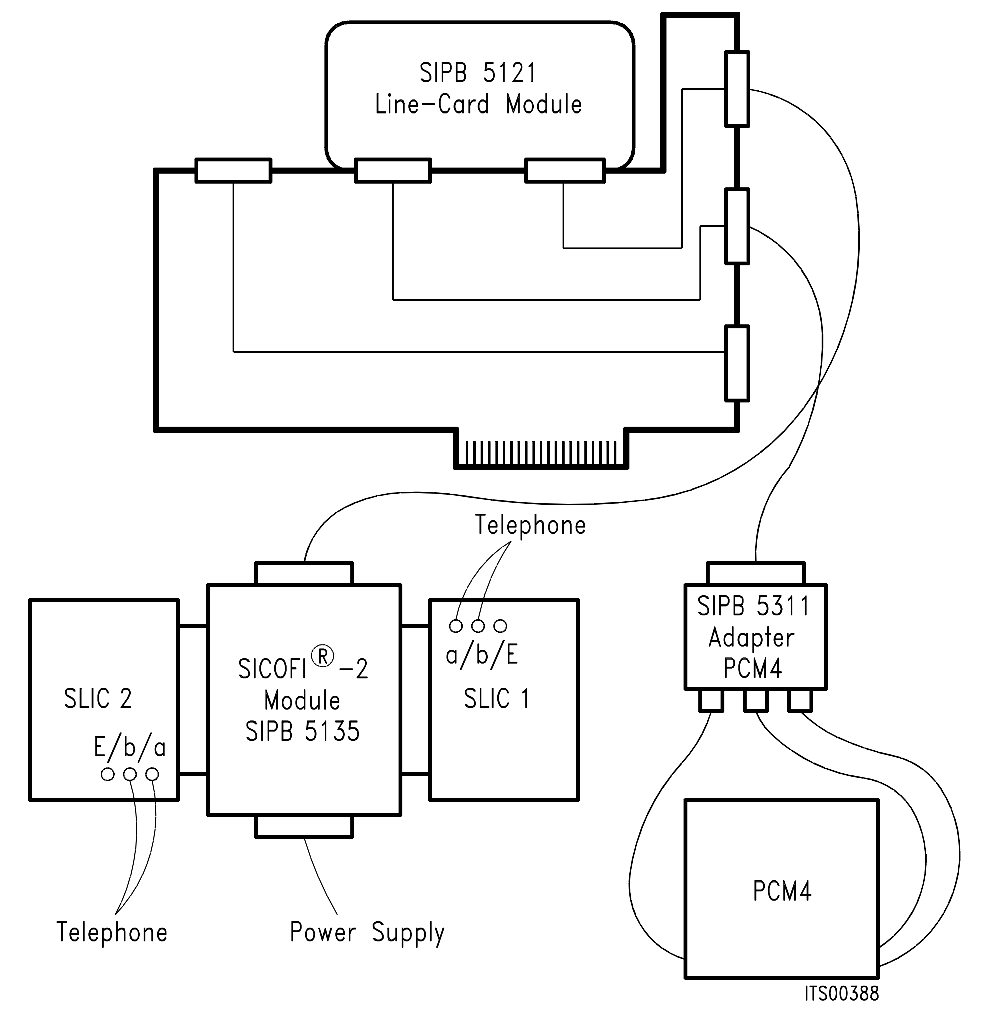
- Compatible to SIPB 5000 userboard system
- Two interfaces for connecting customer specific SLIC boards
- Same SLIC connector as on the SICOFI Testboard STUT 2060
- SICOFI-2 can be operated in two different interface modes (SLD or IOM®-2)

4.2 General Overview

The use of the Siemens ISDN PC Development System provides significant savings in R & D time when designing a customer specific ISDN application. The system consists of modular hardware in the form of the Siemens ISDN PC User Board (SIPB) and of several software packages.

With the SICOFI-2 PEB 2260 the SICOFI-2 module already provides a ready to use codec/filter and interfaces to two SLICs. Thus this module offers the outstanding advantage of enabling immediate starting with experiments on a subscriber line board.

The SICOFI-2 module SIPB 5135 is developed to be used in connection with the Line Card Module SIPB 5121. If at the secondary side of the Line Card Module a PCM4 Adaptor SIPB 5311 is connected, a very useful development and testing tool for the analog line card is built up. Using a PCM4 of Wandel & Goltermann the following measurements are possible:
- return loss
- level in A/D- and D/A-direction
- gain tracking in A/D- and D/A-direction
- noise in A/D- and D/A-direction
- echo return loss



Measuring Set Up with SICOFI®-2 Module

Software Description STS 2060

Contents **Page**

Contents (cont'd) **Page**

1 Introduction

How to Use This Manual

If you are already familiar with the former SICOFI software version 2.0, we suggest starting having a look at the 'New features in SICOFI software version 3.0' described in the appendix 9.1.

The background and some theory is described in chapters 2, 3 and 4.

If you want to start straightaway with the program, begin directly with chapter 5.

An example in chapter 6 explains how to obtain SICOFI coefficients for a special SLIC application.

Some tricks to take advantage of all the possibilities of the program are explained in chapter 7.

Measurements of SICOFI-SLIC transfer functions and some specifications are described in chapter 8.

The modularity and flexibility of the software introduces a large amount of files and variables. An alphabetical index is available at the end of this document in chapter 10:

'Index of the variables used in the software'

An idea of how to proceed in any case is suggested by the following **figure 1**.

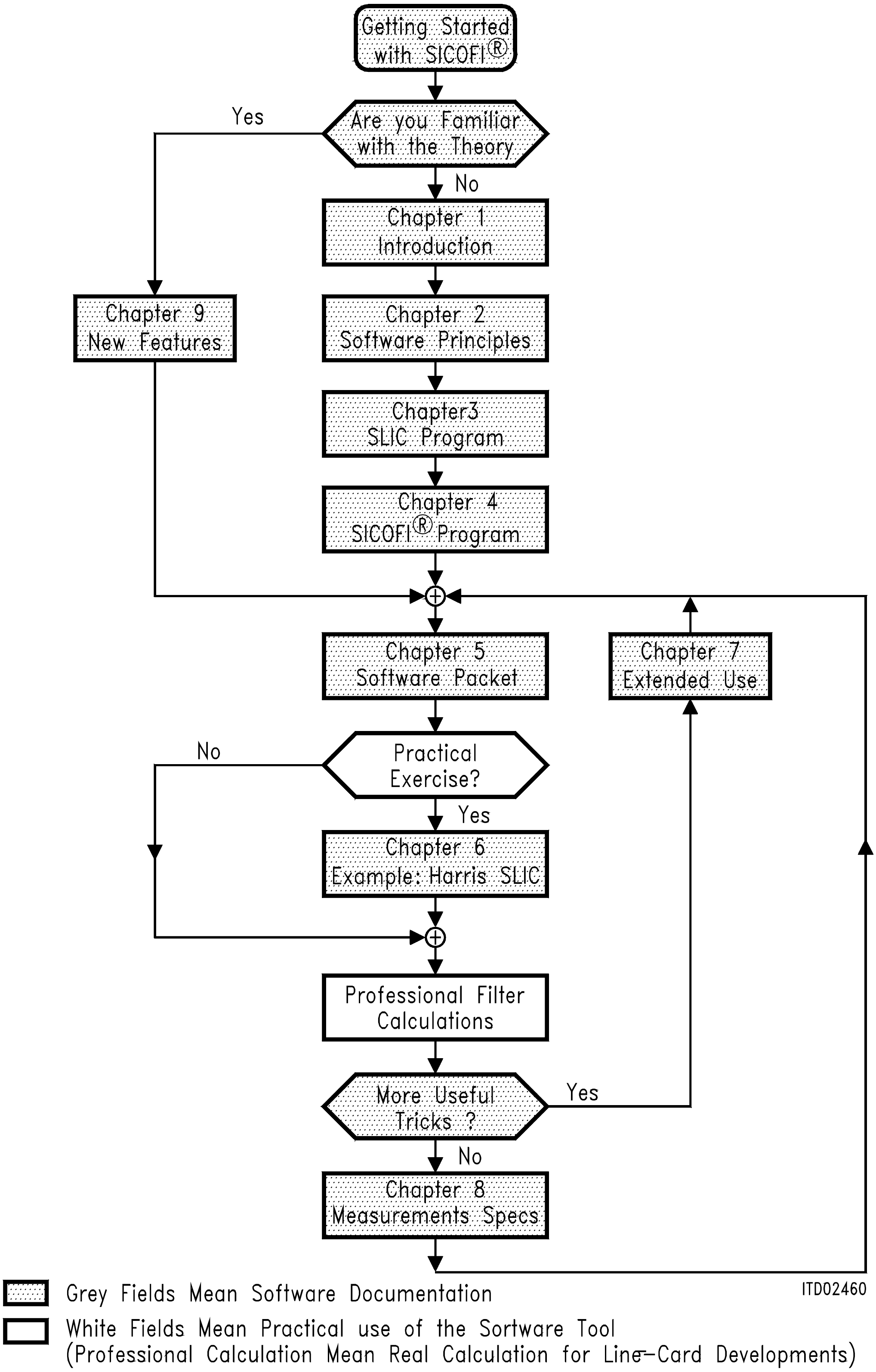


Figure 1
General Suggestions for Using this Manual

The SICOFI provides separate input and output ports for transmit and receive direction.

Transmit Direction

The analog input signal is A/D converted, digitally filtered and transmitted either PCM-encoded or linear. The A/D converter used is a modified slope adaptive interpolative sigma-delta modulator with a sampling rate of 128 kHz. To remove resulting noise, antialiasing is done with a 2nd order Sallen-Key prefilter (PREFI). Subsequently the signal is downsampled to 8 kHz by decimation filters D1 and D2 together with the PCM bandpass filters (LPX, HP).

Receive Direction

The digital input signal is received PCM-encoded or linear, digitally filtered and D/A converted to generate the analog output signal. Digital interpolation up to 128 kHz is done by the PCM lowpass filter (LPR) and the interpolation filters I1 and I2. The D/A Converter output is fed to the 2nd order Sallen-Key postfilter (POFI).

Programmable Function

The high flexibility of the SICOFI is based on a variety of user programmable filters, which are analog gain adjustment AGR and AGX, digital gain adjustment GR and GX, frequency response adjustment R and X, impedance matching filter Z and the transhybrid balancing filter B.

To gain an optimum result within a given environment while observing existing prescriptions, Siemens offers to the SICOFI user the software packet STS 2060, which performs the calculation of the filter coefficients by using an overall optimizing approach.

Because of the modularity of the SICOFI software program, it is possible to use the SICOFI together with

- transformer SLICs with series or transverse feeding
- fixed electronic SLICs (**see chapter 9.2: Available SICOFI / SLIC Documentation**)
- new user specific SLICs

The STS 2060 software runs on any IBM-AT compatible PC under MS-DOS Version 3.0 or later providing 640 Kbyte available RAM, a 1.2 Mbyte floppy disk drive, and the math coprocessor 80297 (optional).

The purpose of the following pages is to given an overview on the SICOFI software and its background.

For more details on the SICOFI hardware, refer to the SICOFI data sheets.

A list of the available SICOFI software and hardware tools will be found in chapter 9.2.

2 SICOFI® Software Principle

The hardware can be split into two parts: SLIC and its external circuitry on the one hand and SICOFI on the other (**see figure 2**).

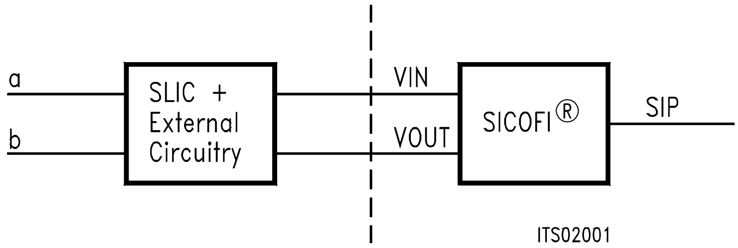


Figure 2
SLIC-SICOFI® Hardware

Accordingly the STS 2060 software consists of two major sections: SLIC program and SICOFI program.

A transfer file (SLIC file) provides the interface between these two programs (**see figure 3**).

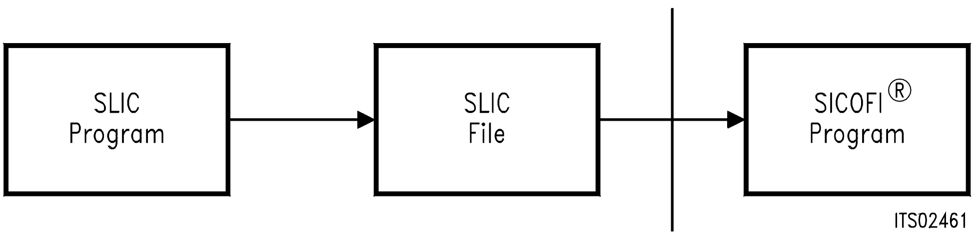


Figure 3
Software Structure

Details of the SICOFI software structure are shown in the following figure:

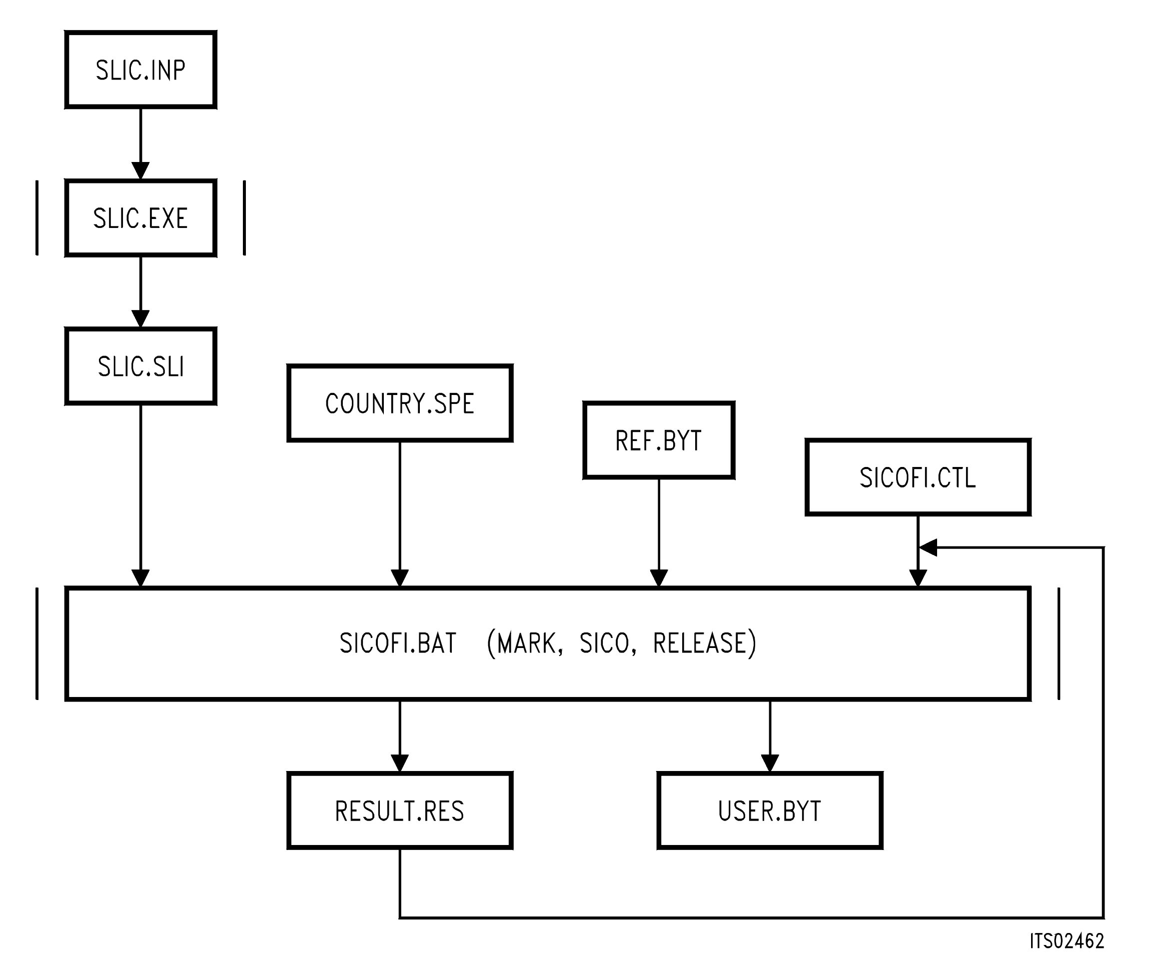


Figure 4
Details of the Software Structure

All the specific values concerning the SLIC and its external circuitry (physical data, filter dimensions, ...) are gathered in an input file SLIC.INP.

The SLIC program SLIC.EXE models the SLIC and its external circuitry in order to create a file SLIC.SLI which contains their transmission characteristics.

SLIC.SLI is a transfer file (output/input file) between the SLIC program and the SICOFI program to introduce the SLIC circuit data into the SICOFI program.

COUNTRY.SPE is an input file of the SICOFI program describing the customer's specification (CCITT etc ...) and measurement configuration parameters (e.g. termination impedance).

REF.BYT is an optional input file of the SICOFI program. It is a reference file which defines a frame in which the program can write the calculated coefficients with some predefined commands. These commands are the macrocommands necessary to send the SICOFI coefficients from the Peripheral Board Controller PBC (PEB 2050) to SICOFI (PEB 2060) by means of the SLD-bus control byte. After a calculation the actual SICOFI coefficients may be stored in an output file called e.g. USER.BYT. This file contains the commands from the REF.BYT file together with updated coefficients.

SICOFI.CTL is the control file of the SICOFI program. It contains the data controlling the optimization and simulation processes.

SICOFI.BAT is the SICOFI batch program which starts a execution program to generate the SICOFI coefficients and calculate the theoretical transfer functions of the set of SLIC-SICOFI.

RESULT.RES is the output file of SICOFI.BAT. It contains the coefficients for programming the SICOFI according to the SLIC used. The calculated results corresponding to various measurements to be taken on the set SICOFI + SLIC are listed. (e.g. return loss, frequency response, echo return loss, etc.). This result file can also be used as control file of SICOFI.BAT.

3 SLIC Program Description

3.1 Program Functions, M-Parameter

The SLIC program SLIC.EXE generates a model of the SLIC and its external circuitry to provide the SICOFI program with the transfer functions of this circuit.
The SLIC and its external circuitry are accessible through three ports as shown in **figure 5**.

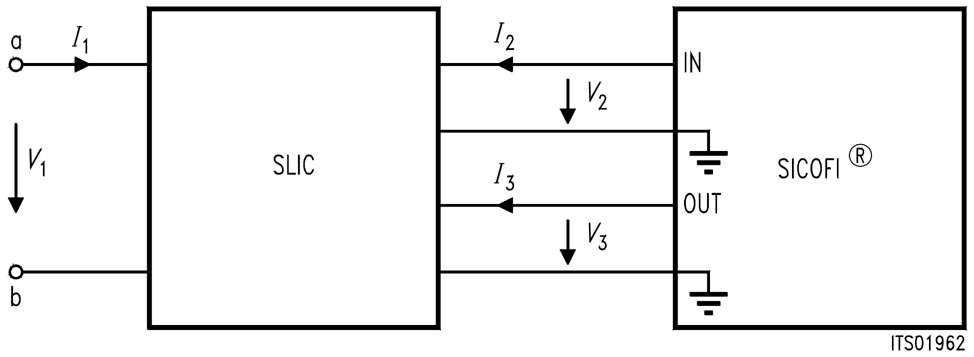
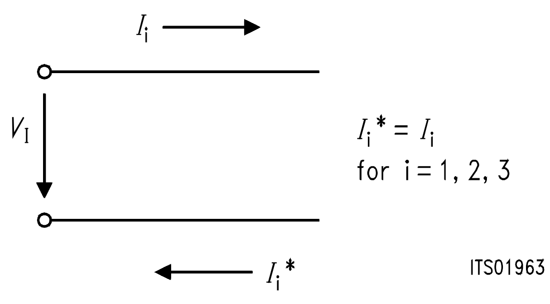


Figure 5
SLIC and its External Circuitry as a Three-Port

I_1, I_2 and I_3 are port currents and V_1, V_2 and V_3 are port voltages.
This circuit can be described by the following set of equations:
(1) $I_1 = \text{M11} \times V_1 + \text{M12} \times V_3 + \text{M13} \times I_2$
(2) $V_2 = \text{M21} \times V_1 + \text{M22} \times V_3 + \text{M23} \times I_2$
(3) $I_3 = \text{M31} \times V_1 + \text{M32} \times V_3 + \text{M33} \times I_2$

Note: definition of a port



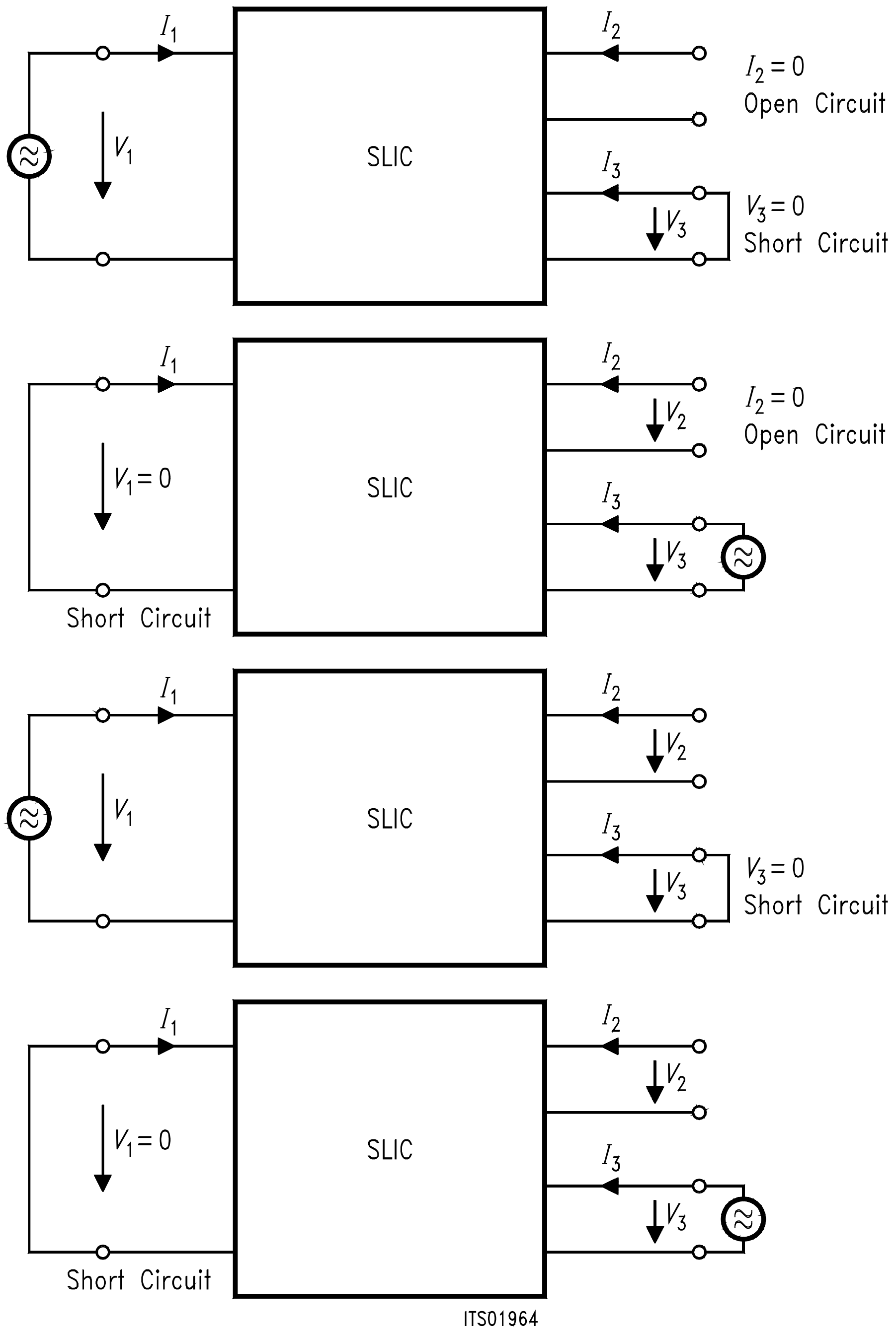
When the SLIC is connected to the SICOFI, we can assume that:

– $I_2 = 0$ because of the high SICOFI input impedance. (In special cases the SICOFI input impedance can be included in the three-port model.)

– I_3 is not relevant in the following calculations because the SICOFI works as an ideal voltage generator. (In special cases the SICOFI output impedance of about 10 Ω may be included in the SLIC model.)

According to the above remarks the equations can be simplified as follows:
(4) $I_1 = \text{M11} \times V_1 + \text{M12} \times V_3$
(5) $V_2 = \text{M21} \times V_1 + \text{M22} \times V_3$

The four remaining parameters M11, M12, M21, M22 fully describe the SLIC and its external circuitry.
They are determined as follows:



$M11 = I_1/V_1$ with $V_3 = 0$

$M12 = I_1/V_3$ with $V_1 = 0$

$M21 = V_2/V_1$ with $V_3 = 0$

$M22 = V_2/V_3$ with $V_1 = 0$

Figure 6
Definition of M-Parameters

Each M-parameter is then expressed in the SLIC program as an algebraic equation, containing a combination of the various SLIC parameters which are provided by the SLIC input file SLIC.INP. According to the values of the SLIC input data the SLIC program calculates the values of the M-parameters as a function of frequency and writes them to an output file SLIC.SLI. The values of each M-parameter for frequencies between 10 Hz and 3990 Hz in steps of 10 Hz are written into a table (**see chapter 3.3**).

SLIC.SLI then serves for the interface between the SLIC program and the SICOFI program.

The SLIC program SLIC.EXE and its source file SLIC.FOR are provided for fixed SLICs (see hereunder listed SLIC programs) and can be modified by the user to suit his peculiar application.

SLIC programs provided on the Siemens floppy disk STS 2060:

HARRIS.EXE	execution program of HARRIS SLIC HC 5502
TRAFOS.EXE	execution program of a transformer SLIC
TRAFOT.EXE	with series or transverse feeding.

The following SLIC programs are also available on request:

SGS.EXE	execution program of SGS SLIC L3030
NSGS.EXE	execution program of SGS SLIC L3090
ERIC.EXE	execution program of ERICSSON SLIC PBL 3762

The user can also develop his own SLIC program using any programming language. The only condition is to respect the standard format defined for the tables of SLIC.SLI (**see chapter 3.3**).

Chapter 3.2 shows an example of the SLIC input file for the HARRIS SLIC 5502.

The format of the SLIC program output file SLIC.SLI is shown in **chapter 3.3**.

3.2 Input File Description for HARRIS SLIC

This description is an example of the SLIC input file for the HARRIS SLIC HC 5502. **Figure 7** shows the interconnection of the HARRIS SLIC and the SICOFI.

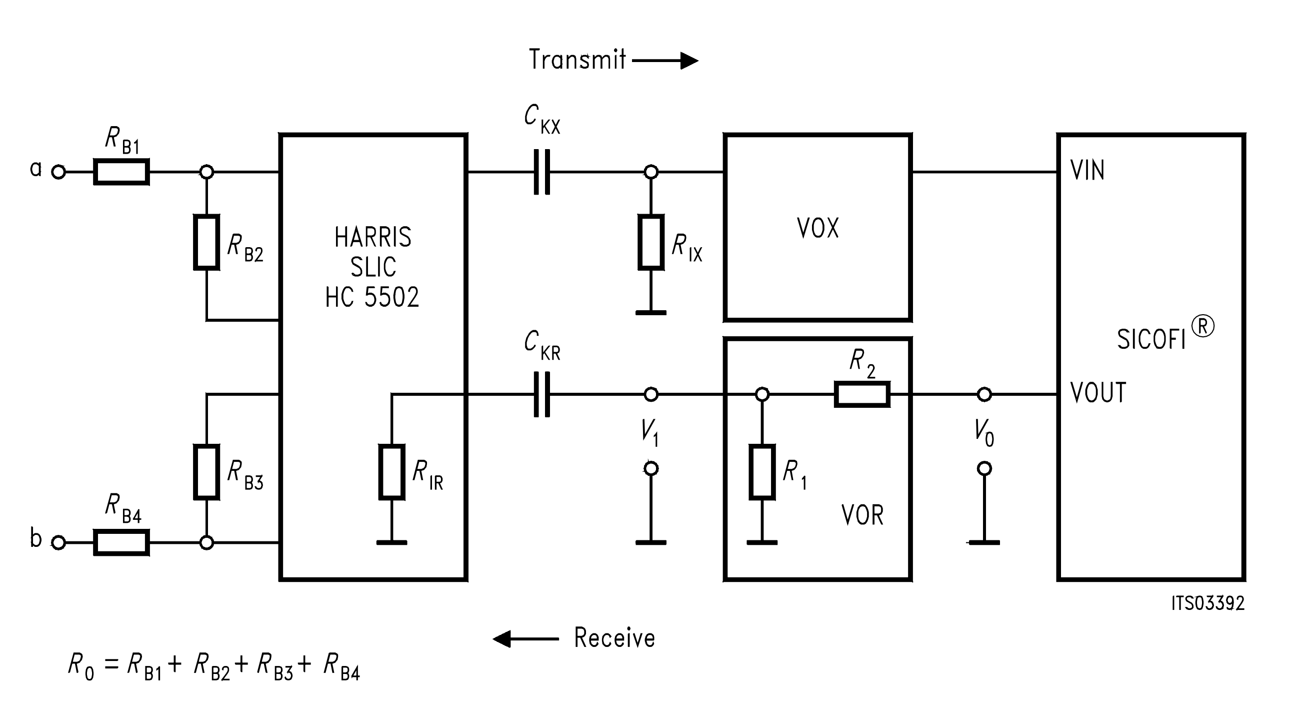


Figure 7
Connection SICOFI®-HARRIS SLIC

Note: SICOFI version V 4.x already includes a programmable attenuation (AGR) in the receive path.

The input file HARRIS.INP of the HARRIS SLIC program contains the following variables, which may be changed prior to a new run of the HARRIS.EXE program:

Variable name:	VOR
Function:	indicates the VOltage amplification factor between SICOFI and SLIC in Receive path
Value:	REAL number ($V_1/V_0 = R_2/R_1 + R_2$) if R_1, R_2 << R_{IR} e.g. $R_1 = R_2 = 300\ \Omega$
Variable name:	RIR
Function:	Input Resistor of the HARRIS SLIC in the Receive path
Value:	in Ω, e.g. $R_{IR} = 90000\ \Omega$ (data sheet)
Variable name:	CKR
Function:	decoupling Capacitor of the Receive path
Value:	in Farad

Variable name:	VOX
Function:	indicates the VOltage amplification factor between SLIC and SICOFI in transmit (Xmit) path.
Value:	REAL number (V_3/V_2)

Variable name:	RIX
Function:	Input Resistor in the transmit (Xmit) path
Value:	in Ohm

Variable name:	CKX
Function:	decoupling Capacitor of the transmit (Xmit) path.
Value:	in Farad

Variable name:	R_0 ($R_0 = R_{B1} + R_{B2} + R_{B3} + R_{B4}$)
Function:	controls the impedance matching (with help of SICOFI Z-filter it can be very simple (REAL))
Value:	in Ohm (REAL value)

Variable name:	ZSLI
Function:	minimal attenuation (resp. maximal gain) of the SLIC 4-wire side. Used by the SICOFI program during automatic calculation of Z-filter coefficients to check any possible overload in SICOFI Z-filter – SLIC loop (**see figure 8**)
Value:	in dB (must be expressed as attenuation: $-20 \times \log (V_T/V_R)$)
Practical use:	must be measured before using the SLIC and the SICOFI programs. It can be changed with an editor.

Note: The attenuation of the closed loop "Z filter – SLIC" must be greater than 1 (gain < 0 dB) in the frequency band 0 – 16 kHz in order to avoid any overload or oscillation.

The user has to measure the attenuation of the loop "SLIC input to SLIC output" over the whole frequency band 0 – 16 kHz for different terminating impedances.

The worst case (the smallest attenuation resp. the greatest gain) has then to be declared under the variable named ZSLI.

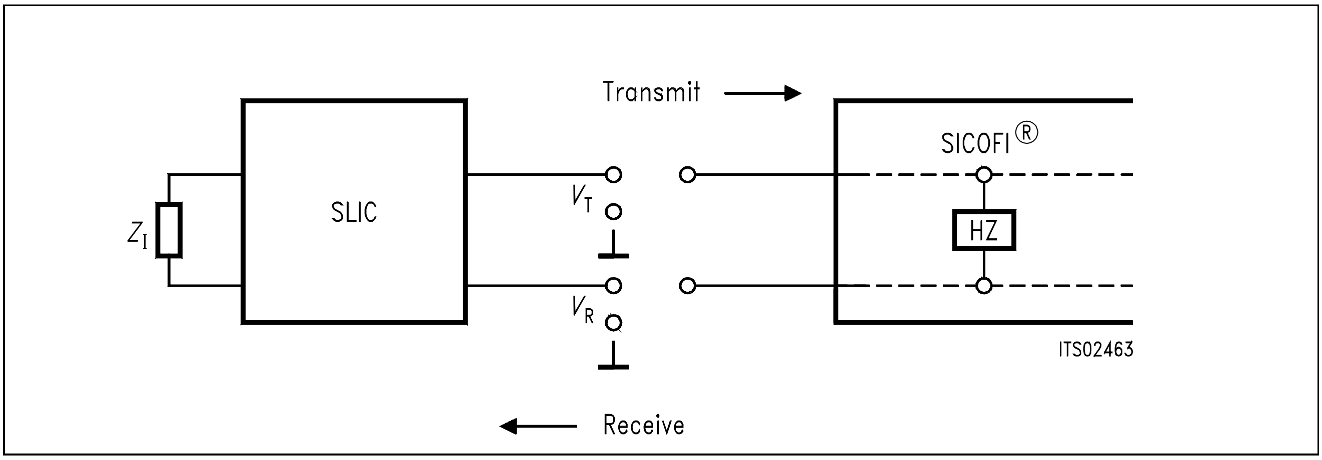


Figure 8
ZSLI Definition

Example: 3.5 dB gain in the loop " SLIC input to SLIC output": ZSLI = – 3.5

3.3 Output File Description, Format of the M-Parameter Table

The output file of the SLIC program has to be named "***.SLI".

The SICOFI program expects a table as shown in **figure 9**.

Figure 9
Format of the M-Parameter Table

```
* HARRIS SLIC                                                      Comment
* VOR = 0.50000    RIR = 90000.         CKR = 1.000E-06            lines
* VOX =  1.0000    RIX = 0.10000E+06    CKX = 1.000E-06            beginning
* R0  =  600.00                                                    with "*".

ZSLI    worst case half loop value
0.50000

       FREQ              REAL              IMAG
M11-TABLE                                                    keyword
  10.000000      1.666667E-03      0.000000E+00
  20.000000      1.666667E-03      0.000000E+00              table
...........      ............      ............
3980.000000      1.666667E-03      0.000000E+00              400 steps
3990.000000      1.666667E-03      0.000000E+00              of 10 Hz each.
M12-TABLE
  10.000000     -1.616127E-03     -2.857940E-04
  20.000000     -1.653738E-03     -1.462225E-04
 ...
3980.000000     -1.666666E-03     -7.405309E-07
3990.000000     -1.666666E-03     -7.386749E-07
M21-TABLE
  10.000000      9.752955E-01      1.552231E-01
  20.000000      9.937073E-01      7.907671E-02
 ...
3980.000000      9.999999E-01      3.998867E-04
3990.000000      9.999999E-01      3.988845E-04
M22-TABLE
  10.000000     -9.191039E-01     -3.177564E-01
  20.000000     -9.790611E-01     -1.656447E-01
 ...
3980.000000     -9.999995E-01     -8.442052E-04
3990.000000     -9.999995E-01     -8.420893E-04
```

The first comment lines beginning with "*" document the external SLIC components. These lines are copied to the SICOFI result file.

The first column indicates the frequency value, the second one the real part value of the M-parameter at this frequency and the third one the imaginary part value.

These three values are separated by at least a single space character.

Every REAL number must contain a decimal point (e.g. 2. or 2.00).

The value of the variable ZSLI of the SLIC input file is obligatorily declared again in this file.

4 SICOFI® Program Description

The actual SICOFI program section starts with an overview of the SICOFI program features. Then it describes the different input files of the SICOFI program like the CONTROL file, SPECIFICATION file and the BYT file. At the end of this chapter you will find a description of the SICOFI RESULT file with additional explaining comments.

4.1 Program Functions

The SICOFI program has been developed to help the user in adapting the SICOFI to his particular application.

It allows him:

– to find the optimal set of coefficients of each SICOFI filter and to calculate the theoretical transfer functions of the whole circuit SICOFI-SLIC (return loss, transhybrid loss, frequency responses, …) (Command OPT).

– to simulate the transfer functions of a part of the circuit SICOFI-SLIC and to perform some tolerance analysis (Command SIM).

The SICOFI program is user friendly.

Without exiting the program one can:

– modify the value of the variables in the control file (SICOFI.CTL) and interchange input files (Command DATA).

–

– use abbreviations for the variable units (powers of ten).

– store a calculation session in a file (Command ECHO).

– generate a USER.BYT file newest to the set of coefficients optimized (Command BYT).

– store in a file some intermediate results or the final ones (Command RES).

– access help files (Command HELP).

– use DOS commands (Command DOS).

– start a SLIC calculation without leaving the program.

– program the SICOFI testboard with a RS232 interface program.

A command line which shows the above mentioned commands is always presented after a filter calculation run at the bottom of the screen.

4.2 Control File: SICOFI.CTL

This file contains the data controlling the optimization and simulation processes. A control file HARRIS.CTL is given at the end of this variable list on **chapter 4.2**. If not adversely noted, variables may be changed during a session (use command DATA).

Variable name: SPEC

Abbreviation meaning: SPECification file name.

Function:	indicates in which file the specifications to be fulfilled are described.
Value:	the name of an existing file!
Practical use:	the file has to be prepared with the editor before running the program. For different countries peculiar SPEC-files may be prepared. The SPEC file name can be changed during the session (command DATA). The extension name must be ***.SPE.
Variable name:	SLIC
Abbreviation meaning:	SLIC program output file.
Function:	indicates the name of the output file of the SLIC which contains the SLIC parameters.
Value:	give the name of an existing file!
Practical use:	the file is generated by the SLIC program and it can be changed during the session by changing the name (SLIC = OTHER.SLI) with command DATA. The extension name must be ***.SLI.
Variable name:	VERSION
Abbreviation meaning:	VERSION of the SICOFI which coefficients have to be calculated.
Function:	indicates the version of the SICOFI in order that the program can take the adequate SICOFI transfer functions into account.
Value:	Vx.y (e.g. V3.1, V4. x …)
Variable name:	REL
Abbreviation meaning:	RELative question flag
Function:	indicates whether the values of the transfer functions in simulation mode are relative (refering to values at FREF) or absolute.
Value:	Y (relative) or N (absolute)

Variable name:	BYTE
Abbreviation meaning:	reference BYTE file.
Function:	indicates the name of the reference file used to generate a new file consisting of the Peripheral Board Controller macrocommands combined with the newly calculated coefficients.
Value:	give the name of an existing file!
Practical use:	the reference file must be prepared with an editor before running the session but the name can be changed during the session (command DATA). The extension name must be ***.BYT.

Variable name:	CHNR
Abbreviation meaning:	CHannel NummbeR.
Function:	indicates for which SIP-line (0 … 7) and which channel (A or B) the macrocommands of the reference file have to be updated.
Value:	CHNR = 0, A for SIP line 0 and voice channel A.

Variable name:	PLQ
Abbreviation meaning:	PLot Question flag.
Function:	the calculated transfer functions ZIN, AD, DA and DD are stored together with the corresponding specification masks by the command RES. This will provide the possibility to plot the result curves together with the specification masks.
Value:	Y or N.
Practical use:	**Note:** You may generate a plot table with the command 4 SIM. This plot file is stored with the command 6 RES. The screen plot program is not available with the present program version (3.0), but the user may use his own plot program to display the prepared plot data.

Variable name:	FSTA
Abbreviation meaning:	plot Frequency STArt.
Function:	defines at which frequency the plot starts.
Value:	in Hz (FSTA > 0 Hz).
Practical use:	Data valid only when PLQ = Y.

Variable name:	FSTO
Abbreviation meaning:	plot Frequency STOp.
Function:	defines at which frequency the plot stops.
Value:	in Hz (FSTO < 4000 Hz).
Practical use:	Data valid only when PLQ = Y. You must define: FSTO > FSTA.

Variable name:	STEP
Abbreviation meaning:	plot frequency STEP.
Function:	defines the frequency step used for calculation of the plot results.
Value:	in Hz.
Practical use:	Data valid only when PLQ = Y.

Variable name:	ON
Abbreviation meaning:	SICOFI filters switched ON.
Function:	defines which filters are switched on for the optimization and simulation process.
Value:	All or a combination of Z, X, R, GX, GR and B: e.g. ON = Z or ON = Z + R + X + B or ON = ALL
Practical use:	You must declare variables ON or OFF.

Variable name:	OFF
Abbreviation meaning:	SICOFI filters switched OFF.
Function:	defines which filters are switched off during the optimization and simulation process.
Value:	All or a combination of Z, X, R, GX, GR and B: e.g. OFF = R + X + B or OFF = ALL
Practical use:	You must declare variables ON or OFF.

Variable name:	SHORT
Abbreviation meaning:	SHORT display flag
Function:	flag which indicates that the results will be displayed in a short form. No: display of the calculated coefficients and of all the transfer functions. Yes: neither the calculated coefficients nor the return loss and transhybrid loss are displayed. For Z and B filters only the minimum reserve to or the maximum violation of corresponding specifications are displayed.
Value:	Y (Yes) or N (No)

Variable name:	OPT
Abbreviation meaning:	OPTimization of the SICOFI filter coefficients
Function:	indicates the filters for which the program will calculate the coefficients.
Value:	ALL or a combination of Z, X, R and B e.g. OPT = Z or OPT = Z + R + X + B or OPT = ALL. GR and GX filters are optimized at the same time as the R and X filters respectively.
Practical use:	An optimization starts with the command OPT.

Variable name:	SIM
Abbreviation meaning:	SIMulation of different transfer paths.
Function:	indicates the path of the circuit SICOFI-SLIC which transfer function will be simulated. The different transfer functions, which can be simulated, are explained in **chapter 5.6** (command SIM).
Value:	ALL or a combination of ZIN, AD, DA, DD, ASI, ASO, DSI, DSO (e.g. ZIN + DSI)
Practical use:	A simulation starts with the command SIM.

Variable name:	ZXRB
Abbreviation meaning:	Calculation status of the Z-, X-, R- and B-filter respectively.
Function:	indicates the calculation status: Which filter coefficients have already been calculated?
Value:	N (New), O (old) or X (not calculated). "New" means that the coefficients of the corresponding filter have been calculated during the last run. "Old" means that the coefficients of the corresponding filter have been calculated before the last run.
Practical use:	Is simply an indicator to the user which must not be changed during the session.

Variable name:	ZAUTO
Abbreviation meaning:	AUTOmatic calculation flag of the Z filter coefficients.
Function:	indicates whether the program is to use mathematical algorithms to optimize the Z filter coefficients (automatic calculation), or the sampling points FZP defined by the variables PZIN, PSP, WFZ (no automatic calculation).
Value:	Y (automatic) or N (no automatic calculation)
Practical use:	**Note:** ZAUTO was previously defined by PZIN = 0. During the automatical calculation, an iteration number appears on the screen to show the progression of the program and indicates how close the program is to a satisfying result. As soon as the iteration number turns negative, the result is fulfilling the required specifications. The more negative the result is, the better it is.

Variable name:	PZIN
Abbreviation meaning:	number of sampling Points for Z-filter calculation withIN the speechband.
Function:	indicates the number of frequency sampling points of the Z filter within the speech band (100 Hz < FREQ < 3400 Hz) if the Z filter coefficients are not automatically optimized (ZAUTO = N).
Value:	between 5 and 20 (One must have: 5 < PZIN + PSP < 20).
Practical use:	Experience has shown that the optimum value for PZIN is between 8 and 13.

Variable name: PSP

Abbreviation meaning: number of sampling Points in Stop band

Function: indicates the number of frequency sampling points of the Z filter out of the speech band (3400 Hz < FREQ < 16000 Hz) if the Z filter coefficients are not automatically optimized (ZAUTO = N).

Value: PSP must fulfill the following condition: 5 < PZIN + PSP < 20.

Practical use: Experience has shown that PSP = 3 is the optimum value.

Variable name: FZP

Abbreviation meaning: Frequency points for Z-filter calculation

Function: indicates the frequency of the sampling points of the Z filter in non-automatic (ZAUTO = N) optimization mode (PZIN + PSP values are expected).

Value: between 100 and 16000 Hz.

Practical use: FZP (2) = 500,2.0
changes Z-filter frequency point (2) to new frequency (500 Hz) and new weighting factor (2.0).
The user may also change all sampling frequency points:
FZP = 350, 450, 1000, 1300, 1600, 2000, 2500, 2800, 3000, 3200, 3400, 8000, 10000, 13000

Variable name: WFZ

Abbreviation meaning: Weighting Factors for Z filter.

Function: indicates the weighting factors assigned to individual frequency sampling points FZP of the Z filter in non automatic optimization mode (ZAUTO = N). PZIN and PSP weighting factors are expected.

Value: INTEGER value.

Practical use: Experience has shown that the values of WFZ preferably are between 0.1 and 10.0. They can be changed during the session (command DATA).
WFZ = 1.0, 1.5, 1.5, 2.0, 2.0, 1.5, 1.0, 1.0, 1.0, 1.0, 1.0, 1.0, 1.0, 1.0
changes all the weighting factors for the frequency points defined in FZP. If different frequency points have a relative high weighting factor, the program tries to calculate good results at this points, but the results at other frequencies may become worse.

Variable name: FZ

Abbreviation meaning: Frequency range for Z-filter calculation. In automatic optimization mode (ZAUTO = Y) FZ indicates the frequency band to which optimization applies (2 values are expected).

Value: The range should be within the limits defined in the actual specification file:
FZ = 300 3400

Practical use: FZ = 500 3200 defines a new optimization range for the Z-filter.

Variable name: ZLIM

The value of this variable has to be changed only in special cases … See its description in **chapter 7.1**.

Variable name: ZREP

Abbreviation meaning: REPeat flag of Z filter automatic calculation

Function: indicates whether or not the automatic optimization of Z filter coefficients will be restarted from precalculated values.

Value: Y (Yes) or N (No).

Variable name: ZSIGN

The value of this variable has to be changed only in special cases. See its description in **chapter 7.1**. Most of the time ZSIGN = 1.

Variable name:	FR
Abbreviation meaning:	Frequency band for R filter calculation
Function:	indicates the frequency band which the optimization of the R filter coefficients applies.
Value:	two INTEGER values within the speech band. The range should be within the limits defined in the actual specification file: FR = 300 3400

Variable name:	RDISP
Abbreviation meaning:	R filter frequency response DISPlay flag
Function:	indicates whether or not the absolute frequency response of the R filter alone will be displayed.
Value:	Y (Yes) or N (No).
Practical use:	**Note:** In software versions prior to V3.0 RDISP was defined by RFIL.

Variable name: RREFQ

The value of this variable has to be changed only in special cases … See its description in **chapter 7.1**. Most of the time RREFQ = N.

Variable name: RREF

The value of this variable has to be changed only in special cases … See its description in **chapter 7.1**.

Variable name:	FX
Abbreviation meaning:	Frequency band for X filter calculation
Function:	indicates the frequency band to which the optimization of the X filter coefficients applies.
Value:	two INTEGER values within the speech band: FX = 300 3400

Variable name:	XDISP
Abbreviation meaning:	X filter frequency response DISPlay flag
Function:	indicates whether or not the absolute frequency response of the X filter alone will be displayed.
Value:	Y (Yes) or N (No).
Practical use:	**Note:** XDISP was previously defined by XFIL

Variable name: XREFQ

The value of this variable has to be changed only in special cases … See its description in **chapter 7.1**. In general XREFQ = N.

Variable name: XREF

The value of this variable has to be changed only in special cases … See its description in **chapter 7.1**.

Variable name:	BAUTO
Abbreviation meaning:	AUTOmatic calculation flag of the B filter coefficients.
Function:	indicates whether the program uses mathematical algorithms to optimize the B filter coefficients (automatic calculation) or the sampling points FBP defined by the variables PB, GWFB, WFB (non-automatic calculation). (see also ZAUTO)
Value:	Y (automatic) or N (non-automatic)
Practical use:	**Note:** BAUTO was previously defined by PB = 0

Variable name:	PB
Abbreviation meaning:	number of sampling Points for B filter calculation
Function:	indicates the number of frequency sampling points of the B filter within the speech band (100 Hz < FREQ < 3400 Hz) if the B filter coefficients are not automatically optimized (BAUTO = N).
Value:	between 10 and 20.
Practical use:	the program uses the sampling points defined in the control file to calculate the B filter coefficients. Experience has shown that the optimum value for PB is around 10.

Variable name:	GWFB
Abbreviation meaning:	General Weighting Factors for B filter.
Function:	indicates the general weighting factor of the B filter in non-automatic optimization mode (BAUTO = N).
Value:	REAL.
Practical use:	Experience has shown that the optimum value for GWFB is between 0.01 and 0.1.

Variable name:	FBP
Abbreviation meaning:	Frequencies of sampling Points for B filter calculation
Function:	indicates the frequencies of the sampling points for B filter calculation in non-automatic optimization mode (PB values are expected).
Value:	value between 100.0 and 3400.0 Hz.
Practical use:	FBP (3) = 800, 1.5 changes B-filter frequency point (3) to new frequency (800 Hz) and new weighting factor (1.5). The user may also change all sampling frequency points: FBP = 350, 450, 800, 1000, 1600, 2000, 2500, 2800, 3200, 3300

Variable name:	FB
Abbreviation meaning:	Frequency range for B filter calculation
Function:	In automatic optimization mode (BAUTO = Y) FB indicates the sampling frequency band (2 values are expected): FB = 300 3400
Value:	the range should be within the limits defined in the actual specification file.
Practical use:	FB = 500 3200 defines a new optimization range for the B filter.

Variable name:	WFB
Abbreviation meaning:	Weighting Factors for B filter.
Function:	indicates the weighting factors of the individual sampling frequency points of the B filter in non-automatic optimization mode (BAUTO = N).
Value:	REAL value.
Practical use:	Experience has shown that the values of WFB are between 0.5 and 5.0. WFB = 3.0, 2.5, 2.0, 1.0, 1.0, 1.0, 1.0, 1.0, 1.0, 1.0 changes all the weighting factors for the frequency points defined in FBP. If different frequency points have a relative high weighting factor, the program tries to calculate good results at this points, but the results at other frequencies may become worse.

Variable name:	BDF
Abbreviation meaning:	B-Delay Filter
Function:	indicates the delay factor of the B filter in multiples of 62.5 micro sec.
Value:	0, 1, 2 or 3 (× 62.5 micro sec.).
Practical use:	Experience has shown that the optimum value is mostly BDF = 1.
Practical use:	**Note:** In software versions prior to V3.0 BDF was defined by TBM.

Variable name: BLIM

The value of this variable has to be changed only in special cases ... See its description in **chapter 7.1**.

Variable name:	BREP
Abbreviation meaning:	REPeat flag of B filter automatic calculation
Function:	indicates whether or not the automatic optimization of B filter coefficients will be restarted from already calculated values.
Value:	Y (Yes) or N (No).

Variable name: BSIGN

The value of this variable has to be changed only in special cases … See its description in **chapter 7.1**. In general BSIGN = 1.

Variable name:	DPOF
Abbreviation meaning:	supplementary Delay after the SICOFI POst-Filter
Function:	Allows the insertion of an additional group delay in receive path between the SLIC and the SICOFI.
Value:	in seconds.
Practical use:	See also special application described in **chapter 7.1**.

Variable name:	DPRE
Abbreviation meaning:	supplementary Delay before the SICOFI PRE-filter
Function:	Allows the insertion of an additional group delay in transmit path between the SLIC and the SICOFI.
Value:	in seconds.
Practical use:	See also special application described in **chapter 7.1**.

Variable name:	APOF
Abbreviation meaning:	supplementary Amplification after the SICOFI POst-Filter
Function:	Allows the insertion of an additional attenuation in receive path between the SLIC and the SICOFI.
Value:	in dB.
Practical use:	See also special application described in **chapter 7.1**.

Variable name:	APRE
Abbreviation meaning:	supplementary Amplification before the SICOFI PRE-filter
Function:	Allows the insertion of an additional attenuation in transmit path between the SLIC and the SICOFI.
Value:	in dB.
Practical use:	See also special application described in **chapter 7.1**.

Variable name:	AGX
Abbreviation meaning:	Analog Gain control transmit-path (Xmit) of SICOFI.
Function:	Allows an additional amplification in transmit path of SICOFI.
Value:	AGX = 00 0 dB AGX = 01 6 dB amplification AGX = 10 12 dB amplification AGX = 11 14.2 dB amplification
Practical use:	AGX is used for SICOFI versions V 4.1 or later. It is programmed by the SICOFI configuration register CR3.

Variable name:	AGR
Abbreviation meaning:	Analog Gain control receive-path of SICOFI.
Function:	Allows an additional attenuation in receive path of SICOFI.
Value:	AGR = 00 0 dB AGR = 01 6 dB attenuation AGR = 10 12 dB attenuation AGR = 11 14.2 dB attenuation
Practical use:	AGR is used for SICOFI versions V 4.1 or later. It is programmed by the SICOFI configuration register CR3.

Variable name:	TM3
Abbreviation meaning:	Test Mode of SICOFI: Additional digital gain in transmit path
Function:	Allows an additional digital amplification in transmit path of SICOFI.
Value:	TM3 = 000 0 dB TM3 = 001 6 dB amplification TM3 = 011 12 dB amplification
Practical use:	TM3 is used for SICOFI versions V 4.1 or later. It is programmed by the SICOFI configuration register CR4. The quantization steps of the SICOFI GX filter are relative high in the range of 8 to 12 dB. By programming TM3 you may find a GX amplification range with smaller quantization steps in the range 0 to 8 dB. Additional programming of TM3 is allowed which is not used in the SICOFI coefficients program: TM3 = 100 Enable on chip sine wave generation TM3 = 110 Far analog loop back

4.2.1 Listing of the SICOFI Control File HARRIS.CTL

```
SPEC = BRD.SPE                      SLIC = HARRIS.SLI
BYTE = REF.BYT                      CHNR = 0,A
VERSION = 4.2                       REL = Y
ON = ALL
OPT = Z+X+R+B                       ZXRB = NNNN
ZAUTO = N                           PZIN = 11  PSP = 3
FZP =  300.0      500.0             1000.0     1300.0     1500.0
      2000.0     2500.0             2900.0     3000.0     3200.0
      3400.0     7000.0             10000.     14000.
WFZ =  0.100     1.00               2.00       1.50       1.00
        3.00     1.00               1.00       1.00       3.00
        2.80     1.00               1.00       1.00
FR    300.00     3400.0
RDISP = Y        RREFQ = N
FX    300.00     3400.0
XDISP = Y        XREFQ = N
BAUTO = N        PB = 10             GWFB = 0.500E-01      BDF = 1
FBP =  300.0      500.0              700.0     1000.0     1500.0
      2100.0     2300.0             2900.0     3200.0     3300.0
WFB =  4.000     2.000              1.000      5.000      1.000
       2.000     1.000              5.000      1.000      1.000
APRE =  0.0      DPRE = 0.0            APOF = 0.0    DPOF = 0.0
AGR = 00         AGX = 00              TM3 = 000
;
```

4.3 Specification File: COUNTRY.SPE

This file defines the national specifications which must be fulfilled. A specification file BRD.SPE containing the particular specifications for the Federal Republic of Germany is given at the end of this variable list on **chapter 4.3.3**. Values of variables may be changed by using a common editor (Using command DOS).

Variable name:	FREF
Abbreviation meaning:	Frequency REFerence.
Function:	indicates the reference frequency all calculations and frequency responses are referred to.
Value:	in Hz, e.g. FREF = 1014.
Practical use:	Once defined for an application it does not need to be modified.

Variable name:	LAW
Abbreviation meaning:	Compression/expansion LAW.
Function:	defines the law according to which the 16 bit word is compressed (resp. the 8 bit word is expanded).
Value:	A or U.
Practical use:	Once defined for an application it does not need to be modified.

Variable name:	VREF
Abbreviation meaning:	REFerence Voltage.
Function:	equals the reference voltage defined by the PTT (Telecom Authority). The reference voltage is the resulting voltage at the reference impedance ZR, if 1 mW of power of frequency FREF are applied. VREF = SQRT (0.001* |ZR|).
Value:	in V.
Practical use:	Once defined for an application it does not need to be modified. Instead of using this reference voltage VREF you may use the country specific reference impedance ZR (see ZRRP1, ZRCP1, ZRRP2, ZRCP2, ZRRS, ZRCS). Then the SICOFI program automatically calculates the corresponding reference voltage.

Variable names:	ZRRP1, ZRCP1, ZRRP2, ZRCP2, ZRRS, ZRCS
Abbreviation meaning:	resistors and capacitors of the impedance ZR (see circuit library in **chapter 4.3.2**).
Function:	ZR defines the impedance used to calculate the reference voltage if this one is not explicitly declared.
Value:	resistors in Ohm and capacitors in Farad.

Variable name:	RLX
Abbreviation meaning:	Relative Level of the Xmit signal.
Function:	indicates the relative levels on the a,b line of the transmit signal with the reference level (0 dBm0) on the digital side.
Value:	in dBr.
Practical use:	See sign convention explained in **chapter 4.3.1**.

Variable name:	RLR
Abbreviation meaning:	Relative Level of the Receive signal.
Function:	indicates the relative level on the a,b line of the receive signal with the reference level (0 dBm0) on the digital side.
Value:	in dBr.
Practical use:	See sign convention explained in **chapter 4.3.1**.

Variable name:	ABIMP
Abbreviation meaning:	A, B -wire IMPedance
Function:	indicates the terminating impedance of the a,b line used for the measurements of the frequency response.
Value:	"ZI" or "Z3".
Practical use:	This impedance is not being considered in calculating the return loss and transhybrid loss. (see ZIRP1, ZICP1, ZIRP2, ZICP2, ZIRS, ZICS and Z3RP1, Z3CP1, Z3RP2, Z3CP2, Z3RS, Z3CS).

Variable names:	ZIRP1, ZICP1, ZIRP2, ZICP2, ZIRS, ZICS
Abbreviation meaning:	resistors and capacitors of impedance equivalent circuit "ZI" (see circuit library in **chapter 4.3.2**).
Function:	"ZI" defines the input impedance which the line card has to present from a,b line.
Value:	resistors in Ohm and capacitors in Farad.
Variable names:	ZLRP1, ZLCP1, ZLRP2, ZLCP2, ZLRS, ZLCS
Abbreviation meaning:	resistors and capacitors of impedance equivalent circuit "ZL" (see circuit library in **chapter 4.3.2**).
Function:	"ZL" defines the load impedance used for digital to digital measurements and calculations (e.g. echo return loss).
Value:	resistors in Ohm and capacitors in Farad.
Variable names:	Z3RP1, Z3CP1, Z3RP2, Z3CP2, Z3RS, Z3CS
Abbreviation meaning:	resistors and capacitors of impedance equivalent circuit "Z3" (see circuit library in **chapter 4.3.2**).
Function:	"Z3" defines a terminating impedance used for analog to digital and digital to analog measurements when ABIMP = Z3.
Value:	resistors in Ohm and capacitors in Farad.

The following variables define specification masks.

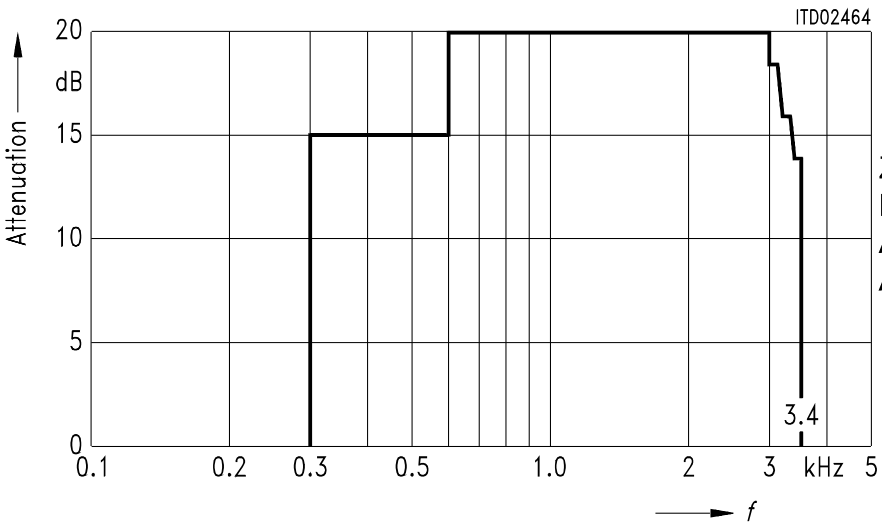
A mask can be described as a table as follows:

FR defines the frequency at which the mask value changes.

AT– defines the lower threshold value of the mask at the frequency FR.

AT+ defines the higher threshold value of the mask at the frequency FR.

Example: **figure 10** defines the mask of the return loss.



ZRE

FR	300	600	3kHz	3.4kHz
AT–	0	15	20	15
AT+	15	20	20	0

Figure 10
Specification Mask

In the specification file the following specification masks can be described:

Variable name: ZRE

Function: defines the mask of the return loss.

Value: FR in Hz, AT– and AT+ in dB.

Variable name: ZMIR

This variable does not need to be modified by the user. It is described in **chapter 7.1**.

Variable name: DA, UPPER

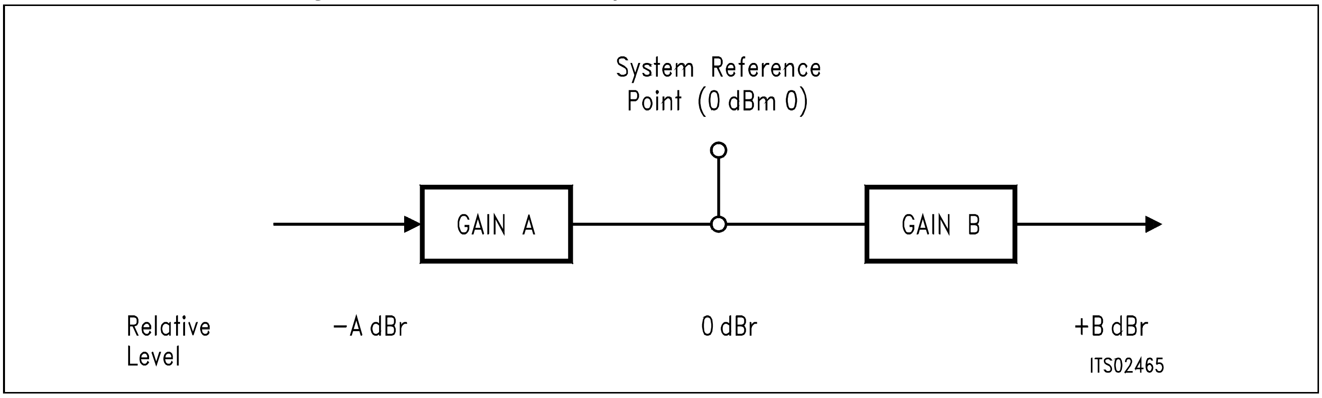
Function: defines the upper bound of the specification mask of the frequency response in receive path (D/A).

Value: FR in Hz, AT– and AT+ in dB.

Variable name:	DA, LOWER
Function:	defines the lower bound of the specification mask of the frequency response in receive path (D/A).
Value:	FR in Hz, AT– and AT+ in dB.
Variable name:	DA, DELAY
Function:	defines the specification mask of the group delay in receive path (D/A).
Value:	FR in Hz, AT– and AT+ in ms.
Variable name:	AD, UPPER
Function:	defines the upper bound of the specification mask of the frequency response in transmit path (A/D).
Value:	FR in Hz, AT– and AT+ in dB.
Variable name:	AD, LOWER
Function:	defines the lower bound of the specification mask of the frequency response in transmit path (A/D).
Value:	FR in Hz, AT– and AT+ in dB.
Variable name:	AD, DELAY
Function:	defines the specification mask of the group delay in transmit path (A/D).
Value:	FR in Hz, AT– and AT+ in ms.
Variable name:	DD
Function:	defines the mask of the transhybrid loss
Value:	FR in Hz, AT– and AT+ in dB.

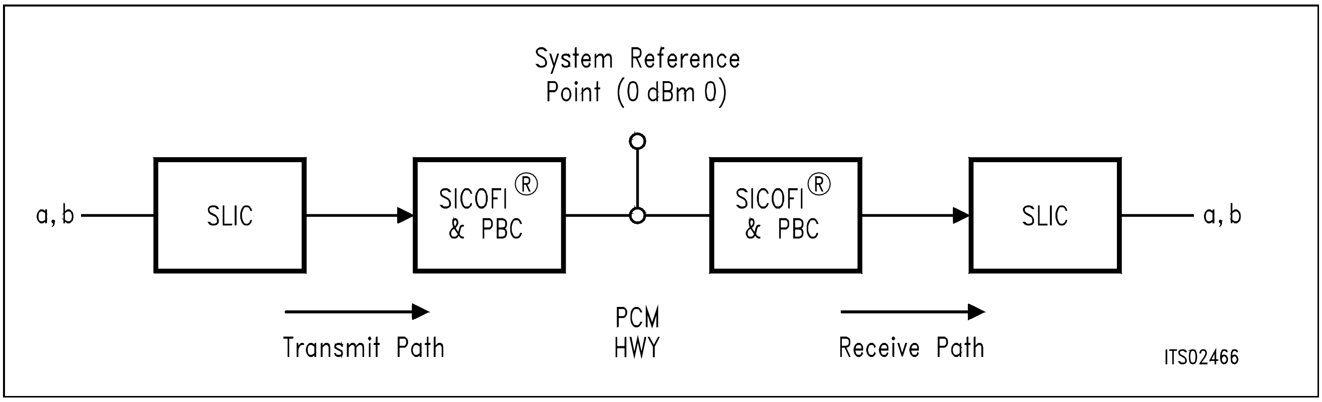
4.3.1 Sign Convention for Relative Levels

For a transmission system the relative levels are defined in dBr corresponding to the reference level 0 dBm0 of the signal at the reference point as shown below.

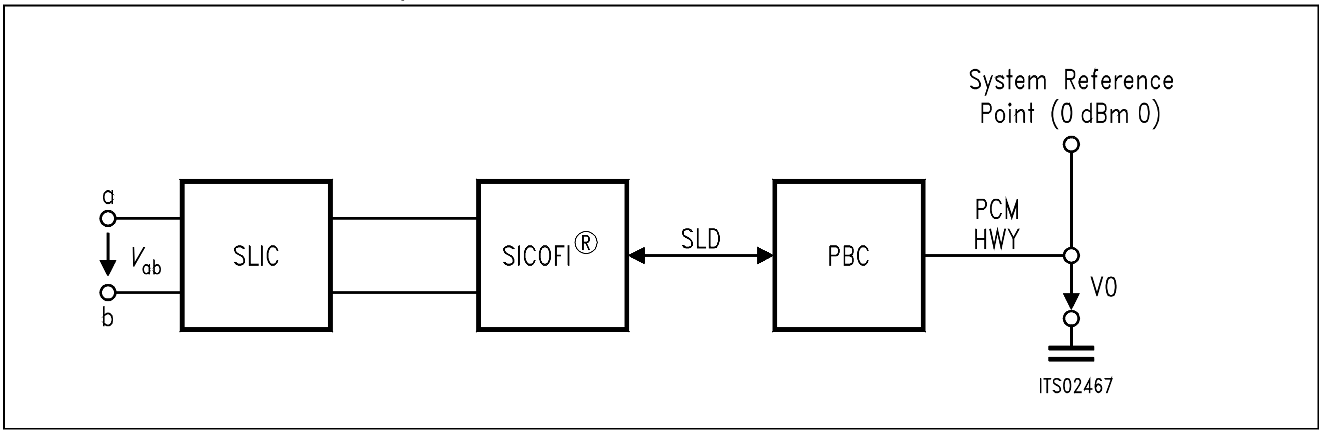


This convention is used in the SICOFI program and has to be applied to the circuit SICOFI-SLIC to determine the correct signs of the variables RLX and RLR.

The circuit SICOFI-SLIC can be described with separated transmit and receive paths as shown below.



Or drawn from another viewpoint:

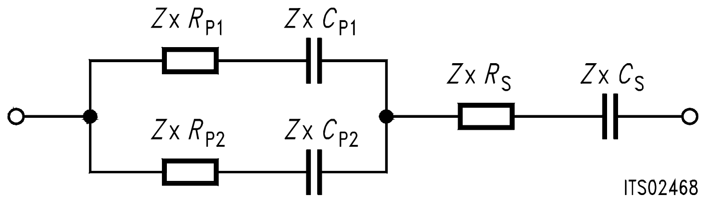


If A is the gain in transmit direction (A = 20 log $\frac{V_0}{V_{ab}}$), then RLX = – A dBr.

If B is the gain in receive direction (B = 20 log $\frac{V_{ab}}{V_0}$), then RLR = + B dBr.

4.3.2 Circuit Library

The impedance used in the SICOFI Coefficient Program are all described in terms of the equivalent circuit diagram shown below:



Impedance Z^* is e.g. Z_I, Z_L, Z_3 or Z_R.

- ZI defines the input impedance which the line card has to present to a,b line.
- ZL is the load impedance used for digital to digital measurements.
- Z3 defines a terminating impedance used for analog to digital and digital to analog measurements when ABIMP = Z3.
- ZR is the reference impedance for calculation of the reference voltage V_{REF} (ZR or V_{REF} may be used to define the reference).

4.3.3 Listing of the SICOFI® Specification File BRD.SPE

```
FREF = 1014.0    LAW = A

VREF = 0.9480    RLX = 0.          RLR =      –7.0

ABIMP = ZI

ZLRP1 = 820.     ZLCP1 = 0.        ZLRP2 = 0.      ZLCP2 = 0.115E-06
ZLRS  = 220.     ZLCS  = 0.
ZIRP1 = 820.     ZICP1 = 0.        ZIRP2 = 0.      ZICP2 = 0.115E-06
ZIRS  = 220.     ZICS  = 0.
Z3RP1 = 820.     Z3CP1 = 0.        Z3RP2 = 0.      Z3CP2 = 0.115E-06
Z3RS  = 220.     Z3CS  = 0.
ZRRP1 = 820.     ZRCP1 = 0.        ZRRP2 = 0.      ZRCP2 = 0.115E-06
ZRRS  = 220.     ZRCS  = 0.

ZRE
FR        300         500         3k          3.4k
AT–       0           20          20            16
AT+      16           20          20             0

ZMIR
FR        4k         12k
AT–      30           3
AT+      30           3

DA,UPPER
FR        300    500  2.7k        3k          3.4k
AT–       100    .75  .25         .35         .75
AT+       .75    .25  .35         .75         100

DA,LOWER
FR        300        3.4k
AT–       0          –.25
AT+       –.25        0

DA,DELAY
FR          500       600         1k          2.6k        2.8k
GD–         10k      .420         .150        .085        .150
GD+        .420      .150         .085        .150         10k

AD,UPPER
FR        300    500  2.7k        3k          3.4k
AT–       100    .75  .25         .35         .75
AT+       .75    .25  .35         .75         100
```

Listing of the SICOFI® Specification File BRD.SPE (cont'd)

```
AD,LOWER
FR         300         3.4k
AT–        0           –.25
AT+       –.25          0

AD,DELAY
FR          500         600         1k          2.6k        2.8k
GD–         10k        .420        .150        .085        .150
GD+        .420        .150        .085        .150         10k
DD
FR         300         500         2.5k        3.4k
AT–         0           27            27       23
AT+        23           27            27        0
```

4.4 Byte File: USER.BYT

This file contains the commands used by the program RS 232 to program the SICOFI Test Board STUT 2060 from the Peripheral Board Controller PBC (**see chapter 5.4**).
The calculated SICOFI coefficients are the same as in the SICOFI-Application: HARRIS SLIC HC 5502.
The table below gives the meaning of the different commands.

Command	Meaning
PSR = 36	Defines the phase shift on PCM Highway between the frame synchronization pulse SYP of the PBC and the PCM time slots.
CAM00 = 41	Assignment of the time slots.
CAM20 = 40	Assignment of the time slots.
CIWO = 26, F4, 80	Deactivates all SICOFI filters.
CIWO = 13, 20, BA, EA, 25, 23, 41, C1, BB	Writes Z filter coefficients 20, BA, EA, 25, 23, 41, C1, BB in SICOFI A of SIP0 line.
CIWO = 23, 50, C8, B5, 4A, C2, 21, 04, 90	Writes X filter coefficients 50, C8, B5, A4, C2, 21, 04, 90
CIWO = 2B, D0, C8, 84, DC, B1, 93, 02, 1D	Writes R filter coefficients D0, C8, 84, DC, B1, 93, 02, 1D
CIWO = 30, A0, 11, 20, 92	Writes GX and GR filter coefficients A0, 11, 20, 92
CIWO = 03, C4, 12, 23, 32, 72, B9, B2, BA	Writes B filter coef. (1st part) C4, 12, 23, 32, 72, B9, B2, BA
CIWO = 0B, 00, 97, FD, C8, DD, 4C, C2, BC	Writes B filter coef. (2nd part) 00, 97, FD, C8, DD, 4C, C2, BC
CIWO = 18, 19, 19, 11, 19	Writes B-Delay filter coefficients 19, 19, 11, 19
SIG0 = C0	Writes signaling byte C0.
CIWO = 26, F4, 78	Activates all SICOFI filters.

4.5 Listing and Description of the RESULT.RES FILE

The following pages comment the contents of the result file HARRIS.RES.

```
Input_file_name: HARRIS.CTL           Date: 31.01.89  15:56
SPEC = BRD.SPE                        SLIC = HARRIS.SLI
BYTE = REF.BYT                        CHNR = 0,A
PLQ  = N
ON = ALL            VERSION = 4.2          SHORT = N
OPT = Z+X+R+B       ZXRB = NNNN            REL = Y
ZAUTO = N           ZREP = N     ZSIGN = 1
FZ =     300.00     3400.0       ZLIM =  2.00
                    PZIN = 11    PSP =   3
FZP =    300.00     500.00    1000.0    1300.0     1500.0
         2000.0     2500.0    2900.0    3000.0     3200.0
         3400.0     7000.0    10000.    14000.
WFZ =    .100        1.00      2.00      1.50       1.00
         3.00        1.00      1.00      1.00       3.00
         2.80        1.00      1.00      1.00
FR =     300.00     3400.0
RDISP = Y           RREFQ = N    RREF = .18639
FX =     300.00     3400.0
XDISP = Y           XREFQ = N    XREF = -6.1268
BAUTO = N           BREP = N     BSIGN = 1
FB =     300.00     3400.0       BLIM =  2.00      BDF = 1
                    PB = 10      GWFB =  .500E-01
FBP =    300.00     500.00    700.00     1000.0    1500.0
         2100.0     2300.0    2900.0     3200.0    3300.0
WFB =    4.0000     2.0000    1.0000     5.0000    1.0000
         2.0000     1.0000    5.0000     1.0000    1.0000
APRE =   .00   DPRE =   .00   APOF =  .00    DPOF = .00
AGX  = 00      AGR  = 00      TM3  = 000
```

Control file section of SICOFI program

```
XZQ =   .16406250E+00  .26757810E+00  .21679690E+00
        .97656250E-01  .13183590E-01
XRQ =   .94531250E+00  .44921880E-01 -.50781250E-01
        .29296880E-02 -.29296880E-02
XXQ =   .15078130E+01  .65625000E+00  .68359380E-01
        .23681640E-01  .48828130E-03
XBQ =  -.11132810E+00 -.35937500E+00  .82031250E-01
        .19531250E+00 -.60607910E-01
       -.80078130E-01  .60058590E-01  .15487670E-01
       -.33691410E-01  .14160160E-01
XGQ =   .57226560E+00  .13046880E+01
```

Quantized values of the optimized coefficients

```
;                                                  Separator to indicate the end of the control file
 Bytes for Z-Filter (13):             60,2B,A3,2B,4B,42,33,22
 Bytes for R-Filter (2B):             F0,29,97,C2,1B,15,0B,BC
 Bytes for X-Filter (23):             70,C8,A5,4D,14,21,02,61
 Bytes for Gain-factors (30):         31,23,20,B2               Hexadecimal codes of the optimized coefficients
 2nd part of bytes B-Filter (0B):     00,C6,D1,24,F6,43,2D,2C   (see *.BYT file)
 1st part of bytes B-Filter (03):     C3,DD,A2,4B,22,1A,BB,BB
 Bytes for B-filter delay (18):       19,19,11,19
* HARRIS SLIC
* VOR = .50000    RIR = 90000.        CKR = .10000E-05
* VOX = 1.0000    RIX = .10000E+06    CKX = .10000E-05          Input file of the SLIC program
* R0  = 600.00

Run #   1
Z-FILTER calculation results
 Reference impedance for optimization:
ZIRP1=   820. ZICP1=   .000 ZIRP2=   0. ZICP2=   .115E-06
ZIRS =   220. ZICS =   .000
 Calculated and quantized coefficients:
XZ  =    .16507    .26725    .21631    .09693    .01324     Optimized coefficients of Z filter
XZQ =    .16406    .26758    .21680    .09766    .01318     Quantized values of the optimized coefficients of Z filter
Bytes for Z-Filter  (13):  60,2B,A3,2B,4B,42,33,22          Hexadecimal codes of the optimized coefficients of Z filter
                                                            Hexadecimal code of the Coefficient OPeration command COP
                                                            used to program the Z filter
RETURN LOSS
FREQ (Hz)      loss (dB)           FREQ (Hz)      loss (dB)
   100.         33.772               2000.         21.902
   200.         31.952               2100.         22.372
   300.         29.816               2200.         22.981
   400.         28.025               2300.         23.756
   500.         26.560               2400.         24.740
   600.         25.362               2500.         25.993
   700.         24.374               2600.         27.601
   800.         23.558               2700.         29.665
   900.         22.886               2800.         32.059
  1000.         22.337               2900.         33.430
  1100.         21.897               3000.         31.760
  1200.         21.555               3100.         28.591
  1300.         21.305               3200.         25.633
  1400.         21.138               3300.         23.126
  1500.         21.052               3400.         21.005
  1600.         21.049               3500.         19.171
  1700.         21.125               3600.         17.558
  1800.         21.290               3700.         16.123
  1900.         21.543               3800.         14.832
```

Theoretical return loss expected to be measured when SICOFI is programmed with the quantized values of the optimized coefficients of Z filter

```
Min. Z-loop reserve:         2.944 dB at frequency:  500.0 Hz
Min. Z-loop mirror reserve: 11.341 dB at frequency: 4000.0 Hz
```

- Minimal reserve in the Z loop
- Minimal reserve of the mirror signal in the Z loop

```
Run #   1
X-FILTER calculation results
 Reference impedance for optimization:
ZIRP1=   820. ZICP1=   .000 ZIRP2=   0. ZICP2=   .115E-06
ZIRS =   220. ZICS =   .000
Calculated and quantized coefficients:
XX  =   1.51053    .65349    .06808    .02365    .00057
XXQ =   1.50781    .65625    .06836    .02368    .00049
Bytes for X-Filter (23): 70,C8,A5,4D,14,21,02,61
```

- XX: Optimized coefficients of X filter
- XXQ: Quantized values of the optimized coefficients of X filter
- 70,C8,A5,4D,14,21,02,61: Hexadecimal codes of the optimized coefficients of X filter
- (23): Hexadecimal code of the coefficient operation command used to program the X filter

```
X-filter attenuation function (in dB),
(always absolute values)
FREQ (Hz) loss (dB) GD (msec) FREQ (Hz) loss (dB) GD (msec)
   100.    -7.059     .048       2000.    -3.933      .009
   200.    -7.030     .047       2100.    -3.675      .006
   300.    -6.982     .047       2200.    -3.411      .003
   400.    -6.915     .046       2300.    -3.143      .000
   500.    -6.830     .045       2400.    -2.869     -.003
   600.    -6.726     .043       2500.    -2.589     -.006
   700.    -6.606     .041       2600.    -2.304     -.009
   800.    -6.469     .039       2700.    -2.014     -.013
   900.    -6.318     .037       2800.    -1.719     -.018
  1000.    -6.151     .035       2900.    -1.420     -.022
  1100.    -5.972     .033       3000.    -1.119     -.028
  1200.    -5.780     .030       3100.     -.818     -.034
  1300.    -5.577     .028       3200.     -.521     -.040
  1400.    -5.364     .025       3300.     -.234     -.047
  1500.    -5.143     .022       3400.      .039     -.054
  1600.    -4.913     .020       3500.      .290     -.061
  1700.    -4.677     .017       3600.      .511     -.068
  1800.    -4.435     .014       3700.      .695     -.074
  1900.    -4.187     .011       3800.      .832     -.078
```

- GD = Group Delay
- Absolute frequency response of the X filter alone (attenuation + group delay). This table is displayed only with the SICOFI control file variable XDISP = Y.

```
GX results:
All attenuation values (in dB) refer to FREF =  1014. Hz
RLX   SLIC+Z   AGX   VREF/VSIC     Xref   TM3    GX
.00 -  3.85 -  .00  -   4.41   -  -6.13 - .00 = -2.32 ideal
.01 =  3.85 +  .00  +   4.41   +  -6.13 + .00 + -2.31 quant
Second byte for Gain:       ,20,B2
```

- 1014. Hz: Reminder of the reference frequency
- ideal: Ideal value of GX starting from the desired value of R_{LX}
- quant: From obtained value of R_{LX} quantized value of GX
- ,20,B2: Hexadecimal code of the optimized coefficient of GX

Calculation of transmit transfer function (AD)
All attenuation values (in dB) refer to FREF = 1014.0 Hz

TGref CA = .232 ms   TGref CB = .245 ms

Group delay in transmit direction (A/D) for the voice channel A and B resp. at the reference frequency FREF.

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
100.	13.831	2.520	2000.	.049	.009
200.	.346	1.784	2100.	.053	.014
300.	.015	.587	2200.	.055	.019
400.	.037	.286	2300.	.057	.025
500.	.034	.164	2400.	.059	.032
600.	.023	.102	2500.	.062	.041
700.	.012	.066	2600.	.066	.051
800.	.003	.043	2700.	.072	.063
900.	–.003	.028	2800.	.081	.076
1000.	–.006	.018	2900.	.095	.092
1100.	–.006	.011	3000.	.113	.112
1200.	–.003	.006	3100.	.137	.136
1300.	.002	.003	3200.	.171	.166
1400.	.008	.001	3300.	.218	.207
1500.	.016	.000	3400.	.291	.260
1600.	.024	.000	3500.	.412	.337
1700.	.031	.001	3600.	.640	.455
1800.	.038	.003	3700.	1.145	.648
1900.	.044	.006	3800.	2.476	.984

Frequency response in transmit direction (A/D) of the set SICOFI+SLIC+external circuitry.
These are the theoretical values expected to be measured when SICOFI is programmed with the quantized values of the optimized coefficients of X filter.

```
Run #   1
R-FILTER calculation results
 Reference impedance for optimization:
ZIRP1=   820. ZICP1=   .000 ZIRP2=   0. ZICP2=   .115E-06
ZIRS =   220. ZICS =   .000
 Calculated and quantized coefficients:
XR  =    .94728    .04531   -.05067    .00264   -.00258
XRQ =    .94531    .04492   -.05078    .00293   -.00293
Bytes for R-Filter (2B): F0,29,97,C2,1B,15,0B,BC
```

- XR line: Optimized coefficients of R filter
- XRQ line: Quantized values of the optimized coefficients of R filter
- F0,29,97,C2,1B,15,0B,BC: Hexadecimal codes of the optimized coefficients of R filter
- (2B): Hexadecimal code of the COP-command used to program the R filter

R-filter attenuation function (in dB),
(always absolute values)

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
100.	.537	-.008	2000.	.052	.011
200.	.522	-.007	2100.	.078	.011
300.	.497	-.006	2200.	.113	.011
400.	.465	-.005	2300.	.156	.011
500.	.425	-.003	2400.	.208	.010
600.	.381	-.002	2500.	.269	.009
700.	.334	.000	2600.	.339	.008
800.	.286	.002	2700.	.418	.006
900.	.238	.003	2800.	.505	.004
1000.	.192	.005	2900.	.600	.002
1100.	.151	.006	3000.	.701	-.000
1200.	.113	.008	3100.	.807	-.003
1300.	.082	.009	3200.	.915	-.006
1400.	.056	.009	3300.	1.022	-.009
1500.	.037	.010	3400.	1.126	-.013
1600.	.025	.011	3500.	1.222	-.016
1700.	.021	.011	3600.	1.307	-.019
1800.	.023	.011	3700.	1.378	-.021
1900.	.034	.011	3800.	1.431	-.023

Absolute frequency response of the R filter alone (attenuation + group delay).
This table is displayed only with the SICOFI control file variable *R*DISP = Y.

```
GR results:
All attenuation values (in dB) refer to FREF =  1014. Hz
-RLR    SLIC+Z     AGR    VSIC/VREF    Rref     GR
7.00  -  6.38   -  .00  -   -4.41  -    .19  =  4.84  ideal
7.01  =  6.38   +  .00  +   -4.41  +    .19  +  4.85  quant
First byte for Gain (30) :        31,33
```

- 1014. Hz: Reminder of the reference frequency
- ideal line: Ideal value of GR starting from the desired value of *R*LR
- quant line: From obtained value of *R*LR quantized value of GR
- 31,33: Hexadecimal code of the optimized coefficient of GR

Calculation of receive transfer function (DA)
All attenuation values (in dB) refer to FREF = 1014.0 Hz

TGref CA = .235 ms   TGref CB = .218 ms

Group delay in transmit direction (D/A) for the voice channel A and B resp. at the reference frequency FREF.

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
100.	.059	.011	2000.	.047	.041
200.	.056	.001	2100.	.050	.048
300.	.050	.000	2200.	.052	.055
400.	.042	.000	2300.	.053	.062
500.	.034	.001	2400.	.053	.071
600.	.025	.002	2500.	.054	.081
700.	.017	.004	2600.	.055	.092
800.	.010	.005	2700.	.058	.106
900.	.006	.007	2800.	.063	.121
1000.	.003	.009	2900.	.071	.139
1100.	.003	.011	3000.	.084	.161
1200.	.005	.013	3100.	.105	.188
1300.	.008	.015	3200.	.136	.221
1400.	.013	.018	3300.	.185	.264
1500.	.019	.021	3400.	.267	.321
1600.	.026	.024	3500.	.408	.401
1700.	.033	.028	3600.	.671	.522
1800.	.038	.032	3700.	1.231	.718
1900.	.043	.036	3800.	2.640	1.056

Frequency response in transmit direction (D/A) of the set SICOFI+SLIC+external circuitry.
These are the theoretical values expected to be measured when SICOFI is programmed with the quantized values of the optimized coefficients of R filter.

```
Run #   1
B-FILTER calculation results
Reference impedance for optimization:
ZLRP1=   820. ZLCP1=   .000 ZLRP2=   0. ZLCP2=   .115E-06
ZLRS =   220. ZLCS =   .000
Calculated and quantized coefficients:
XB  =   -.11222   -.35881    .08265    .19353   -.06063
        -.08070    .05988    .01549   -.03382    .01419
XBQ =   -.11133   -.35938    .08203    .19531   -.06061
        -.08008    .06006    .01549   -.03369    .01416
2nd part of bytes B-Filter (0B) :  00,C6,D1,24,F6,43,2D,2C
1st part of bytes B-Filter (03) :  C3,DD,A2,4B,22,1A,BB,BB
```

- XB: Optimized coefficients of B filter
- XBQ: Quantized values of the optimized coefficients of B filter
- 00,C6,D1,24,F6,43,2D,2C: Hexadecimal codes of the second part of the optimized coefficients of B filter
- C3,DD,A2,4B,22,1A,BB,BB: Hexadecimal codes of the first part of the optimized coefficients of B filter
- (0B): Hexadecimal code of the COP-command used to program the second part of B filter
- (03): Hexadecimal code of the COP-command used to program the first part of B filter

TRANS HYBRID LOSS

FREQ (Hz)	loss (dB)	FREQ (Hz)	loss (dB)
100.	48.629	2000.	45.730
200.	39.496	2100.	46.340
300.	42.330	2200.	47.186
400.	45.483	2300.	48.631
500.	48.880	2400.	50.950
600.	52.046	2500.	53.760
700.	53.650	2600.	57.230
800.	53.233	2700.	61.328
900.	52.387	2800.	61.702
1000.	51.862	2900.	59.872
1100.	51.637	3000.	57.133
1200.	51.332	3100.	53.136
1300.	50.575	3200.	49.168
1400.	49.624	3300.	45.697
1500.	48.489	3400.	42.616
1600.	47.357	3500.	40.181
1700.	46.503	3600.	38.344
1800.	45.826	3700.	37.331
1900.	45.592	3800.	38.242

Trans hybrid loss table: Theoretical transhybrid loss expected to be measured when SICOFI is programmed with the quantized values of the optimized coefficients of B filter.

Note: Theoretical values of the transhybrid loss greater than 40 dB are only calculated but may not be measurable exactly!

```
Additonal B-filter delay (in seconds):   .625E-04
Bytes for B-filter delay (18) :  19,19,11,19
```

- .625E-04: Value of the delay of B filter
- 19,19,11,19: Hexadecimal code of the B-delay filter coefficients
- (18): Hexadecimal code of the COP-command used to program the B-delay filter

5 Using the Software Packet

Note: To aid comprehensibility the following symbol < > has been introduced.
Any text enclosed within this symbol has to be typed from the PC keyboard.

5.1 Installation of SICOFI® Software

The SICOFI program STS 2060 requires the following environment:

– an IBM-AT Personal Computer or compatible running MS-DOS Version 3.0 or later
– a coprocessor 80287
– 640 Kbyte RAM available memory
– 1.2 Mbyte floppy disk drive
(on request the program can be provided for a 360 Kbyte floppy disk drive)

Note: CONFIG.SYS file has to include:
SET BUFFERS = 20
SET FILES = 20
DEVICE = ANSI.SYS
Various files and buffers are opened by the program. The program automatically closes them with the command EXIT.

Having assembled all the necessary material you can start working with the program:

Insert the SICOFI disk in drive A.

Change to drive A: <a:>
Call the installation program: <setup>

The program SETUP creates the directories C:\SICOFI and C:\SICOFI\DOC on drive C (hard disk).

The tables on the next page show which files will be copied by the program SETUP into each directory.

Warning: The program SETUP will overwrite any existing files.

Directory of C:\SICOFI	File contents
SICOFI.BAT	running batch file using SICO.EXE
SICO.EXE	SICOFI execution program
HARRIS.FOR	source file of HARRIS SLIC program written in FORTRAN
HARRIS.EXE	SLIC execution program of HARRIS SLIC
HARRIS.INP	input file of HARRIS.EXE
HARRIS.SLI	output file of HARRIS.EXE
HARRIS.CTL	control file of SICOFI program when calculating coefficients for SICOFI-HARRIS SLIC applications
HARRIS.RES	result file of SICOFI coefficients calculation for HARRIS SLIC
TRAFOS.FOR	source files of transformer SLIC
TRAFOT.FOR	programs with series or transverse feeding written in FORTRAN
TRAFOS.EXE	SLIC execution programs of transformer
TRAFOT.EXE	SLIC of the SICOFI User Board STU 2060
TRAFOS.INP	input file of TRAFOS.EXE
TRAFOT.INP	input file of TRAFOT.EXE with series or transverse feeding
TRAFOT.SLI	output file of transformer SLIC program
TRAFO.CTL	control file of SICOFI program when calculating coefficients for SICOFI-transformer SLIC applications
BRD.SPE	specification file for Germany
REF.BYT	reference byte file (USER.BYT)
BRD1.SPE	modified specification file for Germany
BRD1.IMP	impedance file
SICOAUTO.BAT	SICOFI BATCH program
MODE.CTL	SICOFI BATCH MODE file
BATCH.CTL	SICOFI BATCH CONTROL file
MARK.COM	mark current memory position
RELEASE.COM	release memory above last mark
RS232.EXE	RS232 Interface Program

C:\SICOFI\DOC	File contents
SYSTEM.HLP	System Environment
MENU.HLP	Menu Help
SLIC1.HLP - SLIC6.HLP	SLIC
SICO1.HLP - SICO8.HLP	SICOFI
GX.HLP	Table of SICOFI Gain GX
GR.HLP	Table of SICOFI Attenuation GR
CTL.HLP	Control file
SPE.HLP	Specification file
BYT.HLP	Programming byte file
LEVEL.HLP	Level
IMPED.HLP	Impedance definition
FEATURE.HLP	Features of SICOFI version V 3.0
APPLIC.HLP	Available SICOFI / SLIC applications
TEXTOUT.SIC	SICOFI program output text
ERROROUT.SIC	SICOFI program error text

The following SLIC programs are also available on request:

SGS.EXE execution program of SGS-THOMSON SLIC L3030 + L3000
NSGS.EXE execution program of SGS-THOMSON SLIC L3090 + L3000
ERIC.EXE execution program of ERICSSON SLIC PBL 3762

A READ.ME file is available on the floppy disk.

To modify the SLIC part of the program, the following is necessary:

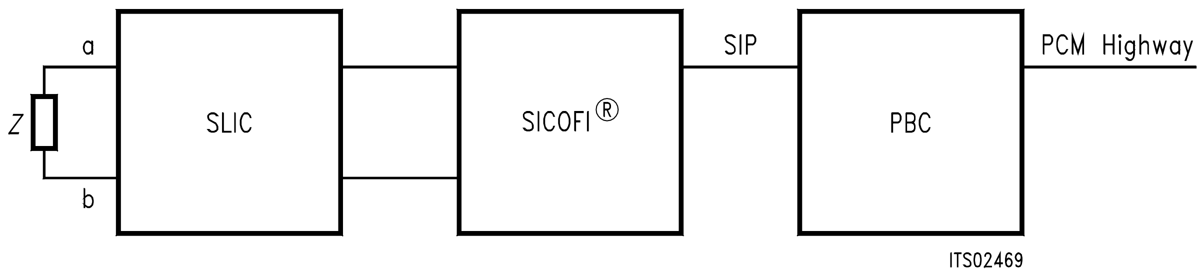
– an editor
– a compiler (e.g. MICROSOFT FORTRAN COMPILER advised, IBM professional FORTRAN compiler PROFORT, RMFORT ...)

  Note: our SLIC programs have been compiled using MICROSOFT compiler
– a linker (e.g. MICROSOFT, PROFORT, PLINK86 ...)

To start the program, type: <SICOFI>

5.2 STS 2060 Main Menu

Siemens AG., Components Group, HL IT PD 22
Authors: Mr. Kliese, Mr. Glasser Tel.: 089/4144-3662



Subsciber Line Module Analog

1 SLIC Calculation
2 SICOFI Program
3 RS 232 SICOFI Programming
4 EXIT

Enter your selection:

<1>: you calculate the model of your SLIC (see chapter 5.3).
<2>: you start the SICOFI program (see chapter 5.5).
<3>: you initialize the RS 232 interface in order to program the SICOFI Test Board from your PC (see chapter 5.4).
<0>: you leave the STS 2060 software packet to return to MS-DOS.

5.3 STS 2060 SLIC Menu

```
1 HARRIS SLIC HC 5502 / 5504
2 Transformer SLIC with Series Feeding
3 Transformer SLIC with Transverse Feeding
4 SGS - Thomson SLIC L3030 / L3000
5 SGS - Thomson SLIC L3090 / L3000
6 ERICSSON SLIC PBL 3736 / AMD 7950
7 ERICSSON SLIC PBL 3762
8 USER SLIC
0 EXIT To Main Menu
```

Enter your selection:

<1>, ... or <7>: the model of the indicated SLIC will be calculated and the corresponding M-parameters will be generated and written in a file (named by yourself) "***.SLI".

<8>: you have written your own SLIC routine. This routine has to be named "USER.EXE". This routine has to generate the M-parameters or K-parameters and to write them to a file named "***.SLI".

<0>: you return to the STS 2060 main menu.

5.4 STS 2060 RS 232 Menu

The program RS 232 uses the ***.BYT file to program the SICOFI Test Board STUT 2060.

This Test Board has to be connected to the PORT COM1.

The contents of the ***.BYT file is sent through the PORT COM1 via the interface RS 232 to the Test Board (**see chapter 4.4 Byte file: USER.BYT**).

```
RS 232 Program V 1.0                           Siemens HL IT PD 22
9600 Baud, 8 bit, no Parity Bit and one Stop Bit at Port COM1

(1) File Definition                (2) File Programming
(3) Terminal Programming           (0) END RS232 Programming
```

INPUT: 1

Please enter input file name: REF.BYT

⇒ Programming input file: REF.BYT

Enter your selection:

<1>: you declare which ***.BYT file you want to use to program the SICOFI Test Board.

<2>: the ***.BYT file has already been declared. The programming of the SICOFI Test Board can start immediately.

<3>: The SICOFI Test Board is programmed directly from the PC keyboard (without using any ***.BYT file).

<0>: you return to STS 2060 main menu.

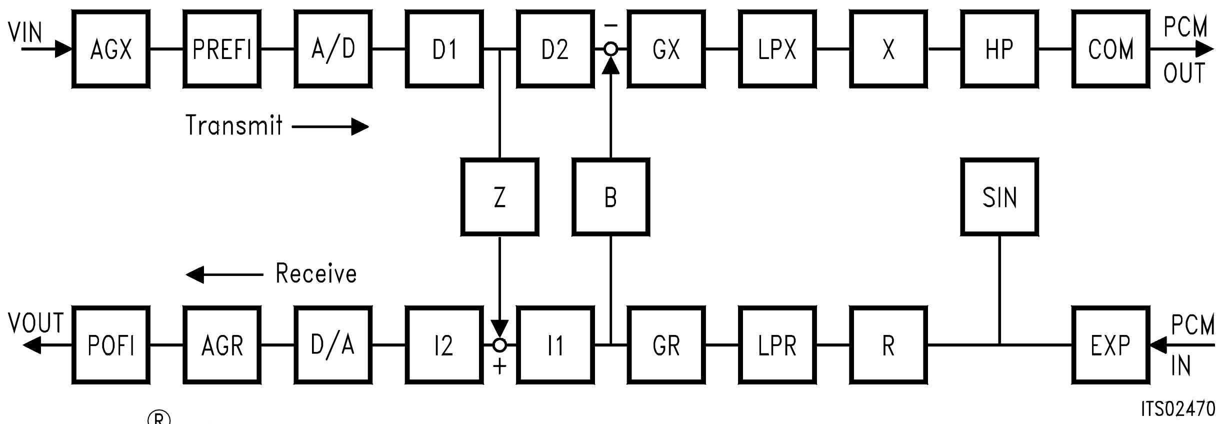
Note: If you have used the command <3>, the command <Q> will bring you back to the above menu.

5.5 Using SICOFI® Program

Before starting the SICOFI program you must check:

- at least one control file "***.CTL" exists in the working directory.
- the specification file "***.SPE" and the SLIC transfer file "***.SLI" respectively declared by the control file variables SPEC and SLIC exist in the working directory.

```
Siemens AG., Components Group, HL IT PD 22
Authors: Mr. Kliese, Mr. Glasser Tel.: 089/4144-3662
```



SICOFI® V4.x Signal Flow Graph

```
Enter control file name: <***.ctl>
Reading SICOFI control file  ...  ***.CTL
Reading SLIC parameter file  ...  ***.SLI
Reading specification file   ...  ***.SPE
1 Disp 2 DATA 3 Opt 4 Sim 5 Byt 6 Res 7 Echo 8 Help 9 DOS 0 EXIT
```

5.6 STS 2060 SICOFI® Menu

At this point different commands are accessible. These commands can be choosen by typing the number or moving the cursor up to the desired command.

<1> or DISP:

Using this command you can display the current control file on the PC screen.
If you change the value of a variable (command DATA), this will be taken into account by the next display.
To display other files of the working directory, refer to the command DOS.

<2> or DATA:

Using this command you can change the value of a variable. How to proceed?

Type: <variable name><separator><new value><RETURN>

The possible separators are: < > <,> < = > <*> <%> <$> <!>
Several variables may be changed at the same time.

If the value of a variable corresponding to a file name (e.g. SPEC) is changed, not only the change will be taken into account but also the contents of the file will be automatically read and available for the SICOFI program.

To facilitate the declaration of the particular values of a variable the program offers the possibility to abbreviate the power of ten factor using the following conventions:

P	corresponds to pico (1.0 E - 12)
N	corresponds to nano (1.0 E - 09)
U	corresponds to micro (1.0 E - 06)
M	corresponds to milli (1.0 E - 03)
K	corresponds to kilo (1.0 E + 03)
MEG	corresponds to mega (1.0 E + 06)
G	corresponds to giga (1.0 E + 09)

e.g.
```
OPT = X + R
SIM = ALL
ZAUTO = Y
FX = 300,3.2k
```

<3> or OPT:

Using this command the program will optimize, automatically or not (see variables ZAUTO and BAUTO), the coefficients of the filters indicated by the variable OPT.

Note: The coefficient of the GR filter is automatically calculated together with those of the R filter.
The coefficient of the GX filter is automatically calculated together with those of the X filter.
The coefficient of the B-delay filter is automatically calculated together with those of the B filter.

Once obtained each coefficient is quantized to the closest value programmable at the SICOFI.
Assuming the SICOFI is now programmed with the quantized coefficients, the program calculates the theoretical transfer functions of the set SICOFI-SLIC (taking into account which filters are switched on and which are switched off; see variables ON/OFF).

The table below shows which transfer function is calculated after which coefficient optimization:

optimized coefficients	calculated transfer functions
Z filter	Return loss
R filter	Transfer function in receive direction (4-wire to 2-wire). R filter absolute frequency response (if RDISP = Y)
X filter	Transfer function in transmit direction (4-wire to 2-wire). X filter absolute frequency response (if XDISP = Y)
B filter	Transhybrid loss

<4> or SIM:

Using this command the program will simulate the absolute or relative (see variable REL) transfer functions or the set SICOFI-SLIC indicated by the variable SIM. These transfer functions may be checked by measurements (taking into account which filter is switched on and which one is switched off; see variables ON/OFF).

The diagram and table below show the meaning of each transfer function that can be simulated:

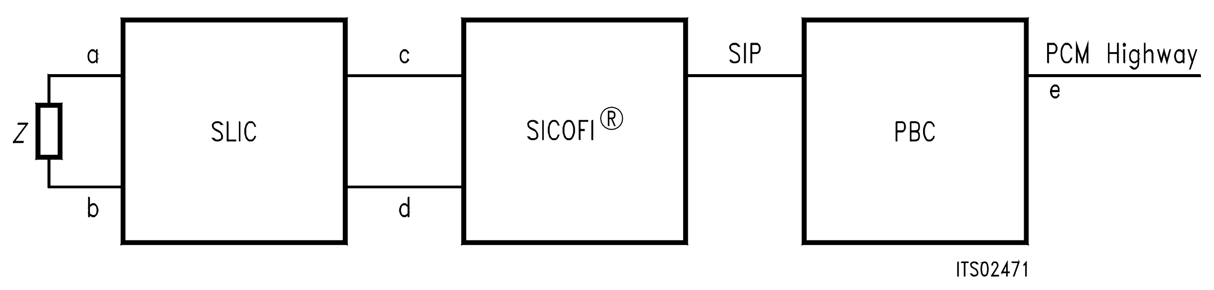


Figure 11
Definition of Transfer Functions

Transfer Function:	Equivalent Measurement:
ZRE: return loss	at a,b (Z = ZIN)
ZIN: input impedance	at a,b
AD: analog to digital	a,b to e
DA: digital to analog	e to a,b
DD: digital to digital	e to e via a,b (Z = ZL)
ASI: analog to SICOFI input	a,b to c
ASO: analog to SICOFI output	a,b to d (Z-filter on)
DSI: digital to SICOFI analog input	e to c via a,b (Z = ZL or Z = ZI)
DSO: digital to SICOFI analog output	e to d

When the variable REL of the control file is "N", the program calculates absolute attenuation values.
With the REL variable of the control file set "Y", the program displays relative values normalized to the frequency FREF.

<5> or BYT:

Using this command the program takes the file declared under the variable BYTE as reference file and interchanges the coefficients written in this file with those calculated by the SICOFI program.
Using the command BYT the program asks for a new ***.BYT file name.
This new file can then be used with the program RS 232 to program the SICOFI Test Board.

<6> or RES:

Using this command you can store the results of the last SICOFI coefficient calculation in a file which name may be defined by yourself.
The result file is described in chapter 4.5.
To have a complete documentation of the transfer functions and coefficients, all SICOFI filters should be switched on (OPT = ALL or OPT = Z + R + X + B) in the last calculation.

<7> or ECHO:

Using this command under the current directory a file is created in which everything appearing on the PC screen is stored.
To close the echo file type ECHO once again.
After a session you may print the echo file for documentation purposes.

<8> or HELP:

Using this command you may access the program documentation without leaving the SICOFI program.

<9> or DOS:

Using this command you can work with the DOS of your PC. All the usual DOS commands are available (DIR, RENAME, TYPE, ...). After having used this command you automatically return to the SICOFI menu.

<0> or EXIT:

Using this command you return to the STS 2060 main menu.

6 Example: How to Obtain SICOFI® Coefficients for a Special SLIC Application

6.1 Calculation of M-Parameters for HARRIS SLIC

The following chapter gives an example showing how to obtain the optimized SICOFI coefficients for an application using the HARRIS SLIC HC 5508. The specifications to be fulfilled are those of the "Deutsche Bundespost".

Figure 12 shows in the upper part a simplified block diagram of the HARRIS SLIC HC 5508 and in the lower part the architecture which is taken from the datasheet.

In **figure 13** you see the connection of the HARRIS SLIC to the SICOFI. In the two blocks AX and AR with external interface components capacitors C_{CX} and C_{CR} decouple a DC offset. Because the SICOFI input impedance is very high (MΩ), we then also need the resistor R_{IX} in transmit path to have a defined high pass and time constant. In our application we take C_{CX} = C_{CK} = 1 µF, R_{IX} = 100 kΩ and VOX = VOR = 1.

To gain the transfer function of the SLIC and its external interface components, it is necessary first to derive the M-Parameter as described in **chapter 3.1**.

The user then has to write a SLIC program which calculates the M-Parameters. With his SLIC program he generates a M-Parameter table of the SLIC like the table in **chapter 3.3**.
The name of the M-Parameter output file may be HARRIS1.SLI and is used for an input file to the SICOFI coefficients program.

Next a SICOFI control file like HARRIS.CTL, which is listed on **chapter 4.2.1**, has to be edited. You have to update the "SLIC = HARRIS.SLI" to "SLIC = HARRIS1.SLI".

Now you may calculate the SICOFI coefficients as described in **chapter 6.2**.

The results are stored in a result file HARRIS1.RES which is described in **chapter 4.5**.

a) Derivation of the equations of the M-parameters:

In the following equations, AX and AR are the transfer function factors of the two blocks. With the factor K = 1000 we get:

$$I_1 = \frac{(V_1 - V_0)}{(2 \times R_F)} \tag{1}$$

$$V_0 = -V_m + \frac{V_m \times K \times Z_0}{K \times 2 \times R_F} - 2 \times AR \times V_3 \tag{2}$$

$$V_0 = -(V_1 - V_0) + \frac{(V_1 - V_0) \times K \times Z_0}{K \times 2 \times R_F} - 2 \times AR \times V_3 \tag{3}$$

$$\frac{(V_1 - V_0) \times K \times Z_0}{K \times 2 \times R_F} = \frac{(V_1 - V_0) \times Z_0}{2 \times R_F} = V_1 + 2 \times AR \times V_3 \tag{4}$$

with (1) and (4)

$$I_1 \times Z_0 = V_1 + 2 \times AR + V_3 \tag{5}$$

$$V_2 = -AX \times (V_1 - V_0) + \frac{K \times Z_0}{K \times 2 \times R_F} = -AX \times (V_1 - V_0) \quad \frac{Z_0}{2 \times R_F} \tag{6}$$

Conclusions:

$$M11 = \frac{I_1}{V_1} = \frac{1}{Z_0} \qquad \text{with } V_3 = 0 \tag{7}$$

$$M12 = \frac{I_1}{V_3} = \frac{2 \times AR}{Z_0} \qquad \text{with } V_1 = 0 \tag{8}$$

with V_3 = 0 and (5)

$$V_1 = I_1 \times Z_0 \tag{9}$$

$$M21 = \frac{V_2}{V_1} = \frac{-AX \times (V_1 - V_0)}{2 \times R_F \times I_1} = -AX \tag{10}$$

with (6), (9) and (1)

$$V_3 = \frac{(V_1 - V_0) \times Z_0}{2 \times AR \times 2 \times R_F} \qquad \text{with (4)} \tag{11}$$

$$M22 = \frac{V_2}{V_3} = -2 \times AX \times AR \times \text{with } V_1 = 0 \text{ and (6), (11)} \tag{12}$$

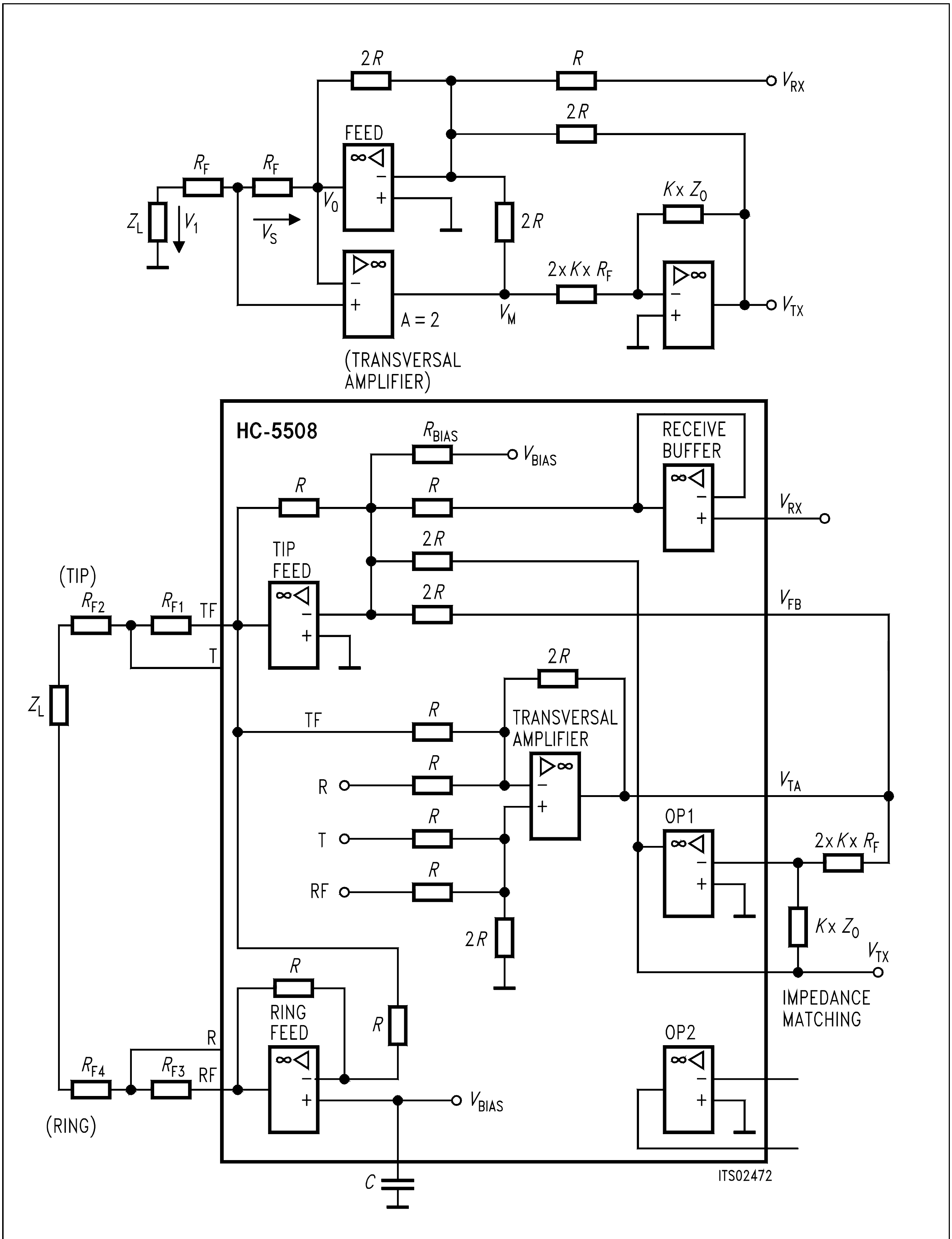


Figure 12
Internal Architecture of HARRIS SLIC HC 5508/09

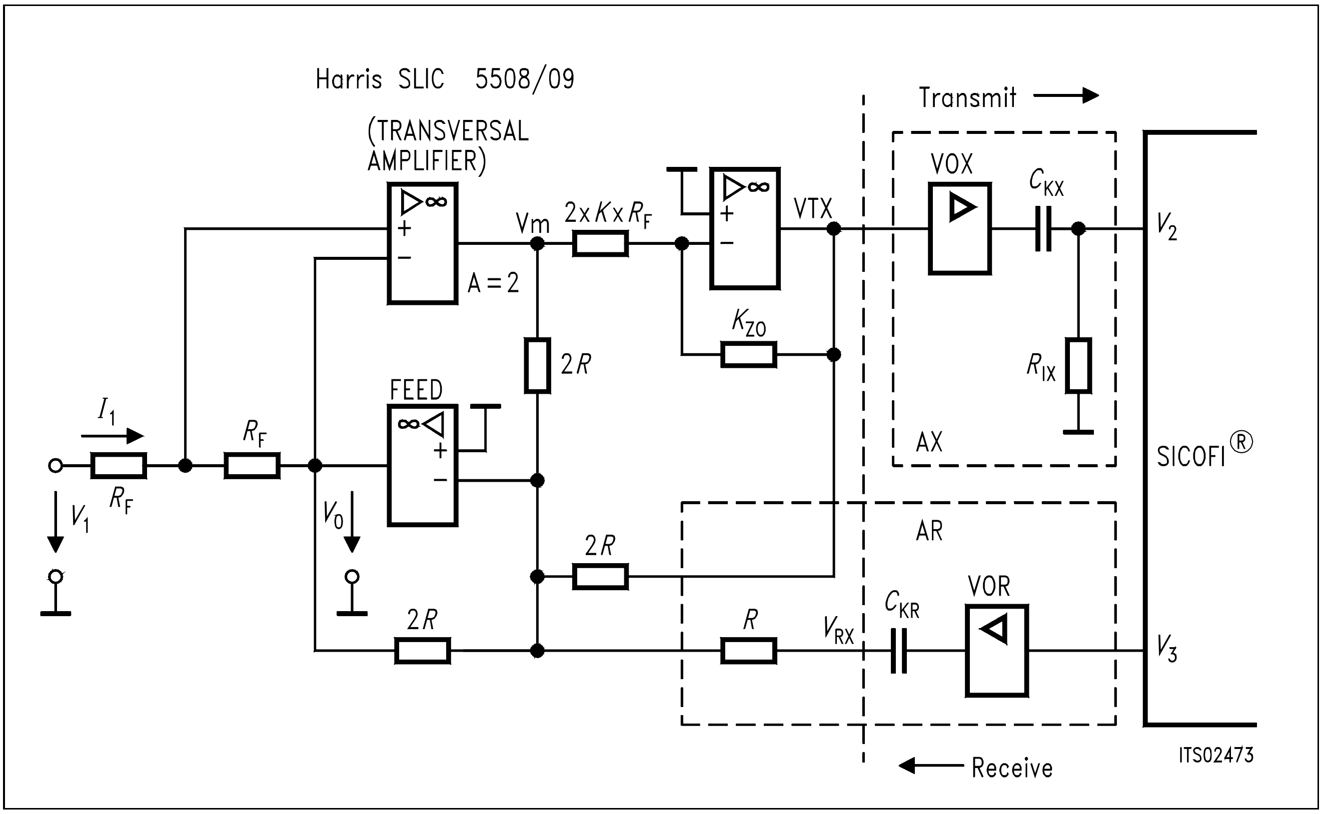


Figure 13
Connection of HARRIS SLIC HC 5508/09 with SICOFI®

6.2 Working Method for Calculating SICOFI® Coefficients

The aim of this chapter is to give you some hints to take advantage of the flexibility of the STS 2060 software.

– The SICOFI is a CODEC filter which enables you to have only a single SLIC circuit for different application purposes (e.g. different countries).

  The SLIC circuit has to be optimized first in order to use the SICOFI filters in their optimum working range (optimum use of the filters). For this aim you start in calculating the Z filter coefficients for the different applications. Modify the values of the different SLIC parameters in order to obtain the best compromise.

Then the SLIC parameters are frozen and, using the automatic calculation of the Z filter (ZAUTO = Y), the Z filter coefficients are optimized.

Subsequently the R (GR) and/or X (GX) filter coefficients are optimized.

Only then the B filter coefficients may be optimized in the automatic mode (BAUTO = Y).

Due to the architecture of the SICOFI, the filter coefficients have to be calculated in the sequence described above.

– Several specification files can be prepared before using the program in order to proceed more quickly during the calculation of the coefficients for different applications. Indeed only the file name declared with the variable SPEC needs to be changed to restart the calculation without leaving the SICOFI program.

7 Extended SICOFI® Calculation Features

7.1 Special Variables in the Control File

The values of these variables in general do not need to be changed during the optimization of the coefficients. They can be modified however to help you to advance in the optimization process if satisfactory results have not yet been achieved. If not adversely noted, variables may be changed during a session (command DATA).

ZMIR

Abbreviation meaning: Z-loop MIRror signal mask

Function: defines the mask of the Z-loop mirror signal. In calculating the Z filter coefficients the SICOFI program checks that the convolution effects due to the decimation and interpolation filters are really negligible as they should be.

Value: FR in Hz, AT- and AT+ in dB

RREFQ

Abbreviation meaning: RREF flag question

Function: indicates whether the R filter frequency response will be automatically optimized or calculated according to the value defined by RREF (see below).

Value: Y (according to RREF) or N (automatically).

RREF

Abbreviation meaning: R filter attenuation at REference Frequency

Function: indicates the value of the R filter attenuation at the reference frequency FREF when RREFQ = Y.

Value: in dB.

XREFQ

Abbreviation meaning: XREF flag question

Function: indicates whether the X filter frequency response will be automatically optimized or calculated according to the value defined by XREF (see below).

Value: Y (according to XREF) or N (automatically).

XREF

Abbreviation meaning: X filter attenuation at REference Frequency

Function: indicates the value of the X filter attenuation at the reference frequency FREF when XREFQ = Y.

Value: in dB.

ZLIM

Abbreviation meaning: Z filter coefficient LIMit

Function: indicates the limit of Z filter coefficient values during the automatic optimization (ZAUTO = Y).

Value: REAL value < 3.0.

Practical use: The variable ZLIM influences the precision of the quantization of the Z filter coefficients. By modifying the value of ZLIM you can decrease the quantization error.

ZLIM is the limit of the scale used to quantize the coefficients. The recommended value is 2. It can be set to a larger value in order to expand the scale but the actual coefficients should NOT be larger than 3.

ZSIGN

Abbreviation meaning: Z filter optimization SIGN

Function: indicates whether the automatic optimization of Z filter coefficients will be as far as possible from or as close as possible to the defined return loss specification ZRE.

Value: 1 (far) or – 1 (close).

Practical use: Valid only when ZAUTO = Y.

BLIM

Abbreviation meaning:	B filter coefficient LIMit
Function:	indicates the limit of B filter coefficient values during the automatic optimization (BAUTO = Y).
Value:	REAL value < 3.0.
Practical use:	The explanation concerning the variable ZLIM applies to BLIM accordingly.

BSIGN

Abbreviation meaning:	B filter optimization SIGN
Function:	indicates whether the automatic optimization of B filter coefficients will be as far as possible from or as close as possible to the defined transhybrid loss specification DD.
Value:	1 (far) or – 1 (close).
Practical use:	Valid only when BAUTO = Y.

DPRE, DPOF, APOF, APRE:

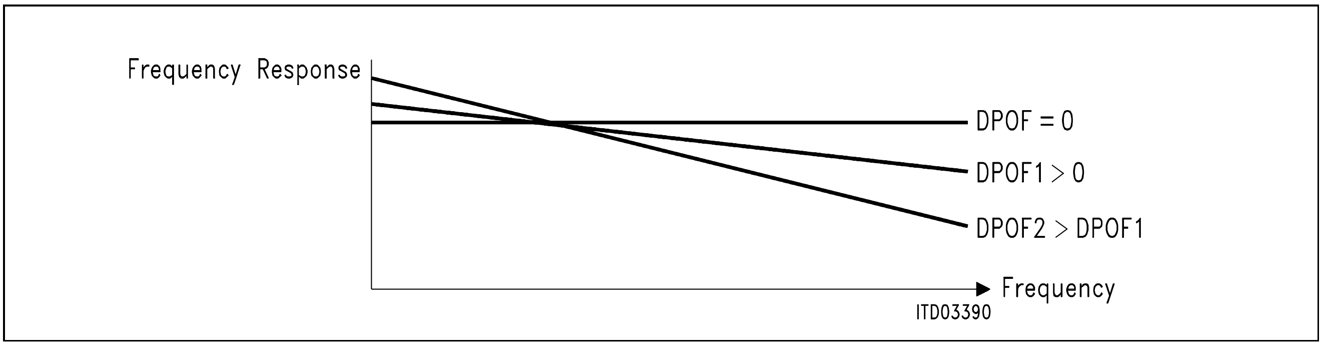
When the SLIC has not been correctly modelled, the simulated frequency responses of the circuit SICOFI-SLIC may greatly differ from the measured ones.

The variables DPRE, DPOF, APOF, APRE introduce some fictive delays or attenuations respectively to allow the user to correct any failure in the SLIC model.

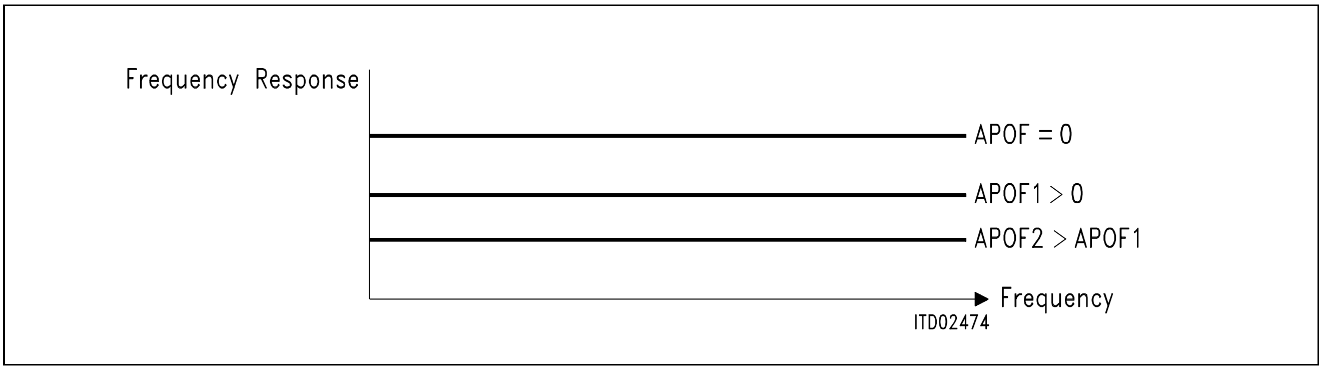
The optimum values of these variables are obtained experimentally; the influence of these variables however can be roughly described as follows:

Positive values of the variables DPRE and DPOF cause a deterioration of the frequency response in the high frequency band.

Positive values of the variables APRE and APOF cause a deterioration of the frequency response in the whole speech band (see diagram below).



This diagram is also valid for DPRE.



This diagram is also valid for APRE.

7.2 Special Variables in the Specification File

In the specification file some impedance like the input impedance Z_I, load impedance Z_L, terminating impedance Z_3 and the reference impedance Z_R are defined. These impedances are described in terms of the equivalent circuit diagram shown in **chapter 4.3**.

In special cases like the British Telecom it is necessary to calculate more complex impedance schemes which cannot be described using our impedance library. Therefore we introduce the additional feature of reading a defined complex impedance table from a file.

If the equivalent circuit of the impedance Z_I, Z_L, or Z_3 is not defined in the specification file, the SICOFI program searches for the keywords 'ZI', 'ZL' or 'Z3' with an assignment of the name of an impedance file *.IMP.

If you want to use these complex impedances you may write a small program written in any programming language which calculates the impedance in the range of 10 Hz – 4000 Hz in steps of 10 Hz. A listing of the specification file BRD1.SPE using these special variables is given below.

7.2.1 Listing of the Specification File BRD1.SPE with Special Variables

```
FREF  =  1014.0    LAW  =  A
VREF  =  0.9480    RLX  =  0.     RLR  =  -7.0
ABIMP  =  ZI
ZL  =  BRD1.IMP
ZI  =  BRD1.IMP
Z3  =  BRD1.IMP
ZRE
FR            300      500       3k        3.4k
AT-           0        20        20          16
AT+          16        20        20           0
ZMIR
FR            4k       12k
AT-          30         3
AT+          30         3
DA,UPPER
FR           300       500       2.7k      3k        3.4k
AT-          100       .75       .25       .35       .75
AT+          .75       .25       .35       .75       100
DA,LOWER
FR           300       3.4k
AT-          0         -.25
AT+          -.25       0
DA,DELAY
FR            500       600       1k       2.6k      2.8k
GD-           10K      .420      .150      .085      .150
GD+          .420      .150      .085      .150       10K
AD,UPPER
FR           300       500       2.7k      3k        3.4k
AT-          100       .75       .25       .35       .75
AT+          .75       .25       .35       .75       100
AD,LOWER
FR            300      3.4k
AT-           0        -.25
AT+          -.25       0
AD,DELAY
FR            500       600      1k        2.6k      2.8k
GD-           10K      .420      .150       .085     .150
GD+          .420      .150      .085       .150      10K
DD
FR           300       500       2.5k      3.4k
AT-           0         27         27      23
AT+          23         27         27       0
```

7.2.2 Format of the Impedance File *.IMP

This file contains an impedance table, which is defined in the actual specification file and may be read by the SICOFI coefficients program.

The impedance file has the following standard form:

1. '*' at the first position of a line means a comment that the SICOFI program will not use for calculations. Such lines are only for documentation purposes.

2. The SICOFI program looks for the values of FREQUENCY, REAL PART and IMAGINARY PART of the calculated impedance.

```
* BRD.SPE : RP1  =  820, CP2  =  115E-09, RS  =  220.
*   FREQ              REAL                 IMAG
  10.000000       1039.971000           -4.858366
  20.000000       1039.885000           -9.715708
  30.000000       1039.741000          -14.571000
  .........         ..........          ..........
  .........         ..........          ..........
 990.000000        830.084800         -357.863200
1000.000000        826.930200         -359.608800
1010.000000        823.776800         -361.317800
1020.000000        820.625100         -362.990500
...........         ..........          ..........
...........         ..........          ..........
3980.000000        344.981800         -294.728100
3990.000000        344.451100         -294.213900
4000.000000        343.923500         -293.701000
```

7.3 K-Parameters

It has been found that from mathematical reasons the M-parameters cannot always be used to model a SLIC. That happens with the Ericsson SLIC. Furthermore the M-parameters are not easy to be measured. Therefore we developped the K-parameters.

Each K-parameter is expressed in the SLIC program as an algebraic equation, combination of the various SLIC parameters which are provided by the SLIC input file SLIC.INP.

According to the values of the SLIC input data the SLIC program calculates the values of the K-parameters in function of the frequency and writes them in an output file SLIC.SLI.

The values of each K-parameter for the frequencies between 10 Hz and 3990 Hz in steps of 10 Hz are written in a table similar to the M-parameters. The contents of these tables are used by the SICOFI program instead of the M-Parameter tables. The format of the K-Parameter Tables is shown on **chapter 7.3.2**.

Proceeding in a similar manner as for obtaining the theoretical equation of the M-parameters, we get the K-parameters.

Figure 14 shows a SLIC with a symmetrical generator V_g and a symmetrical line impedance Z_g.

The SLIC can be considered as a circuit accessible through three ports.

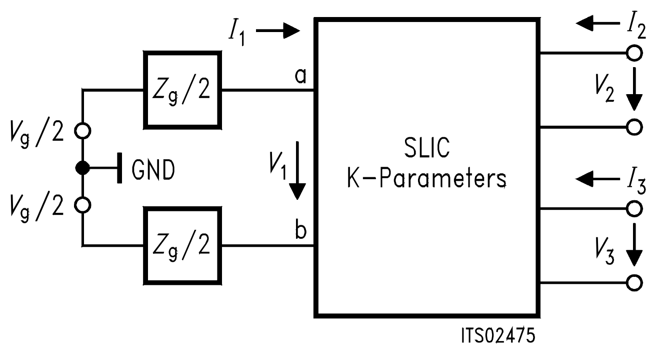


Figure 14
Three-Port Model of a SLIC

Three equations are sufficient to describe the SLIC completely and any linear combination of these variables is possible:

Let us take the following combination:

(1) a1 = $V_1 + Z_g \times I_1$
(2) b1 = $V_1 - Z_g \times I_1$

Then using these new variables, the model of the SLIC becomes:

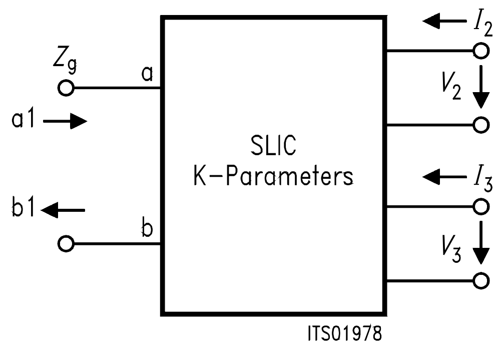


Figure 15
Three-Port Model with the Variables a1 and b1

Following equations can now be written:

(3) $b1 = K11 \times a1 + K12 \times V_3 + K13 \times I_2$
(4) $V_2 = K21 \times a1 + K22 \times V_3 + K23 \times I_2$
(5) $I_3 = K31 \times a1 + K32 \times V_3 + K33 \times I_2$

When the SLIC is connected to the SICOFI, we can assume that:

- $I_2 = 0$ because the input impedance of SICOFI can be included in the model
- I_3 is not relevant in the following calculations because the SICOFI works as an ideal voltage generator. (In special cases the SICOFI output impedance of about 10 Ω may be included in the SLIC model.)

Accordingly the equations system can be simplified as follows:

(6) $b1 = K11 \times a1 + K12 \times V_3$
(7) $V_2 = K21 \times a1 + K22 \times V_3$

a) Parameter K11:

Equation (6) gives K11 = b1/a1 when $V_3 = 0$
From (1) and (2) we can deduce:

$b1/a1 = (V_1 - Z_g \times I_1) / (V_1 + Z_g \times I_1)$
$= (V_1/I_1 - Z_g) / (V_1/I_1 + Z_g)$

Let us call Z_{in} the input impedance of the SLIC:

$Z_{in} = V_1/I_1$

Therefrom

$$K11 = (Z_{in} - Z_g) / (Z_{in} + Z_g) \quad \text{for } V_3 = 0$$

b) Parameter K12:

K12 = b1/V_3 when a1 = 0

From (1) follows: $V_1 + Z_g \times I_1 = 0$

i.e. $V_1 = -Z_g \times I_1$

Thus b1 = $V_1 - Z_g \times I_1 = V_1 + V_1$

Then

K12 = $2 \times V_1 / V_2$

for $V_1 = -Z_g \times I_1$

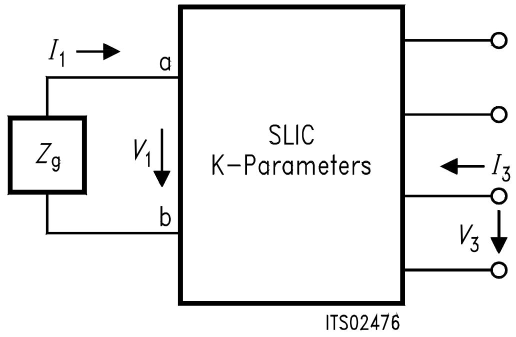


Figure 16
K12 Definition

c) Parameter K21:

K21 = V_2/a1 when $V_3 = 0$

In this case : a1 = $V_1 + Z_g \times I_1 = V_g$

Then

K21 = V_2 / V_g

for $V_3 = 0$

The equivalent circuit is the following:

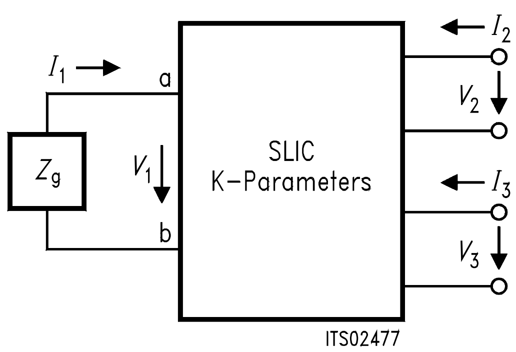


Figure 17
K21 Definition

d) Parameter K22:

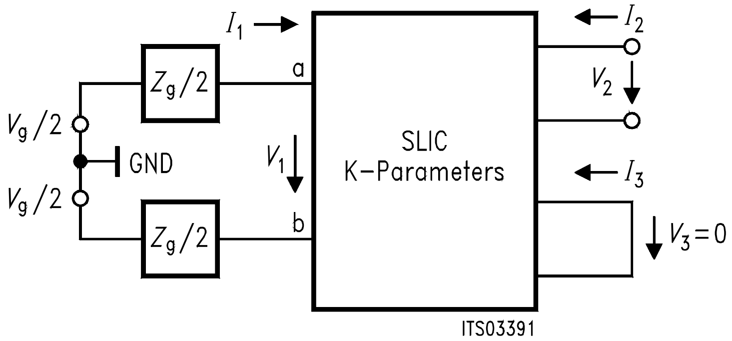


Figure 18
K22 Equivalent Circuit

From (1) and a1 = 0 follows: $V_1 = -Z_g \times I_1$
From (7) and a1 = 0 :

K22 = V_2 / V_3	for $V_1 = -Z_g \times I_1$

Note: 1. All these parameters are accessible by measurement with a symmetrical ground-free generator and a complex voltmeter.
2. $R_L = -20 \times \log10(|K11|)$ is nothing else than the return loss of the SLIC without SICOFI.

Warning: The K-parameters depend on the impedance Z_g and has to be recalculated for every new line impedance.

7.3.1 Format of the K-Parameter Table

This file represents the interface between SICOFI program and SLIC program with K parameters.

It has the following standard form:

Note:
1. '*' at the first position of a line means a comment that the SICOFI program will not use for calculations. Such lines are only for documentation purposes.

2. The SICOFI program looks for the keywords 'ZSLI', 'K11-TABLE', 'K12-TABLE', 'K21-TABLE' and 'K22-TABLE' which have to be at first position without '*' and are followed by the values of FREQUENCY, REAL PART and IMAGINARY PART of the actual parameter.

```
* TRAFO SLIC
* PARAMETER : K
*ZgR1 = 820.0    *ZgC1 = .0000     *ZgR2 = .0000     *ZgC2 = .1150E-06
*ZgRS = 220.0    *ZgCS = .0000
*Z0R1 = 700.0    *Z0C1 = .0000     *Z0R2 = .0000     *Z0C2 = .1000E-06
*Z0RS = .0000    *Z0CS = .0000
*ERZN =  0       *EXZN =  0
*RCU1 = 84.00     *RCU2 = 105.0   *CW1 = .1135E-09  *CW2  = .1354E-09
*L1  =  1.150     * L2  = 1.150   *M  = 1.148
*CSP =  .1000E-05 *
*RV  =  792.0     * LV  = 2.230   *CV = .2670E-08
ZSLI             worst case half loop value
.5000
           FREQ         REAL             IMAG
K11-TABLE                                                keyword
      10.000000   -1.246919E-01     6.369420E-02
      20.000000   -9.300768E-02     1.216179E-01     table
    ...........   .............     ............
    3980.000000   -2.405917E-02     5.318151E-02     400 steps
    3990.000000   -2.436709E-02     5.337689E-02     of 10 Hz each.
K12-TABLE
      10.000000   -5.142274E-03     1.191222E-04
      20.000000   -2.146059E-02     1.294169E-03
    ...........   .............     ............
    3980.000000        1.018615    -6.256870E-02
    3990.000000        1.018857    -6.285563E-02
K21-TABLE
      10.000000   -1.730312E-03     4.013790E-05
      20.000000   -7.222740E-03     4.315760E-04
    ...........   .............     ............
    3980.000000    3.587218E-01    -1.542590E-01
    3990.000000    3.584935E-01    -1.547763E-01
K22-TABLE
      10.000000    1.372118E-01     7.832120E-02
      20.000000    1.578308E-01     1.551709E-01
    ...........   .............     ............
    3980.000000    6.382880E-01     1.535947E-01
    3990.000000    6.384676E-01     1.540913E-01
```

7.4 Running SICOFI® Calculation Program in BATCH Mode

You have the possibility to run the calculation part of the SICOFI coefficients program in a BATCH mode. Instead of typing the commands for the SICOFI program into the keyboard, you may store a sequence of commands in a file.

a) MODE.CTL file

In the directory C:\SICOFI there is a file called MODE.CTL.

In normal (default) working mode the MODE.CTL file contains:

    BATCH = N

In this normal mode the program is waiting for keyboard inputs and you may either start a SLIC program or a calculation of SICOFI coefficients by using different menues.

Using the batch mode change BATCH = N in the MODE.CTL file to

    BATCH = Y

b) BATCH.CTL file

In the BATCH.CTL file you may store a sequence of commands for the SICOFI calculation program. This file has to be in the current working directory.

All commands of the normal calculation mode are available (commands: 1 2 3 4 5 6 7 0) except the commands 8 for HELP and 9 for DOS.

With the BATCH.CTL file shown below the SICOFI program

a) determines the SICOFI coefficients for a HARRIS SLIC application in non-automatic Z and B filter calculation mode.
b) calculates the Z and B filter in an automatic calculation mode (ZAUTO = Y, BAUTO = Y).
c) stores the programming bytes in a file called TEST1.BYT.
c) makes a file result file called TEST1.RES.
d) starts a simulation of SICOFI-SLIC transfer functions
e) stores the results of the simulation in a file called TEST1.SIM.
f) makes a plot file called TEST1.PLT.
g) exits with the last command 0 of the BATCH.CTL file.

Listing of the BATCH.CTL File

```
HARRIS.CTL
1
3
2
ZAUTO = Y   ZREP = Y   BAUTO = Y   BREP = Y
3
5
TEST1.BYT
6
TEST1.RES
2
SIM = ALL
1
4
6
TEST1.SIM
2
SIM = ALL  PLQ = Y
6
TEST1.PLT
0
```

c) SICOAUTO.BAT

To start the SICOFI program in batch mode there has to be a batch file e.g. SICOAUTO.BAT in the current working directory. The contents of the SICOAUTO.BAT file may be:

```
IF EXIST TEST1.BYT DEL TEST1.BYT
IF EXIST TEST1.RES DEL TEST1.RES
IF EXIST TEST1.SIM DEL TEST1.SIM
IF EXIST TEST1.PLT DEL TEST1.PLT
MARK
SICO<BATCH.CTL
RELEASE
```

This batch file starts the program SICO.EXE and takes the commands from the file BATCH.CTL.

If you want to leave this batch mode for to work in the normal SICOFI program mode don't forget to edit the MODE.CTL file in the directory C:\SICOFI and change BATCH = Y to BATCH = N.

Note: If former output files like TEST1.BYT, TEST1.RES, TEST1.SIM or TEST1.PLT already exist, the SICOFI program asks if you want to overwrite them. To suppress this question you should delete those output files before starting the batch sequence.

8 Measurements and Specifications

8.1 Measurements for Verification of SICOFI®-SLIC Transfer Functions

In the simulation mode of the SICOFI coefficients program (command SIM) different transfer functions with SICOFI filters switched on or off can be calculated. On the following pages we propose solution schemes to some of these transfer function measurements e.g:

- Input impedance
- Analog to digital path
- Digital to analog path
- Digital to digital path
- Digital to SICOFI analog output path

We use the PCM4 from Wandel & Goltermann as measurement system.

It is further possible to verify following simulated transfer functions of the SICOFI-SLIC system:

- Digital to SICOFI input path via SLIC loop
- Analog to SICOFI input path
- Analog to SICOFI analog output path via Z-filter loop
- Transfer functions of the SLIC itself with SICOFI filters switched off. This allows to check if the calculated SLIC model is correct.

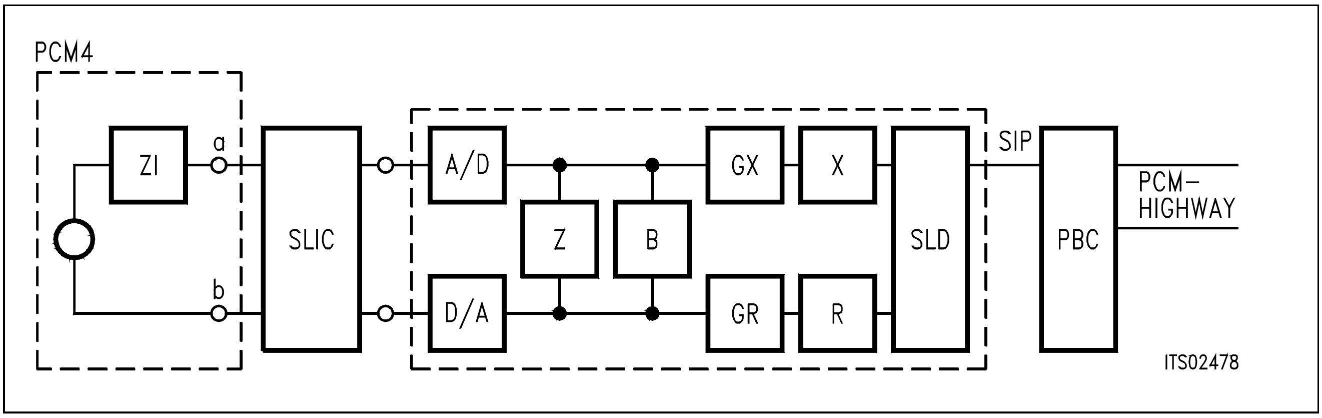


Figure 19

Measuring the Transfer Function Input Impedance

Measurement of return loss with generator impedance Z_l on the a, b line. Optionally, various combination of SICOFI filters can be switched ON or OFF.

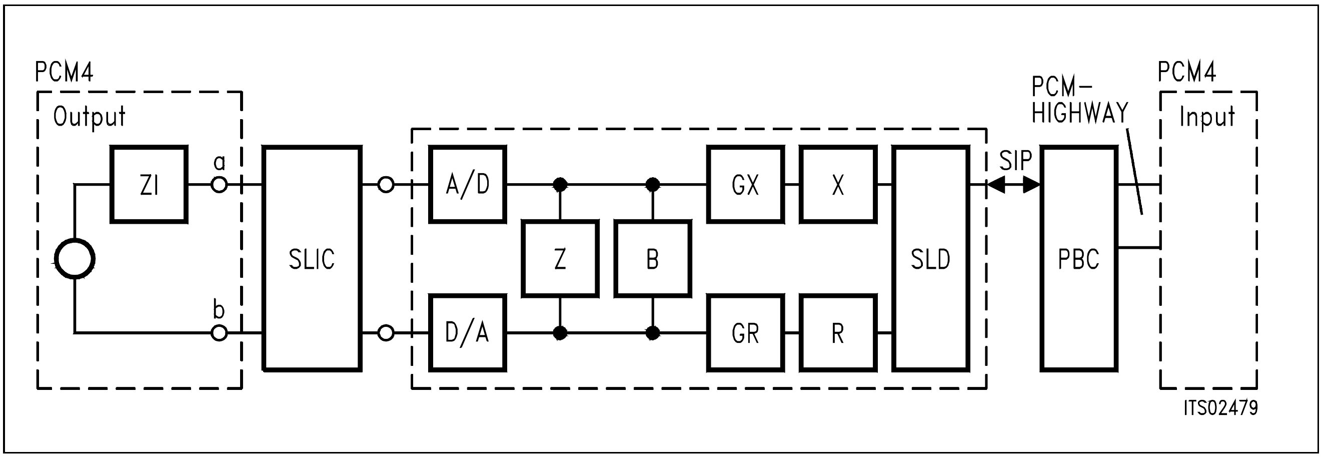


Figure 20

Measuring the Transfer Function Analog – Digital

Analog signal input using the PCM4 across the a, b lines. Generator impedance Z_l/Z_3 on the a, b line. Digital return signal measurement with the PCM4 on the PCM-highway. Optionally, various combinations of SICOFI filters can be switched ON or OFF.

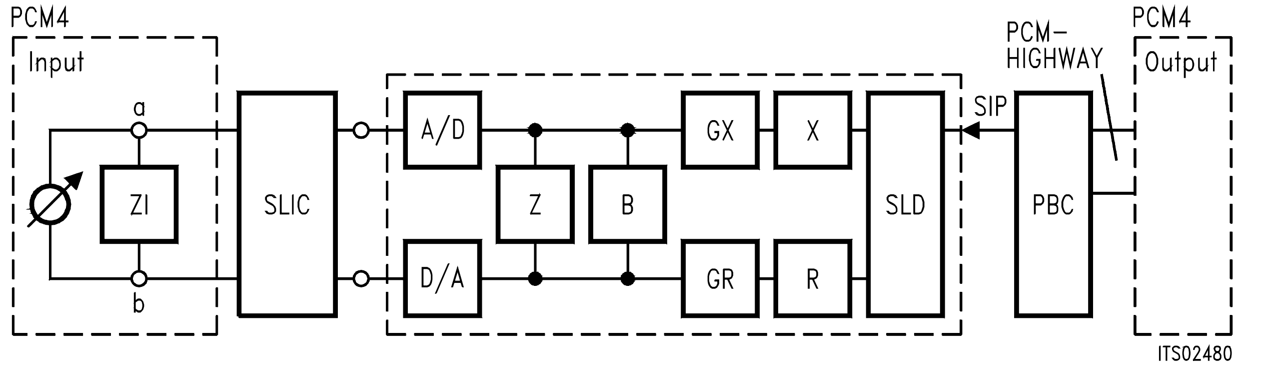


Figure 21

Measuring the Transfer Function Digital – Analog

Digital signal input via the PCM-highway on the PBC. Analog signal measurement with the PCM4 across Z_I/Z_3 on the a, b line. Optionally, various combinations of SICOFI filters can be switched ON or OFF.

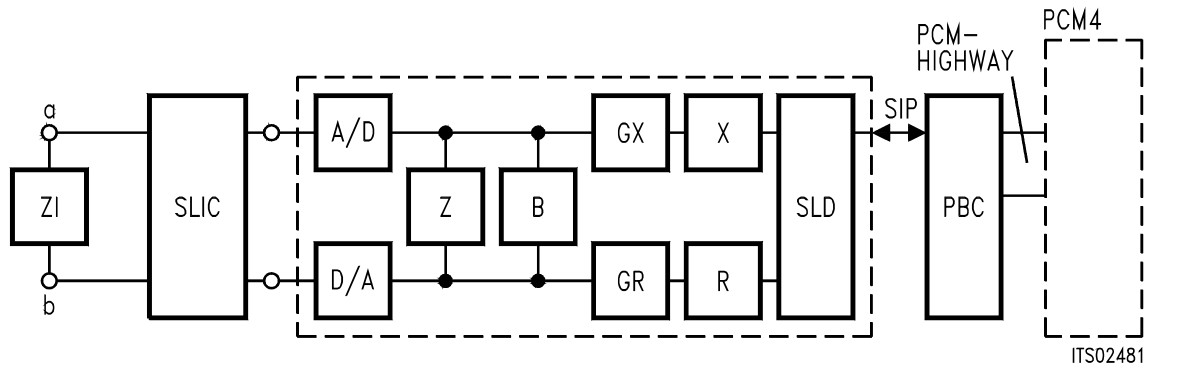


Figure 22

Measuring the Transfer Function Digital – Digital

Digital signal input via the PCM-highway on the PBC. Terminating impedance Z_L on the a, b line. Return digital signal measurement with the PCM4 on the PCM-highway. Optionally, various combinations of SICOFI filters can be switched ON or OFF.

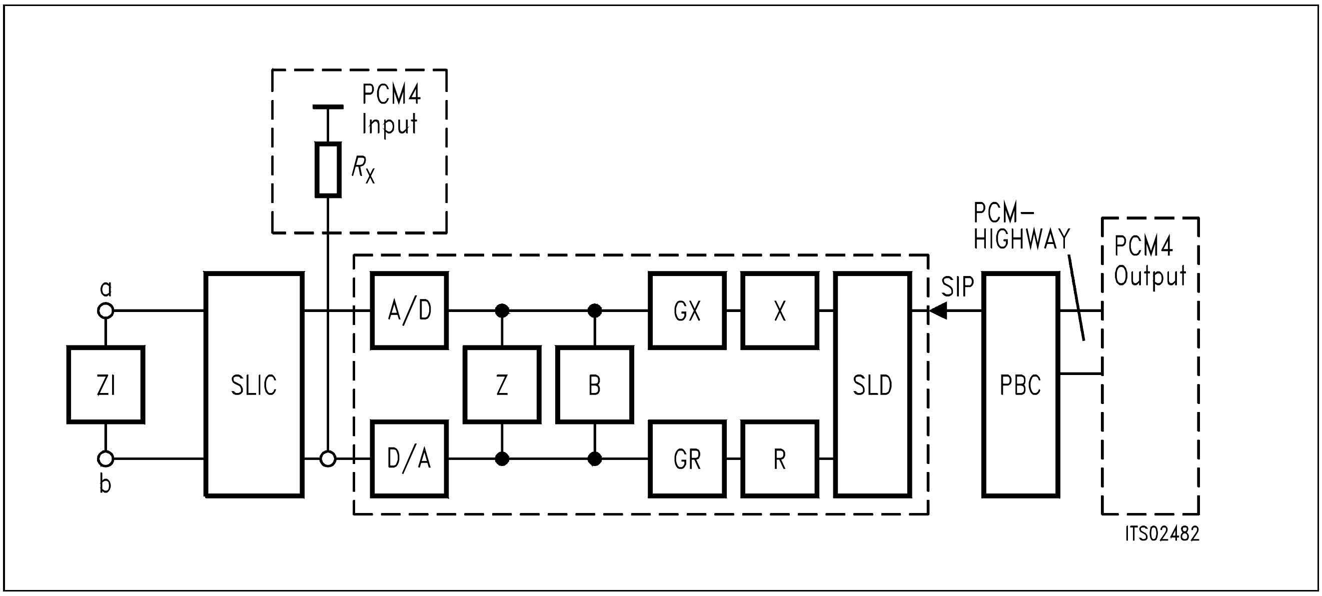


Figure 23

Measuring the Transfer Function Digital – SICOFI® Output

Digital signal input via the PCM-highway on the PBC. Return analog signal measurement with the PCM4 on the SICOFI output (use R_X > 30 kΩ). Terminate the a, b line with impedance Z_I/ Z_3. Optionally, various combinations of SICOFI filters can be switched ON or OFF.

8.2 Extract of Analog Line Card Specifications Valid for the "Deutsche Bundespost"

SLMA specifications differ for each country. Here the peculiar specifications of the "Deutsche Bundespost" (FTZ 12 R4-3) are shown.

The following masks are drawn:

– Return loss

– Balance return loss

– Attenuation distortion in transmit direction (analog → digital)

– Attenuation distortion in receive direction (digital → analog)

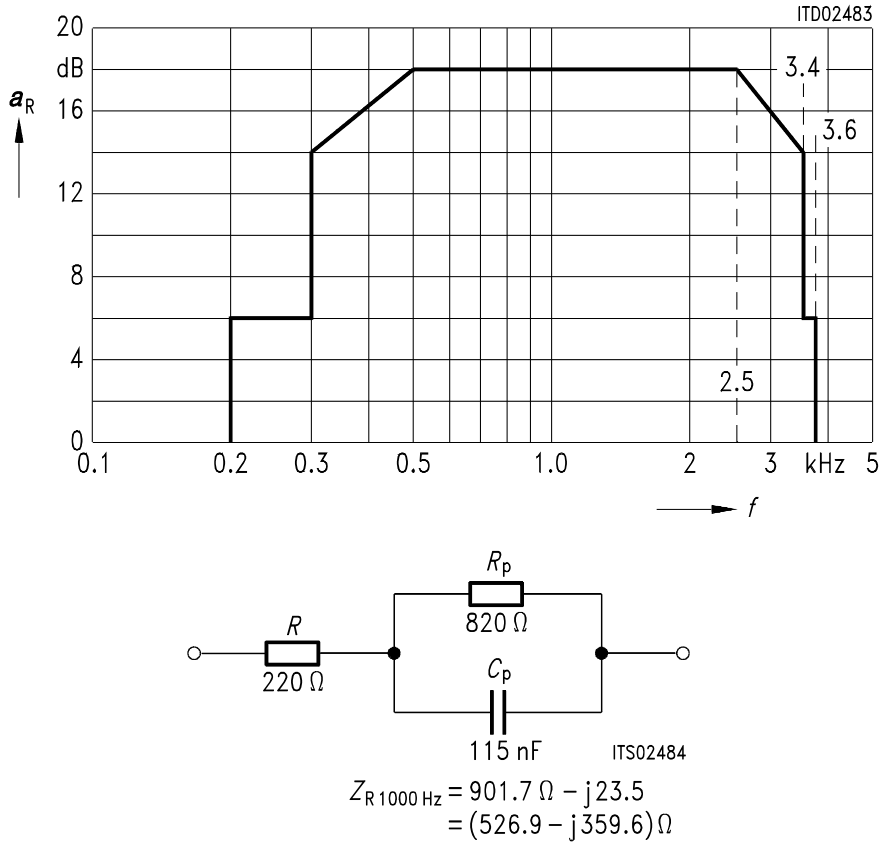


Figure 24

Return Loss a_R

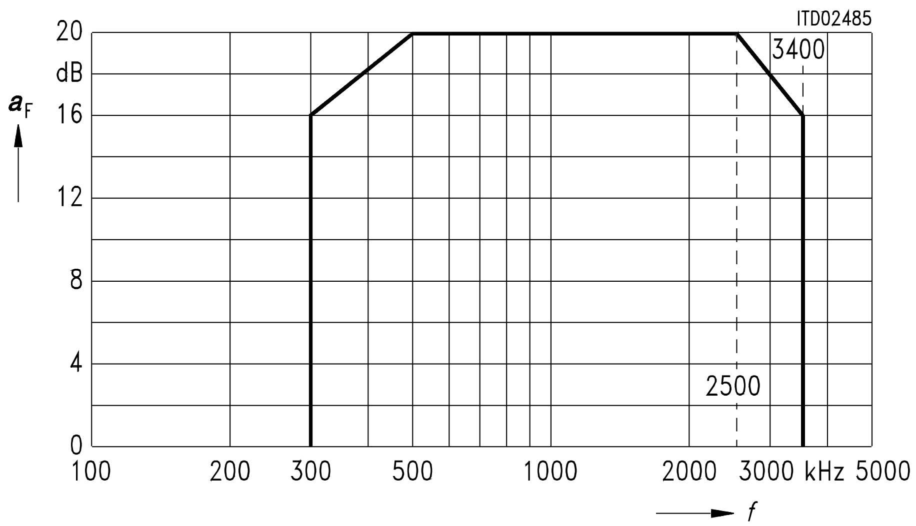


Figure 25

Balance Return Loss a_F

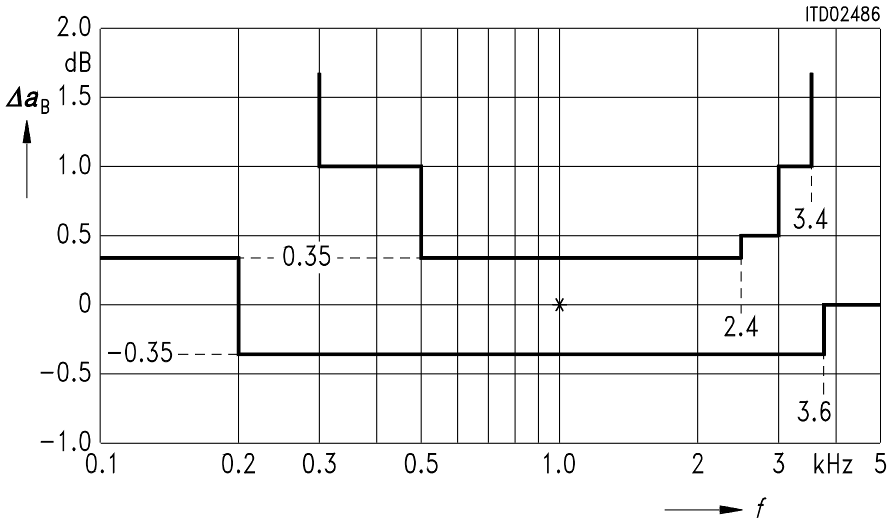


Figure 26

Attenuation Distortion in Transmit Direction
2-Wire Analog → Digital

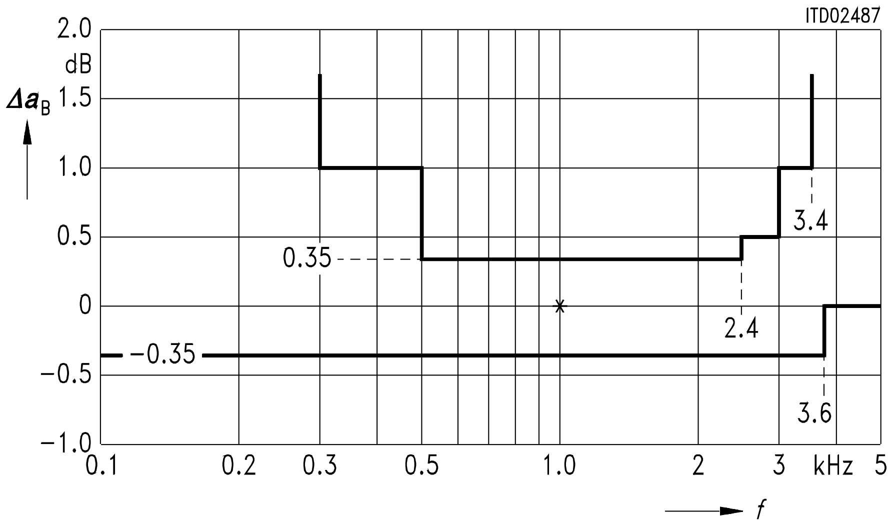


Figure 27

Attenuation Distortion in Receive Direction
Digital → 2-Wire Analog

9 Appendix

9.1 New Features in SICOFI® Software Version 3.0

- program is faster and more user friendly
- easy to install SICOFI software on a PC with a separate SETUP program
- menu driven program surface
- access to different help files (Command HELP) for calculating SICOFI coefficients and SLIC transfer functions. The user can scroll the text contained in different help files.
- SLIC calculation may be started without leaving SICOFI program
- DOS commands are available from program level (Command DOS)
- possibility of starting other small programs (Command DOS)
- RS232 for programming of SICOFI testboard is provided
- extended simulation mode (input impedance, …)
- extra impedance input files covered for input impedance Z_I, terminating impedance Z_3 and load impedance Z_L
- SICOFI program may be run in batch mode
- new features of SICOFI version V 4.x available, like analog amplification AGX, digital amplification TM3 in transmit path and attenuation AGR in receive path

Changes with respect to SICOFI Software Version 2.0:

- Specification file *.SPE has been modified with respect to the definition of input impedance Z_I, load impedance Z_L, impedance Z_3, reference impedance Z_R, reference voltage V_{REF} and return loss specification Z_{IN}.

New Variable	Previous	Function
V_{REF}	V_{REF}	Voltage REFerence of the 0 dBr level
Z_{RE}	Z_{IN}	Z-filter REturnloss specification
Z_{IRP1}	R_{PAR}	Input impedance Z_I was defined together with ERZI.
Z_{ICP1}	- -	
Z_{IRP2}	- -	
Z_{ICP2}	C_{PAR}	
Z_{IRS}	R_{SER}	
Z_{ICS}	C_{SER}	

Same naming conventions for impedance Z_I, Z_L, Z_3 and Z_R.

– Variables in SICOFI control file *.CTL of STS 2060 version 3.0 have been modified:

New Variable	Previous	Function
ZAUTO	PZIN = 0	AUTOmatic calculation of Z filter
BAUTO	PB = 0	AUTOmatic calculation of B filter
FZP	FZ	Frequency points for Z filter calculation in non-automatic optimization mode
FBP	FB	Frequency points for B filter calculation in non-automatic optimization mode
XDISP	XFIL	X filter frequency response DISPlay
RDISP	RFIL	R filter frequency response DISPlay
BDF	TBM	B Delay Filter
AGX	- -	Analog Gain control transmit path
AGR	- -	Analog Gain control receive path
TM3	- -	Test Mode of SICOFI V 4.x: additional gain in transmit path

Note: Do not use specification files or SICOFI control files of SICOFI software version V2.0. The former versions of SLIC.INP together with SLIC.EXE, however, and earlier result files SLIC.SLI could still be used.

```
0.590      1.07031250      1   3       1   0      –1   3      –1   1      30 B9
0.527      1.06250000      1   2       1   0      –1   2      –1   0      20 A8
0.462      1.05468750      1   3       1   0       1   3      –1   1      30 39
0.398      1.04687500      1   3       1   0       1   2      –1   1      30 29
0.333      1.03906250      1   4       1   0       1   1      –1   2      40 1A
0.267      1.03125000      1   3       1   0       1   1      –1   1      30 19
0.201      1.02343750      1   4       1   0       1   2      –1   1      40 29
0.135      1.01562500     –1   3       1   0       1   3      –1   0      B0 38
0.068      1.00781250      1   3       1   0      –1   4      –1   0      30 C8
0.000      1.00000000      1   0       1   1      –1   0       1   0      01 80
```

9.2 Gain Tables for Programming Transmit GX

Table of gain values for programming transmit GX of SICOFI V3.x.

Values from +12 db … 0 dB

$A = \{[(V_1 * 2^{-K1} +1) * V_2 * 2^{-K2} +1] * V_3 * 2^{-K3} +1\} * V_4 * 2^{-K4}$

(dB)	A	v3	k3	v4	k4	v1	k1	v2	k2	HEX
12.041	4.00000000	1	0	1	0	1	0	1	0	00 00
10.881	3.50000000	1	0	1	0	1	1	1	0	00 10
10.238	3.25000000	1	0	1	0	1	2	1	0	00 20
9.897	3.12500000	1	0	1	0	1	3	1	0	00 30
9.722	3.06250000	1	0	1	0	1	4	1	0	00 40
9.632	3.03125000	1	0	1	0	1	5	1	0	00 50
9.588	3.01562500	1	0	1	0	1	6	1	0	00 60
9.542	3.00000000	1	0	1	0	1	0	1	1	00 01
9.497	2.98437500	1	0	1	0	–1	6	1	0	00 E0
9.451	2.96875000	1	0	1	0	–1	5	1	0	00 D0
9.360	2.93750000	1	0	1	0	–1	4	1	0	00 C0
9.173	2.87500000	1	0	1	0	–1	3	1	0	00 B0
8.787	2.75000000	1	0	1	0	1	1	1	1	00 11
8.383	2.62500000	1	0	1	0	1	2	1	1	00 21
8.173	2.56250000	1	0	1	0	1	3	1	1	00 31
8.067	2.53125000	1	0	1	0	1	4	1	1	00 41
8.013	2.51562500	1	0	1	0	1	5	1	1	00 51
7.959	2.50000000	1	0	1	0	–1	1	1	0	00 90
7.904	2.48437500	1	0	1	0	–1	5	1	1	00 D1
7.850	2.46875000	1	0	1	0	–1	4	1	1	00 C1
7.739	2.43750000	1	0	1	0	–1	3	1	1	00 B1
7.513	2.37500000	1	0	1	0	1	1	1	2	00 12
7.282	2.31250000	1	0	1	0	1	2	1	2	00 22
7.163	2.28125000	1	0	1	0	1	3	1	2	00 32
7.104	2.26562500	1	0	1	0	1	4	1	2	00 42
7.059	2.25390625	1	0	1	0	1	6	1	2	00 62
7.044	2.25000000	1	0	1	0	–1	1	1	1	00 91
6.922	2.21875000	1	0	1	0	–1	3	1	2	00 B2
6.799	2.18750000	1	0	1	0	1	1	1	3	00 13
6.674	2.15625000	1	0	1	0	1	2	1	3	00 23
6.611	2.14062500	1	0	1	0	1	3	1	3	00 33
6.579	2.13281250	1	0	1	0	1	4	1	3	00 43
6.547	2.12500000	1	0	1	0	–1	1	1	2	00 92
6.483	2.10937500	1	0	1	0	–1	3	1	3	00 B3
6.418	2.09375000	1	0	1	0	–1	2	1	3	00 A3
6.353	2.07812500	1	0	1	0	1	2	1	4	00 24
6.321	2.07031250	1	0	1	0	1	3	1	4	00 34
6.288	2.06250000	1	0	1	0	–1	1	1	3	00 93
6.222	2.04687500	1	0	1	0	–1	2	1	4	00 A4
6.155	2.03125000	1	0	1	0	–1	1	1	4	00 94
6.088	2.01562500	1	0	1	0	–1	1	1	5	00 95
6.021	2.00000000	1	0	1	0	–1	0	1	0	00 80
5.952	1.98437500	1	1	1	0	–1	5	1	0	10 D0
5.884	1.96875000	1	0	1	0	–1	1	–1	4	00 9C
5.815	1.95312500	1	0	1	0	–1	2	–1	4	00 AC
5.745	1.93750000	1	0	1	0	–1	1	–1	3	00 9B

(dB)	A	v3,	k3	v4,	k4	v1,	k1	v2,	k2	HEX
5.675	1.92187500	1	0	1	0	1	2	-1	4	00 2C
5.604	1.90625000	1	0	1	0	–1	2	–1	3	00 AB
5.532	1.89062500	1	0	1	0	–1	3	–1	3	00 BB
5.460	1.87500000	1	1	1	0	1	1	1	1	10 11
5.424	1.86718750	1	0	1	0	1	4	–1	3	00 4B
5.387	1.85937500	1	0	1	0	1	3	–1	3	00 3B
5.314	1.84375000	1	0	1	0	1	2	–1	3	00 2B
5.166	1.81250000	1	1	1	0	1	2	1	1	10 21
5.014	1.78125000	1	1	1	0	1	3	1	1	10 31
4.938	1.76562500	1	1	1	0	1	4	1	1	10 41
4.861	1.75000000	1	1	1	0	–1	1	1	0	10 90
4.822	1.74218750	1	1	1	0	–1	5	1	1	10 D1
4.783	1.73437500	1	1	1	0	–1	4	1	1	10 C1
4.704	1.71875000	1	1	1	0	–1	3	1	1	10 B1
4.545	1.68750000	1	1	1	0	–1	2	1	1	10 A1
4.383	1.65625000	1	1	1	0	1	2	1	2	10 22
4.300	1.64062500	1	1	1	0	1	3	1	2	10 32
4.259	1.63281250	1	1	1	0	1	4	1	2	10 42
4.217	1.62500000	1	1	1	0	–1	1	1	1	10 91
4.133	1.60937500	1	1	1	0	–1	3	1	2	10 B2
4.048	1.59375000	1	1	1	0	1	1	1	3	10 13
3.963	1.57812500	1	1	1	0	1	2	1	3	10 23
3.920	1.57031250	1	1	1	0	1	3	1	3	10 33
3.876	1.56250000	1	1	1	0	–1	1	1	2	10 92
3.833	1.55468750	1	1	1	0	–1	3	1	3	10 B3
3.789	1.54687500	1	1	1	0	1	1	1	4	10 14
3.745	1.53906250	1	1	1	0	1	2	1	4	10 24
3.701	1.53125000	1	1	1	0	–1	1	1	3	10 93
3.656	1.52343750	1	1	1	0	1	1	1	5	10 15
3.612	1.51562500	1	1	1	0	–1	1	1	4	10 94
3.567	1.50781250	1	1	1	0	–1	1	1	5	10 95
3.522	1.50000000	–1	0	1	0	1	1	–1	0	80 18
3.476	1.49218750	1	2	1	0	–1	5	1	0	20 D0
3.431	1.48437500	1	1	1	0	–1	1	–1	4	10 9C
3.385	1.47656250	1	1	1	0	1	1	–1	5	10 1D
3.339	1.46875000	1	1	1	0	–1	1	–1	3	10 9B
3.293	1.46093750	1	1	1	0	1	2	–1	4	10 2C
3.246	1.45312500	1	1	1	0	1	1	–1	4	10 1C
3.199	1.44531250	1	1	1	0	–1	3	–1	3	10 BB
3.152	1.43750000	1	1	1	0	–1	1	–1	2	10 9A
3.105	1.42968750	1	1	1	0	1	3	–1	3	10 3B
3.057	1.42187500	1	1	1	0	1	2	–1	3	10 2B
2.961	1.40625000	1	2	1	0	1	2	1	1	20 21
2.864	1.39062500	1	2	1	0	1	3	1	1	20 31
2.815	1.38281250	1	2	1	0	1	4	1	1	20 41
2.766	1.37500000	1	1	1	0	–1	1	–1	1	10 99
2.717	1.36718750	1	2	1	0	–1	4	1	1	20 C1
2.667	1.35937500	1	2	1	0	–1	3	1	1	20 B1
2.566	1.34375000	1	2	1	0	1	1	1	2	20 12
2.465	1.32812500	1	2	1	0	1	2	1	2	20 22
2.414	1.32031250	1	2	1	0	1	3	1	2	20 32
2.362	1.31250000	1	2	1	0	–1	1	1	1	20 91
2.310	1.30468750	1	2	1	0	–1	3	1	2	20 B2
2.258	1.29687500	1	2	1	0	–1	2	1	2	20 A2
2.205	1.28906250	1	2	1	0	1	2	1	3	20 23

(dB)	A	v3,	k3	v4,	k4	v1,	k1	v2,	k2	HEX
2.153	1.28125000	1	2	1	0	–1	1	1	2	20 92
2.100	1.27343750	1	2	1	0	–1	2	1	3	20 A3
2.046	1.26562500	1	2	1	0	–1	1	1	3	20 93
1.992	1.25781250	1	2	1	0	–1	1	1	4	20 94
1.938	1.25000000	–1	1	1	0	1	1	–1	0	90 18
1.884	1.24218750	1	2	1	0	–1	1	–1	4	20 9C
1.829	1.23437500	1	2	1	0	–1	1	–1	3	20 9B
1.774	1.22656250	1	2	1	0	–1	2	–1	3	20 AB
1.718	1.21875000	1	2	1	0	–1	1	–1	2	20 9A
1.662	1.21093750	1	2	1	0	1	2	–1	3	20 2B
1.606	1.20312500	1	2	1	0	–1	2	–1	2	20 AA
1.550	1.19531250	1	2	1	0	–1	3	–1	2	20 BA
1.493	1.18750000	1	2	1	0	–1	1	–1	1	20 99
1.435	1.17968750	1	2	1	0	1	3	–1	2	20 3A
1.378	1.17187500	1	3	1	0	1	1	1	2	30 12
1.320	1.16406250	1	3	1	0	1	2	1	2	30 22
1.261	1.15625000	1	2	1	0	1	1	–1	2	20 1A
1.202	1.14843750	1	3	1	0	–1	2	1	2	30 A2
1.143	1.14062500	1	3	1	0	–1	1	1	2	30 92
1.083	1.13281250	1	3	1	0	–1	1	1	3	30 93
1.023	1.12500000	1	1	1	0	1	1	–1	1	10 19
0.963	1.11718750	1	3	1	0	–1	1	–1	3	30 9B
0.902	1.10937500	1	3	1	0	–1	1	–1	2	30 9A
0.840	1.10156250	1	4	1	0	1	2	1	1	40 21
0.778	1.09375000	1	2	1	0	1	2	–1	1	20 29
0.716	1.08593750	1	3	1	0	1	2	–1	2	30 2A
0.653	1.07812500	1	3	1	0	1	1	–1	2	30 1A
0.590	1.07031250	1	3	1	0	–1	3	–1	1	30 B9
0.527	1.06250000	1	2	1	0	–1	2	–1	0	20 A8
0.462	1.05468750	1	3	1	0	1	3	–1	1	30 39
0.398	1.04687500	1	3	1	0	1	2	–1	1	30 29
0.333	1.03906250	1	4	1	0	1	1	–1	2	40 1A
0.267	1.03125000	1	3	1	0	1	1	–1	1	30 19
0.201	1.02343750	1	4	1	0	1	2	–1	1	40 29
0.135	1.01562500	–1	3	1	0	1	3	–1	0	B0 38
0.068	1.00781250	1	3	1	0	–1	4	–1	0	30 C8
0.000	1.00000000	1	0	1	1	–1	0	1	0	01 80

Table of Gain Values for Programming Transmit GX of SICOFI V4.X.

Values from +18 db … 0 dB Date: 1.02.89

$A = \{[(V_1 * 2^{-K1} +1) * V_2 * 2^{-K2} +1] * V_3 * 2^{-K3} +1\} * V_4 * 2^{-K4}$

```
GX = A       if TM3 = 000
GX = 2.* A   if TM3 = 001
GX = 4.* A   if TM3 = 011
```

(dB)	GX	v3,	k3	v4,	k4	v1,	k1	v2,	k2	HEX	TM3
18.063	8.000	1	0	1	0	–1	0	1	0	00 80	011
17.994	7.938	1	1	1	0	–1	5	1	0	10 D0	011
17.926	7.875	1	0	1	0	–1	1	–1	4	00 9C	011
17.857	7.813	1	0	1	0	–1	2	–1	4	00 AC	011
17.787	7.750	1	0	1	0	–1	1	–1	3	00 9B	011
17.717	7.688	1	0	1	0	1	2	–1	4	00 2C	011
17.646	7.625	1	0	1	0	–1	2	–1	3	00 AB	011
17.574	7.563	1	0	1	0	–1	3	–1	3	00 BB	011
17.502	7.500	1	1	1	0	1	1	1	1	10 11	011
17.466	7.469	1	0	1	0	1	4	–1	3	00 4B	011
17.429	7.438	1	0	1	0	1	3	–1	3	00 3B	011
17.356	7.375	1	0	1	0	1	2	–1	3	00 2B	011
17.208	7.250	1	1	1	0	1	2	1	1	10 21	011
17.056	7.125	1	1	1	0	1	3	1	1	10 31	011
16.980	7.063	1	1	1	0	1	4	1	1	10 41	011
16.903	7.000	1	1	1	0	–1	1	1	0	10 90	011
16.864	6.969	1	1	1	0	–1	5	1	1	10 D1	011
16.825	6.938	1	1	1	0	–1	4	1	1	10 C1	011
16.746	6.875	1	1	1	0	–1	3	1	1	10 B1	011
16.587	6.750	1	1	1	0	–1	2	1	1	10 A1	011
16.425	6.625	1	1	1	0	1	2	1	2	10 22	011
16.342	6.563	1	1	1	0	1	3	1	2	10 32	011
16.301	6.531	1	1	1	0	1	4	1	2	10 42	011
16.259	6.500	1	1	1	0	–1	1	1	1	10 91	011
16.175	6.438	1	1	1	0	–1	3	1	2	10 B2	011
16.090	6.375	1	1	1	0	1	1	1	3	10 13	011
16.005	6.313	1	1	1	0	1	2	1	3	10 23	011
15.962	6.281	1	1	1	0	1	3	1	3	10 33	011
15.918	6.250	1	1	1	0	–1	1	1	2	10 92	011
15.875	6.219	1	1	1	0	–1	3	1	3	10 B3	011
15.831	6.188	1	1	1	0	1	1	1	4	10 14	011
15.787	6.156	1	1	1	0	1	2	1	4	10 24	011
15.743	6.125	1	1	1	0	–1	1	1	3	10 93	011
15.698	6.094	1	1	1	0	1	1	1	5	10 15	011
15.654	6.063	1	1	1	0	–1	1	1	4	10 94	011
15.609	6.031	1	1	1	0	–1	1	1	5	10 95	011
15.564	6.000	–1	0	1	0	1	1	–1	0	80 18	011
15.518	5.969	1	2	1	0	–1	5	1	0	20 D0	011
15.473	5.938	1	1	1	0	–1	1	–1	4	10 9C	011
15.427	5.906	1	1	1	0	1	1	–1	5	10 1D	011
15.381	5.875	1	1	1	0	–1	1	–1	3	10 9B	011
15.335	5.844	1	1	1	0	1	2	–1	4	10 2C	011
15.288	5.813	1	1	1	0	1	1	–1	4	10 1C	011

(dB)	GX	v3, k3		v4, k4		v1, k1		v2, k2		HEX	TM3
15.241	5.781	1	1	1	0	–1	3	–1	3	10 BB	011
15.194	5.750	1	1	1	0	–1	1	–1	2	10 9A	011
15.147	5.719	1	1	1	0	1	3	–1	3	10 3B	011
15.099	5.688	1	1	1	0	1	2	–1	3	10 2B	011
15.003	5.625	1	2	1	0	1	2	1	1	20 21	011
14.906	5.563	1	2	1	0	1	3	1	1	20 31	011
14.857	5.531	1	2	1	0	1	4	1	1	20 41	011
14.808	5.500	1	1	1	0	–1	1	–1	1	10 99	011
14.759	5.469	1	2	1	0	–1	4	1	1	20 C1	011
14.709	5.438	1	2	1	0	–1	3	1	1	20 B1	011
14.608	5.375	1	2	1	0	1	1	1	2	20 12	011
14.507	5.313	1	2	1	0	1	2	1	2	20 22	011
14.456	5.281	1	2	1	0	1	3	1	2	20 32	011
14.404	5.250	1	2	1	0	–1	1	1	1	20 91	011
14.352	5.219	1	2	1	0	–1	3	1	2	20 B2	011
14.300	5.188	1	2	1	0	–1	2	1	2	20 A2	011
14.247	5.156	1	2	1	0	1	2	1	3	20 23	011
14.195	5.125	1	2	1	0	–1	1	1	2	20 92	011
14.142	5.094	1	2	1	0	–1	2	1	3	20 A3	011
14.088	5.063	1	2	1	0	–1	1	1	3	20 93	011
14.034	5.031	1	2	1	0	–1	1	1	4	20 94	011
13.980	5.000	–1	1	1	0	1	1	–1	0	90 18	011
13.926	4.969	1	2	1	0	–1	1	–1	4	20 9C	011
13.871	4.938	1	2	1	0	–1	1	–1	3	20 9B	011
13.816	4.906	1	2	1	0	–1	2	–1	3	20 AB	011
13.760	4.875	1	2	1	0	–1	1	–1	2	20 9A	011
13.704	4.844	1	2	1	0	1	2	–1	3	20 2B	011
13.648	4.813	1	2	1	0	–1	2	–1	2	20 AA	011
13.592	4.781	1	2	1	0	–1	3	–1	2	20 BA	011
13.535	4.750	1	2	1	0	–1	1	–1	1	20 99	011
13.477	4.719	1	2	1	0	1	3	–1	2	20 3A	011
13.420	4.688	1	3	1	0	1	1	1	2	30 12	011
13.362	4.656	1	3	1	0	1	2	1	2	30 22	011
13.303	4.625	1	2	1	0	1	1	–1	2	20 1A	011
13.244	4.594	1	3	1	0	–1	2	1	2	30 A2	011
13.185	4.563	1	3	1	0	–1	1	1	2	30 92	011
13.125	4.531	1	3	1	0	–1	1	1	3	30 93	011
13.065	4.500	1	1	1	0	1	1	–1	1	10 19	011
13.005	4.469	1	3	1	0	–1	1	–1	3	30 9B	011
12.944	4.438	1	3	1	0	–1	1	–1	2	30 9A	011
12.882	4.406	1	4	1	0	1	2	1	1	40 21	011
12.820	4.375	1	2	1	0	1	2	–1	1	20 29	011
12.758	4.344	1	3	1	0	1	2	–1	2	30 2A	011
12.695	4.313	1	3	1	0	1	1	–1	2	30 1A	011
12.632	4.281	1	3	1	0	–1	3	–1	1	30 B9	011
12.569	4.250	1	2	1	0	–1	2	–1	0	20 A8	011
12.504	4.219	1	3	1	0	1	3	–1	1	30 39	011
12.440	4.188	1	3	1	0	1	2	–1	1	30 29	011
12.375	4.156	1	4	1	0	1	1	–1	2	40 1A	011
12.309	4.125	1	3	1	0	1	1	–1	1	30 19	011
12.243	4.094	1	4	1	0	1	2	–1	1	40 29	011
12.177	4.063	–1	3	1	0	1	3	–1	0	B0 38	011
12.110	4.031	1	3	1	0	–1	4	–1	0	30 C8	011
12.042	4.000	1	0	1	0	–1	0	1	0	00 80	001
11.973	3.969	1	1	1	0	–1	5	1	0	10 D0	001

(dB)	GX	v3, k3		v4, k4		v1, k1		v2, k2		HEX	TM3
11.905	3.938	1	0	1	0	–1	1	–1	4	00 9C	001
11.836	3.906	1	0	1	0	–1	2	–1	4	00 AC	001
11.766	3.875	1	0	1	0	–1	1	–1	3	00 9B	001
11.696	3.844	1	0	1	0	1	2	–1	4	00 2C	001
11.625	3.813	1	0	1	0	–1	2	–1	3	00 AB	001
11.553	3.781	1	0	1	0	–1	3	–1	3	00 BB	001
11.481	3.750	1	1	1	0	1	1	1	1	10 11	001
11.445	3.734	1	0	1	0	1	4	–1	3	00 4B	001
11.408	3.719	1	0	1	0	1	3	–1	3	00 3B	001
11.335	3.688	1	0	1	0	1	2	–1	3	00 2B	001
11.187	3.625	1	1	1	0	1	2	1	1	10 21	001
11.035	3.563	1	1	1	0	1	3	1	1	10 31	001
10.959	3.531	1	1	1	0	1	4	1	1	10 41	001
10.882	3.500	1	1	1	0	–1	1	1	0	10 90	001
10.843	3.484	1	1	1	0	–1	5	1	1	10 D1	001
10.804	3.469	1	1	1	0	–1	4	1	1	10 C1	001
10.725	3.438	1	1	1	0	–1	3	1	1	10 B1	001
10.566	3.375	1	1	1	0	–1	2	1	1	10 A1	001
10.404	3.313	1	1	1	0	1	2	1	2	10 22	001
10.321	3.281	1	1	1	0	1	3	1	2	10 32	001
10.280	3.266	1	1	1	0	1	4	1	2	10 42	001
10.238	3.250	1	1	1	0	–1	1	1	1	10 91	001
10.154	3.219	1	1	1	0	–1	3	1	2	10 B2	001
10.069	3.188	1	1	1	0	1	1	1	3	10 13	001
9.984	3.156	1	1	1	0	1	2	1	3	10 23	001
9.941	3.141	1	1	1	0	1	3	1	3	10 33	001
9.897	3.125	1	1	1	0	–1	1	1	2	10 92	001
9.854	3.109	1	1	1	0	–1	3	1	3	10 B3	001
9.810	3.094	1	1	1	0	1	1	1	4	10 14	001
9.766	3.078	1	1	1	0	1	2	1	4	10 24	001
9.722	3.063	1	1	1	0	–1	1	1	3	10 93	001
9.677	3.047	1	1	1	0	1	1	1	5	10 15	001
9.633	3.031	1	1	1	0	–1	1	1	4	10 94	001
9.588	3.016	1	1	1	0	–1	1	1	5	10 95	001
9.543	3.000	–1	0	1	0	1	1	–1	0	80 18	001
9.497	2.984	1	2	1	0	–1	5	1	0	20 D0	001
9.452	2.969	1	1	1	0	–1	1	–1	4	10 9C	001
9.406	2.953	1	1	1	0	1	1	–1	5	10 1D	001
9.360	2.938	1	1	1	0	–1	1	–1	3	10 9B	001
9.314	2.922	1	1	1	0	1	2	–1	4	10 2C	001
9.267	2.906	1	1	1	0	1	1	–1	4	10 1C	001
9.220	2.891	1	1	1	0	–1	3	–1	3	10 BB	001
9.173	2.875	1	1	1	0	–1	1	–1	2	10 9A	001
9.126	2.859	1	1	1	0	1	3	–1	3	10 3B	001
9.078	2.844	1	1	1	0	1	2	–1	3	10 2B	001
8.982	2.813	1	2	1	0	1	2	1	1	20 21	001
8.885	2.781	1	2	1	0	1	3	1	1	20 31	001
8.836	2.766	1	2	1	0	1	4	1	1	20 41	001
8.787	2.750	1	1	1	0	–1	1	–1	1	10 99	001
8.738	2.734	1	2	1	0	–1	4	1	1	20 C1	001
8.688	2.719	1	2	1	0	–1	3	1	1	20 B1	001
8.587	2.688	1	2	1	0	1	1	1	2	20 12	001
8.486	2.656	1	2	1	0	1	2	1	2	20 22	001
8.435	2.641	1	2	1	0	1	3	1	2	20 32	001
8.383	2.625	1	2	1	0	–1	1	1	1	20 91	001

(dB)	GX	v3,	k3	v4,	k4	v1,	k1	v2,	k2	HEX	TM3
8.331	2.609	1	2	1	0	–1	3	1	2	20 B2	001
8.279	2.594	1	2	1	0	–1	2	1	2	20 A2	001
8.226	2.578	1	2	1	0	1	2	1	3	20 23	001
8.174	2.563	1	2	1	0	–1	1	1	2	20 92	001
8.121	2.547	1	2	1	0	–1	2	1	3	20 A3	001
8.067	2.531	1	2	1	0	–1	1	1	3	20 93	001
8.013	2.516	1	2	1	0	–1	1	1	4	20 94	001
7.959	2.500	–1	1	1	0	1	1	–1	0	90 18	001
7.905	2.484	1	2	1	0	–1	1	–1	4	20 9C	001
7.850	2.469	1	2	1	0	–1	1	–1	3	20 9B	001
7.795	2.453	1	2	1	0	–1	2	–1	3	20 AB	001
7.739	2.438	1	2	1	0	–1	1	–1	2	20 9A	001
7.683	2.422	1	2	1	0	1	2	–1	3	20 2B	001
7.627	2.406	1	2	1	0	–1	2	–1	2	20 AA	001
7.571	2.391	1	2	1	0	–1	3	–1	2	20 BA	001
7.514	2.375	1	2	1	0	–1	1	–1	1	20 99	001
7.456	2.359	1	2	1	0	1	3	–1	2	20 3A	001
7.399	2.344	1	3	1	0	1	1	1	2	30 12	001
7.341	2.328	1	3	1	0	1	2	1	2	30 22	001
7.282	2.313	1	2	1	0	1	1	–1	2	20 1A	001
7.223	2.297	1	3	1	0	–1	2	1	2	30 A2	001
7.164	2.281	1	3	1	0	–1	1	1	2	30 92	001
7.104	2.266	1	3	1	0	–1	1	1	3	30 93	001
7.044	2.250	1	1	1	0	1	1	–1	1	10 19	001
6.984	2.234	1	3	1	0	–1	1	–1	3	30 9B	001
6.923	2.219	1	3	1	0	–1	1	–1	2	30 9A	001
6.861	2.203	1	4	1	0	1	2	1	1	40 21	001
6.799	2.188	1	2	1	0	1	2	–1	1	20 29	001
6.737	2.172	1	3	1	0	1	2	–1	2	30 2A	001
6.674	2.156	1	3	1	0	1	1	–1	2	30 1A	001
6.611	2.141	1	3	1	0	–1	3	–1	1	30 B9	001
6.548	2.125	1	2	1	0	–1	2	–1	0	20 A8	001
6.483	2.109	1	3	1	0	1	3	–1	1	30 39	001
6.419	2.094	1	3	1	0	1	2	–1	1	30 29	001
6.354	2.078	1	4	1	0	1	1	–1	2	40 1A	001
6.288	2.063	1	3	1	0	1	1	–1	1	30 19	001
6.222	2.047	1	4	1	0	1	2	–1	1	40 29	001
6.156	2.031	–1	3	1	0	1	3	–1	0	B0 38	001
6.089	2.016	1	3	1	0	–1	4	–1	0	30 C8	001
6.021	2.000	1	0	1	0	–1	0	1	0	00 80	000
5.952	1.984	1	1	1	0	–1	5	1	0	10 D0	000
5.884	1.969	1	0	1	0	–1	1	–1	4	00 9C	000
5.815	1.953	1	0	1	0	–1	2	–1	4	00 AC	000
5.745	1.938	1	0	1	0	–1	1	–1	3	00 9B	000
5.675	1.922	1	0	1	0	1	2	–1	4	00 2C	000
5.604	1.906	1	0	1	0	–1	2	–1	3	00 AB	000
5.532	1.891	1	0	1	0	–1	3	–1	3	00 BB	000
5.460	1.875	1	1	1	0	1	1	1	1	10 11	000
5.424	1.867	1	0	1	0	1	4	–1	3	00 4B	000
5.387	1.859	1	0	1	0	1	3	–1	3	00 3B	000
5.314	1.844	1	0	1	0	1	2	–1	3	00 2B	000
5.166	1.813	1	1	1	0	1	2	1	1	10 21	000
5.014	1.781	1	1	1	0	1	3	1	1	10 31	000
4.938	1.766	1	1	1	0	1	4	1	1	10 41	000
4.861	1.750	1	1	1	0	–1	1	1	0	10 90	000

(dB)	GX	v3,	k3	v4,	k4	v1,	k1	v2,	k2	HEX	TM3
4.822	1.742	1	1	1	0	–1	5	1	1	10 D1	000
4.783	1.734	1	1	1	0	–1	4	1	1	10 C1	000
4.704	1.719	1	1	1	0	–1	3	1	1	10 B1	000
4.545	1.688	1	1	1	0	–1	2	1	1	10 A1	000
4.383	1.656	1	1	1	0	1	2	1	2	10 22	000
4.300	1.641	1	1	1	0	1	3	1	2	10 32	000
4.259	1.633	1	1	1	0	1	4	1	2	10 42	000
4.217	1.625	1	1	1	0	–1	1	1	1	10 91	000
4.133	1.609	1	1	1	0	–1	3	1	2	10 B2	000
4.048	1.594	1	1	1	0	1	1	1	3	10 13	000
3.963	1.578	1	1	1	0	1	2	1	3	10 23	000
3.920	1.570	1	1	1	0	1	3	1	3	10 33	000
3.876	1.563	1	1	1	0	–1	1	1	2	10 92	000
3.833	1.555	1	1	1	0	–1	3	1	3	10 B3	000
3.789	1.547	1	1	1	0	1	1	1	4	10 14	000
3.745	1.539	1	1	1	0	1	2	1	4	10 24	000
3.701	1.531	1	1	1	0	–1	1	1	3	10 93	000
3.656	1.523	1	1	1	0	1	1	1	5	10 15	000
3.612	1.516	1	1	1	0	–1	1	1	4	10 94	000
3.567	1.508	1	1	1	0	–1	1	1	5	10 95	000
3.522	1.500	–1	0	1	0	1	1	–1	0	80 18	000
3.476	1.492	1	2	1	0	–1	5	1	0	20 D0	000
3.431	1.484	1	1	1	0	–1	1	–1	4	10 9C	000
3.385	1.477	1	1	1	0	1	1	–1	5	10 1D	000
3.339	1.469	1	1	1	0	–1	1	–1	3	10 9B	000
3.293	1.461	1	1	1	0	1	2	–1	4	10 2C	000
3.246	1.453	1	1	1	0	1	1	–1	4	10 1C	000
3.199	1.445	1	1	1	0	–1	3	–1	3	10 BB	000
3.152	1.438	1	1	1	0	–1	1	–1	2	10 9A	000
3.105	1.430	1	1	1	0	1	3	–1	3	10 3B	000
3.057	1.422	1	1	1	0	1	2	–1	3	10 2B	000
2.961	1.406	1	2	1	0	1	2	1	1	20 21	000
2.864	1.391	1	2	1	0	1	3	1	1	20 31	000
2.815	1.383	1	2	1	0	1	4	1	1	20 41	000
2.766	1.375	1	1	1	0	–1	1	–1	1	10 99	000
2.717	1.367	1	2	1	0	–1	4	1	1	20 C1	000
2.667	1.359	1	2	1	0	–1	3	1	1	20 B1	000
2.566	1.344	1	2	1	0	1	1	1	2	20 12	000
2.465	1.328	1	2	1	0	1	2	1	2	20 22	000
2.414	1.320	1	2	1	0	1	3	1	2	20 32	000
2.362	1.313	1	2	1	0	–1	1	1	1	20 91	000
2.310	1.305	1	2	1	0	–1	3	1	2	20 B2	000
2.258	1.297	1	2	1	0	–1	2	1	2	20 A2	000
2.205	1.289	1	2	1	0	1	2	1	3	20 23	000
2.153	1.281	1	2	1	0	–1	1	1	2	20 92	000
2.100	1.273	1	2	1	0	–1	2	1	3	20 A3	000
2.046	1.266	1	2	1	0	–1	1	1	3	20 93	000
1.992	1.258	1	2	1	0	–1	1	1	4	20 94	000
1.938	1.250	–1	1	1	0	1	1	–1	0	90 18	000
1.884	1.242	1	2	1	0	–1	1	–1	4	20 9C	000
1.829	1.234	1	2	1	0	–1	1	–1	3	20 9B	000
1.774	1.227	1	2	1	0	–1	2	–1	3	20 AB	000
1.718	1.219	1	2	1	0	–1	1	–1	2	20 9A	000
1.662	1.211	1	2	1	0	1	2	–1	3	20 2B	000
1.606	1.203	1	2	1	0	–1	2	–1	2	20 AA	000

(dB)	GX	v3, k3		v4, k4		v1, k1		v2, k2		HEX	TM3
1.550	1.195	1	2	1	0	–1	3	–1	2	20 BA	000
1.493	1.188	1	2	1	0	–1	1	–1	1	20 99	000
1.435	1.180	1	2	1	0	1	3	–1	2	20 3A	000
1.378	1.172	1	3	1	0	1	1	1	2	30 12	000
1.320	1.164	1	3	1	0	1	2	1	2	30 22	000
1.261	1.156	1	2	1	0	1	1	–1	2	20 1A	000
1.202	1.148	1	3	1	0	–1	2	1	2	30 A2	000
1.143	1.141	1	3	1	0	–1	1	1	2	30 92	000
1.083	1.133	1	3	1	0	–1	1	1	3	30 93	000
1.023	1.125	1	1	1	0	1	1	–1	1	10 19	000
.963	1.117	1	3	1	0	–1	1	–1	3	30 9B	000
.902	1.109	1	3	1	0	–1	1	–1	2	30 9A	000
.840	1.102	1	4	1	0	1	2	1	1	40 21	000
.778	1.094	1	2	1	0	1	2	–1	1	20 29	000
.716	1.086	1	3	1	0	1	2	–1	2	30 2A	000
.653	1.078	1	3	1	0	1	1	–1	2	30 1A	000
.590	1.070	1	3	1	0	–1	3	–1	1	30 B9	000
.527	1.063	1	2	1	0	–1	2	–1	0	20 A8	000
.462	1.055	1	3	1	0	1	3	–1	1	30 39	000
.398	1.047	1	3	1	0	1	2	–1	1	30 29	000
.333	1.039	1	4	1	0	1	1	–1	2	40 1A	000
.267	1.031	1	3	1	0	1	1	–1	1	30 19	000
.201	1.023	1	4	1	0	1	2	–1	1	40 29	000
.135	1.016	–1	3	1	0	1	3	–1	0	B0 38	000
.068	1.008	1	3	1	0	–1	4	–1	0	30 C8	000
.000	1.000	1	0	1	1	–1	0	1	0	01 80	000

9.3 Gain Tables for Programming Transmit GR

Table of Attenuation Values for Programing Receive GR in SICOFI.

Values from 0 db … –12 dB

$A = \{[(V_1 * 2^{-K1} +1) * V_2 * 2^{-K2} +1] * V_3 * 2^{-K3} +1\} * V_4 * 2^{-K4}$

(dB)	A	v3,	k3	v4,	k4	v1,	k1	v2,	k2	HEX
0.000	1.000000000	1	0	1	1	–1	0	1	0	01 80
–0.034	0.996093750	1	4	1	0	1	4	–1	0	40 48
–0.068	0.992187500	1	4	1	0	1	3	–1	0	40 38
–0.137	0.984375000	–1	0	–1	0	–1	6	1	0	88 E0
–0.206	0.976562500	–1	4	1	0	1	2	–1	1	C0 29
–0.276	0.968750000	–1	0	–1	0	–1	5	1	0	88 D0
–0.346	0.960937500	–1	4	1	0	1	1	–1	2	C0 1A
–0.417	0.953125000	–1	3	1	0	1	2	–1	1	B0 29
–0.488	0.945312500	–1	3	1	0	1	3	–1	1	B0 39
–0.561	0.937500000	1	1	1	1	1	1	1	1	11 11
–0.633	0.929687500	1	0	1	1	1	3	–1	3	01 3B
–0.707	0.921875000	–1	3	1	0	1	1	–1	2	B0 1A
–0.780	0.914062500	–1	3	1	0	1	2	–1	2	B0 2A
–0.855	0.906250000	1	1	1	1	1	2	1	1	11 21
–0.930	0.898437500	–1	4	1	0	1	2	1	1	C0 21
–1.006	0.890625000	1	1	1	1	1	3	1	1	11 31
–1.044	0.886718750	–1	3	1	0	1	1	–1	4	B0 1C
–1.083	0.882812500	1	1	1	1	1	4	1	1	11 41
–1.140	0.876953125	–1	4	1	0	–1	5	1	0	C0 D0
–1.160	0.875000000	–1	0	–1	0	–1	3	1	0	88 B0
–1.199	0.871093750	1	1	1	1	–1	5	1	1	11 D1
–1.238	0.867187500	1	1	1	1	–1	4	1	1	11 C1
–1.316	0.859375000	1	1	1	1	–1	3	1	1	11 B1
–1.356	0.855468750	–1	3	1	0	1	2	1	3	B0 23
–1.436	0.847656250	–1	3	1	0	–1	3	1	2	B0 B2
–1.476	0.843750000	1	1	1	1	1	1	1	2	11 12
–1.516	0.839843750	–1	3	1	0	1	3	1	2	B0 32
–1.557	0.835937500	–1	3	1	0	1	2	1	2	B0 22
–1.638	0.828125000	1	1	1	1	1	2	1	2	11 22
–1.720	0.820312500	1	1	1	1	1	3	1	2	11 32
–1.783	0.814453125	1	1	1	1	1	5	1	2	11 52
–1.804	0.812500000	1	1	1	1	–1	1	1	1	11 91
–1.845	0.808593750	1	1	1	1	–1	4	1	2	11 C2
–1.887	0.804687500	1	1	1	1	–1	3	1	2	11 B2
–1.972	0.796875000	1	1	1	1	1	1	1	3	11 13
–2.058	0.789062500	1	1	1	1	1	2	1	3	11 23
–2.101	0.785156250	1	1	1	1	1	3	1	3	11 33
–2.144	0.781250000	–1	3	1	0	1	1	1	1	B0 11
–2.188	0.777343750	1	1	1	1	–1	3	1	3	11 B3
–2.231	0.773437500	1	1	1	1	1	1	1	4	11 14
–2.275	0.769531250	1	1	1	1	1	2	1	4	11 24
–2.320	0.765625000	–1	3	1	0	–1	3	1	0	B0 B0
–2.364	0.761718750	1	1	1	1	1	1	1	5	11 15
–2.409	0.757812500	–1	3	1	0	–1	4	1	0	B0 C0
–2.454	0.753906250	–1	3	1	0	–1	5	1	0	B0 D0
–2.499	0.750000000	–1	0	–1	0	1	1	1	1	88 11

(dB)	A	v3,	k3	v4,	k4	v1,	k1	v2,	k2	HEX
–2.544	0.746093750	1	2	1	1	–1	5	1	0	21 D0
–2.590	0.742187500	1	2	1	1	–1	4	1	0	21 C0
–2.636	0.738281250	1	1	1	1	–1	2	–1	4	11 AC
–2.682	0.734375000	1	2	1	1	–1	3	1	0	21 B0
–2.728	0.730468750	1	1	1	1	1	2	–1	4	11 2C
–2.775	0.726562500	1	1	1	1	–1	2	–1	3	11 AB
–2.821	0.722656250	1	1	1	1	–1	3	–1	3	11 BB
–2.868	0.718750000	1	2	1	1	1	1	1	1	21 11
–2.916	0.714843750	1	1	1	1	1	3	–1	3	11 3B
–2.963	0.710937500	1	1	1	1	1	2	–1	3	11 2B
–3.059	0.703125000	1	1	1	1	–1	2	–1	2	11 AA
–3.156	0.695312500	1	2	1	1	1	3	1	1	21 31
–3.205	0.691406250	1	2	1	1	1	4	1	1	21 41
–3.255	0.687500000	1	1	1	1	–1	1	–1	1	11 99
–3.304	0.683593750	1	2	1	1	–1	4	1	1	21 C1
–3.354	0.679687500	1	2	1	1	–1	3	1	1	21 B1
–3.454	0.671875000	1	2	1	1	–1	2	1	1	21 A1
–3.556	0.664062500	1	2	1	1	1	2	1	2	21 22
–3.607	0.660156250	1	2	1	1	1	3	1	2	21 32
–3.659	0.656250000	–1	2	1	0	1	1	1	2	A0 12
–3.710	0.652343750	1	2	1	1	–1	3	1	2	21 B2
–3.763	0.648437500	1	2	1	1	–1	2	1	2	21 A2
–3.815	0.644531250	1	2	1	1	1	2	1	3	21 23
–3.868	0.640625000	–1	2	1	0	–1	3	1	1	A0 B1
–3.921	0.636718750	1	2	1	1	–1	2	1	3	21 A3
–3.974	0.632812500	–1	2	1	0	–1	4	1	1	A0 C1
–4.028	0.628906250	–1	2	1	0	–1	5	1	1	A0 D1
–4.082	0.625000000	–1	0	–1	0	1	2	1	1	88 21
–4.137	0.621093750	1	3	1	1	–1	4	1	0	31 C0
–4.192	0.617187500	1	3	1	1	–1	3	1	0	31 B0
–4.247	0.613281250	1	2	1	1	–1	2	–1	3	21 AB
–4.302	0.609375000	1	3	1	1	–1	2	1	0	31 A0
–4.358	0.605468750	1	2	1	1	1	2	–1	3	21 2B
–4.414	0.601562500	1	2	1	1	–1	2	–1	2	21 AA
–4.471	0.597656250	1	2	1	1	–1	3	–1	2	21 BA
–4.528	0.593750000	–1	2	1	0	1	2	1	1	A0 21
–4.585	0.589843750	1	3	1	1	–1	3	1	1	31 B1
–4.643	0.585937500	1	3	1	1	1	1	1	2	31 12
–4.701	0.582031250	1	3	1	1	1	2	1	2	31 22
–4.760	0.578125000	1	2	1	1	1	1	–1	2	21 1A
–4.818	0.574218750	1	3	1	1	–1	2	1	2	31 A2
–4.878	0.570312500	–1	1	1	0	1	3	–1	3	90 3B
–4.937	0.566406250	–1	1	1	0	1	4	–1	3	90 4B
–4.998	0.562500000	–1	2	1	0	1	1	1	1	A0 11
–5.058	0.558593750	1	4	1	1	–1	3	1	0	41 B0
–5.119	0.554687500	1	4	1	1	–1	2	1	0	41 A0
–5.180	0.550781250	1	3	1	1	–1	2	–1	2	31 AA
–5.242	0.546875000	–1	1	1	0	–1	2	–1	3	90 AB
–5.305	0.542968750	1	3	1	1	1	2	–1	2	31 2A
–5.367	0.539062500	1	3	1	1	1	1	–1	2	31 1A
–5.430	0.535156250	1	3	1	1	–1	3	–1	1	31 B9
–5.494	0.531250000	–1	2	1	0	–1	3	1	0	A0 B0
–5.558	0.527343750	1	5	1	1	–1	2	1	0	51 A0
–5.623	0.523437500	–1	1	1	0	–1	2	–1	4	90 AC
–5.688	0.519531250	1	4	1	1	1	1	–1	2	41 1A

(dB)	A	v3,	k3	v4,	k4	v1,	k1	v2,	k2	HEX
–5.753	0.515625000	–1	2	1	0	–1	4	1	0	A0 C0
–5.819	0.511718750	–1	1	1	0	–1	2	–1	5	90 AD
–5.886	0.507812500	–1	2	1	0	–1	5	1	0	A0 D0
–5.953	0.503906250	–1	2	1	0	–1	6	1	0	A0 E0
–6.021	0.500000000	–1	0	1	0	–1	1	–1	0	80 98
–6.089	0.496093750	1	0	1	2	–1	1	–1	5	02 9D
–6.157	0.492187500	1	0	1	2	–1	1	–1	4	02 9C
–6.227	0.488281250	1	0	1	2	–1	2	–1	4	02 AC
–6.296	0.484375000	1	1	1	2	–1	3	1	0	12 B0
–6.367	0.480468750	1	0	1	2	1	2	–1	4	02 2C
–6.438	0.476562500	1	0	1	2	–1	2	–1	3	02 AB
–6.509	0.472656250	1	0	1	2	–1	3	–1	3	02 BB
–6.581	0.468750000	1	1	1	2	–1	2	1	0	12 A0
–6.654	0.464843750	1	0	1	2	1	3	–1	3	02 3B
–6.727	0.460937500	1	0	1	2	1	2	–1	3	02 2B
–6.801	0.457031250	–1	3	1	1	1	2	–1	2	B1 2A
–6.876	0.453125000	1	0	1	2	–1	2	–1	2	02 AA
–7.027	0.445312500	1	0	1	2	–1	3	–1	2	02 BA
–7.103	0.441406250	1	1	1	2	1	4	1	1	12 41
–7.142	0.439453125	–1	4	1	1	–1	4	1	0	C1 C0
–7.180	0.437500000	1	0	1	2	–1	1	–1	1	02 99
–7.219	0.435546875	–1	3	1	1	–1	1	1	4	B1 94
–7.258	0.433593750	1	1	1	2	–1	4	1	1	12 C1
–7.298	0.431640625	–1	3	1	1	–1	2	1	3	B1 A3
–7.337	0.429687500	1	1	1	2	–1	3	1	1	12 B1
–7.377	0.427734375	–1	3	1	1	1	2	1	3	B1 23
–7.416	0.425781250	–1	3	1	1	–1	2	1	2	B1 A2
–7.456	0.423828125	–1	3	1	1	–1	3	1	2	B1 B2
–7.496	0.421875000	1	1	1	2	1	1	1	2	12 12
–7.537	0.419921875	–1	3	1	1	1	3	1	2	B1 32
–7.577	0.417968750	–1	3	1	1	1	2	1	2	B1 22
–7.659	0.414062500	1	1	1	2	1	2	1	2	12 22
–7.741	0.410156250	1	1	1	2	1	3	1	2	12 32
–7.782	0.408203125	1	1	1	2	1	4	1	2	12 42
–7.824	0.406250000	1	1	1	2	–1	1	1	1	12 91
–7.866	0.404296875	1	1	1	2	–1	4	1	2	12 C2
–7.908	0.402343750	1	1	1	2	–1	3	1	2	12 B2
–7.993	0.398437500	1	1	1	2	–1	2	1	2	12 A2
–8.078	0.394531250	1	1	1	2	1	2	1	3	12 23
–8.121	0.392578125	1	1	1	2	1	3	1	3	12 33
–8.165	0.390625000	1	1	1	2	–1	1	1	2	12 92
–8.208	0.388671875	1	1	1	2	–1	3	1	3	12 B3
–8.252	0.386718750	1	1	1	2	–1	2	1	3	12 A3
–8.296	0.384765625	1	1	1	2	1	2	1	4	12 24
–8.340	0.382812500	1	1	1	2	–1	1	1	3	12 93
–8.385	0.380859375	1	1	1	2	–1	2	1	4	12 A4
–8.429	0.378906250	1	1	1	2	–1	1	1	4	12 94
–8.474	0.376953125	1	1	1	2	–1	1	1	5	12 95
–8.519	0.375000000	–1	1	1	1	–1	1	–1	0	91 98
–8.565	0.373046875	1	1	1	2	–1	1	–1	5	12 9D
–8.610	0.371093750	1	1	1	2	–1	1	–1	4	12 9C
–8.656	0.369140625	1	1	1	2	–1	2	–1	4	12 AC
–8.702	0.367187500	1	1	1	2	–1	1	–1	3	12 9B
–8.749	0.365234375	1	1	1	2	1	2	–1	4	12 2C
–8.795	0.363281250	1	1	1	2	–1	2	–1	3	12 AB

(dB)	A	v3, k3		v4, k4		v1, k1		v2, k2		HEX	
–8.842	0.361328125	1	1	1	2	–1	3	–1	3	12	BB
–8.889	0.359375000	1	1	1	2	–1	1	–1	2	12	9A
–8.936	0.357421875	1	1	1	2	1	3	–1	3	12	3B
–8.984	0.355468750	1	1	1	2	1	2	–1	3	12	2B
–9.080	0.351562500	1	2	1	2	1	2	1	1	22	21
–9.177	0.347656250	–1	2	1	1	–1	3	1	2	A1	B2
–9.226	0.345703125	1	2	1	2	1	4	1	1	22	41
–9.275	0.343750000	1	2	1	2	–1	1	1	0	22	90
–9.325	0.341796875	1	2	1	2	–1	4	1	1	22	C1
–9.374	0.339843750	1	2	1	2	–1	3	1	1	22	B1
–9.475	0.335937500	1	2	1	2	1	1	1	2	22	12
–9.576	0.332031250	1	2	1	2	1	2	1	2	22	22
–9.628	0.330078125	1	2	1	2	1	3	1	2	22	32
–9.679	0.328125000	1	2	1	2	–1	1	1	1	22	91
–9.731	0.326171875	1	2	1	2	–1	3	1	2	22	B2
–9.783	0.324218750	1	2	1	2	–1	2	1	2	22	A2
–9.836	0.322265625	1	2	1	2	1	2	1	3	22	23
–9.889	0.320312500	1	2	1	2	–1	1	1	2	22	92
–9.942	0.318359375	1	2	1	2	–1	2	1	3	22	A3
–9.995	0.316406250	1	2	1	2	–1	1	1	3	22	93
–10.049	0.314453125	1	2	1	2	–1	1	1	4	22	94
–10.103	0.312500000	–1	1	1	1	–1	1	–1	1	91	99
–10.157	0.310546875	1	2	1	2	–1	1	–1	4	22	9C
–10.212	0.308593750	1	2	1	2	–1	1	–1	3	22	9B
–10.267	0.306640625	1	2	1	2	–1	2	–1	3	22	AB
–10.323	0.304687500	1	2	1	2	–1	1	–1	2	22	9A
–10.379	0.302734375	1	2	1	2	1	2	–1	3	22	2B
–10.435	0.300781250	1	2	1	2	–1	2	–1	2	22	AA
–10.492	0.298828125	1	2	1	2	–1	3	–1	2	22	BA
–10.549	0.296875000	1	2	1	2	–1	1	–1	1	22	99
–10.606	0.294921875	1	2	1	2	1	3	–1	2	22	3A
–10.664	0.292968750	1	2	1	2	1	2	–1	2	22	2A
–10.722	0.291015625	1	3	1	2	1	2	1	2	32	22
–10.780	0.289062500	1	2	1	2	1	1	–1	2	22	1A
–10.839	0.287109375	1	3	1	2	–1	2	1	2	32	A2
–10.898	0.285156250	1	3	1	2	–1	1	1	2	32	92
–10.958	0.283203125	1	3	1	2	–1	1	1	3	32	93
–11.018	0.281250000	1	2	1	2	–1	1	–1	0	22	98
–11.079	0.279296875	1	3	1	2	–1	1	–1	3	32	9B
–11.140	0.277343750	1	3	1	2	–1	1	–1	2	32	9A
–11.201	0.275390625	1	3	1	2	–1	2	–1	2	32	AA
–11.263	0.273437500	1	3	1	2	–1	1	–1	1	32	99
–11.325	0.271484375	1	3	1	2	1	2	–1	2	32	2A
–11.388	0.269531250	1	3	1	2	1	1	–1	2	32	1A
–11.451	0.267578125	1	3	1	2	–1	3	–1	1	32	B9
–11.515	0.265625000	1	3	1	2	–1	1	–1	0	32	98
–11.579	0.263671875	1	3	1	2	1	3	–1	1	32	39
–11.643	0.261718750	1	3	1	2	1	2	–1	1	32	29
–11.708	0.259765625	1	4	1	2	1	1	–1	2	42	1A
–11.774	0.257812500	–1	4	1	2	1	1	–1	0	C2	18
–11.840	0.255859375	1	4	1	2	1	2	–1	1	42	29
–11.907	0.253906250	1	5	1	2	–1	1	–1	0	52	98
–11.974	0.251953125	1	6	1	2	–1	1	–1	0	62	98
–12.041	0.250000000	–1	0	–1	1	–1	1	1	0	89	90

9.4 Index of the Variables Used in the Software

Variable		Possible Value	Used in Program/ File
A.	ABIMP	ZI or Z3	SICOFI/ Specification
	AD, DELAY	Hz and ms	SICOFI/ Specification
	AD, LOWER	Hz and dB	SICOFI/ Specification
	AD, UPPER	Hz and dB	SICOFI/ Specification
	AGX	00, 01, 10, 11	SICOFI/ Control
	AGR	00, 01, 10, 11	SICOFI/ Control
	APOF	dB	SICOFI/ Control
	APRE	dB	SICOFI/ Control
	AT+	dB or ms	SICOFI/ Specification
	AT–	dB or ms	SICOFI/ Specification
B.	BAUTO	Y or N	SICOFI/ Control
	BDF	0, 1, 2 or 3	SICOFI/ Control
	BLIM	REAL value<3.	SICOFI/ Control
	BREP	Y or N	SICOFI/ Control
	BSIGN	+1 or –1	SICOFI/ Control
	BYTE	BYT file name	SICOFI/ Control
C.	CHNR	x, y	SICOFI/ Control
	CKR	Farad	HARRIS SLIC/ input
	CKX	Farad	HARRIS SLIC/ input
D.	DA, DELAY	Hz and ms	SICOFI/ Specification
	DA, LOWER	Hz and dB	SICOFI/ Specification
	DA, UPPER	Hz and dB	SICOFI/ Specification
	DD	Hz and dB	SICOFI/ Specification
	DPOF	Second	SICOFI/ Control
	DPRE	Second	SICOFI/ Control
F.	FB	2 INTEGER values 100 Hz<FB<3.4 KHz	SICOFI/ Control
	FBP	100 Hz<FBP<3.4 KHz	SICOFI/ Control
	FR	Hz	SICOFI/ Specification
	FR	2 INTEGER values	SICOFI/ Control
	FREF	Hz	SICOFI/ Specification
	FSTA	Hz	SICOFI/ Control
	FSTO	Hz	SICOFI/ Control
	FX	2 INTEGER value	SICOFI/ Control
	FZ	2 INTEGER values 100 Hz<FZ<16 KHz	SICOFI/ Control
	FZP	100 Hz<FZP<16 KHz	SICOFI/ Control
G.	GWFB	REAL	SICOFI/ Control
L.	LAW	A or MU	SICOFI/ Specification

Variable		Possible Value	Used in Program/ File
O.	OFF	Z,R,X,B,GR,GX..	SICOFI/ Control
	ON	Z,R,X,B,GR,GX..	SICOFI/ Control
	OPT	Z,R,X,B,GR,GX..	SICOFI/ Control
P.	PB	10<PB<20	SICOFI/ Control
	PLQ	Y or N	SICOFI/ Control
	PSP	5<PZIN+PSP<20	SICOFI/ Control
	PZIN	5<PZIN<20	SICOFI/ Control
R.	RDISP	Y or N	SICOFI/ Control
	REL	Y or N	SICOFI/ Control
	RFIL	see RDISP	
	RIR	Ohm	HARRIS SLIC/ input
	RIX	Ohm	HARRIS SLIC/ input
	RLR	dBr	SICOFI/ Specification
	RLX	dBr	SICOFI/ Specification
	RREF	dB	SICOFI/ Control
	RREFQ	Y or N	SICOFI/ Control
	R0	Ohm	HARRIS SLIC/ input
S.	SHORT	Y or N	SICOFI/ Control
	SIM	Z,R,X,B,GR,GX..	SICOFI/ Control
	SLIC	SLIC file name	SICOFI/ Control
	SPEC	SPEC file name	SICOFI/ Control
	STEP	Hz	SICOFI/ Control
T.	TBM	see BDF	
	TM3	000, 001, 011	SICOFI/ Control
V.	VERSION	Vx.y	SICOFI/ Control
	VOR	REAL	HARRIS SLIC/ input
	VOX	REAL	HARRIS SLIC/ input
	VREF	REAL	SICOFI/ Specification
W.	WFB	REAL	SICOFI/ Control
	WFZ	REAL	SICOFI/ Control
X.	XDISP	Y or N	SICOFI/ Control
	XREF	dB	SICOFI/ Control
	XREFQ	Y or N	SICOFI/ Control

Variable		Possible Value	Used in Program/ File
Z.	ZAUTO	Y or N	SICOFI/ Control
	ZI	COMPLEX	SICOFI/ Specification
	ZICP1	Farad	SICOFI/ Specification
	ZICP2	Farad	SICOFI/ Specification
	ZICS	Farad	SICOFI/ Specification
	ZRE	Hz and dB	SICOFI/ Specification
	ZIRP1	Ohm	SICOFI/ Specification
	ZIRP2	Ohm	SICOFI/ Specification
	ZIRS	Ohm	SICOFI/ Specification
	ZL	COMPLEX	SICOFI/ Specification
	ZLCP1	Farad	SICOFI/ Specification
	ZLCP2	Farad	SICOFI/ Specification
	ZLCS	Farad	SICOFI/ Specification
	ZLIM	REAL value<3.	SICOFI/ Control
	ZLRP1	Ohm	SICOFI/ Specification
	ZLRP2	Ohm	SICOFI/ Specification
	ZLRS	Ohm	SICOFI/ Specification
	ZMIR	Hz and dB	SICOFI/ Specification
	ZR	COMPLEX	SICOFI/ Specification
	ZRCP1	Farad	SICOFI/ Specification
	ZRCP2	Farad	SICOFI/ Specification
	ZRCS	Farad	SICOFI/ Specification
	ZREP	Y or N	SICOFI/ Control
	ZRRP1	Ohm	SICOFI/ Specification
	ZRRP2	Ohm	SICOFI/ Specification
	ZRRS	Ohm	SICOFI/ Specification
	ZSIGN	+1 or –1	SICOFI/ Control
	ZSLI	dB	HARRIS SLIC/ input
	ZXRB	N, O or X	SICOFI/ Control
	Z3	COMPLEX	SICOFI/ Specification
	Z3CP1	Farad	SICOFI/ Specification
	Z3CP2	Farad	SICOFI/ Specification
	Z3CS	Farad	SICOFI/ Specification
	Z3RP1	Ohm	SICOFI/ Specification
	Z3RP2	Ohm	SICOFI/ Specification
	Z3RS	Ohm	SICOFI/ Specification

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Calculating SLIC Parameters of the Transformer SLIC Using M-Parameters and SPICE

Preface

A solution to the problem of modeling new SLICs is submitted by using a combination of an arbitrary **SPICE** program and of the **Conversion Program** SLIC.EXE'.

A detailed description of the Conversion Program is given, and its practical use is exemplified.

To read this application note with profits, the SICOFI Coefficients Program and generalities about the SLIC file format and the SPICE input files should be known.

1 Introduction

To calculate the parameters of a SLIC and to simulate its transfer characteristics (e.g. using the STS 2060 SICOFI coefficients program) it is necessary to write for each new type of SLIC a new program. This is not only a time consuming process, but also new errors introduced into the software model may easily lead to wrong results.

The simulation of analog circuits can also be done by using general programs like **SPICE** (we used the version of the firm MICROSIM: PSPICE); but there is a problem: The output provided by SPICE is not suited as input to the SICOFI coefficients program (unless the SPICE Program contains an "Analog Behavioral Modelling").

Therefore a Conversion Program was written in FORTRAN to convert and calculate the SLIC parameter file (.SLI file) to be used with the SICOFI program from the interpolated SPICE output.

Note: This Conversion Program can also be used to interpolate measured SLIC data when these data are in the form of a SPICE output file (see chapter 4.4).

Terminology:
SLIC: Subscriber Line Interface Circuit.
SICOFI: Signal processing Codec Filter (PEB2060).
In the following we will call "SLIC" the hardware and software corresponding to the analog components in a subscriber line interface circuit **excluding** the SICOFI chip.
Please note that the Conversion Program is also called SLIC.EXE.

2 SICOFI® Software Principle

The main functions of a Subscriber Line Interface Circuit (SLIC) are to provide the BORSHT functions (Battery feeding, Overvoltage protection, Ringing, Signaling, Hybrid function, Testing). In the case of a SLIC being used in combination with the SICOFI, the Hybrid function is splitted into the two-wire to four-wire conversion realized by the SLIC, and the impedance matching, hybrid balancing and gain adjustment provided by the internal filters of the SICOFI.

The other functions (such as off-hook detection, metering, stand-by mode, ringing) may also affect the speech signal, but we will not consider them in the SLIC example described below.

As has been told, the hardware can be split into two parts: The SLIC and its external circuitry on one side and the SICOFI on the other (**see figure 1**).

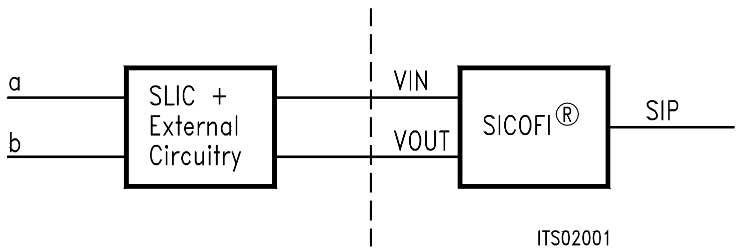


Figure 1
SLIC-SICOFI® Hardware

In a similar way, the software consists of two major sections: The SLIC description file (.SLI file) and the SICOFI program.

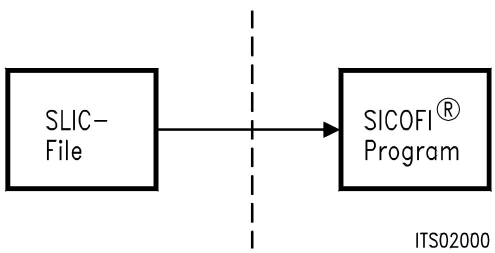


Figure 2
SLIC-SICOFI® Software

According to its functions, a SLIC is a rather complicated circuit (**see figure 12**). Analyzing the SLIC (e.g. for simulating its transfer characteristics) is facilitated in using e.g. PSPICE. Then the SPICE output file, which is not compatible to the SICOFI program, may be adapted by using the Conversion Program 'SLIC.EXE' (**see figure 3**).

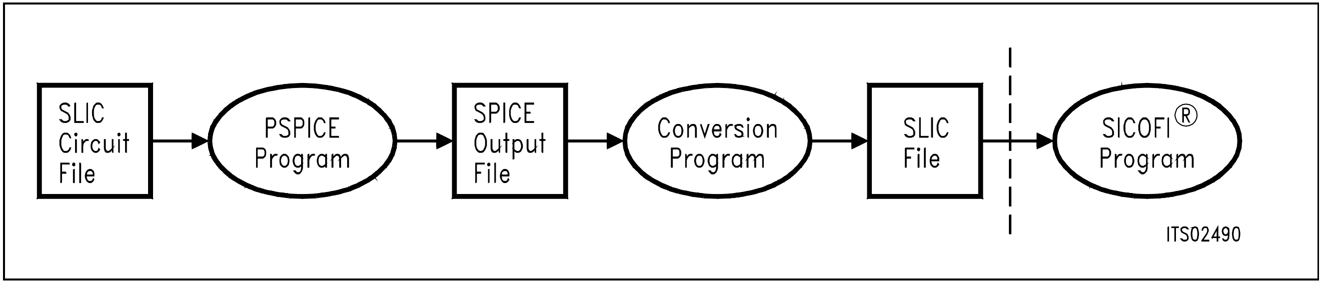


Figure 3
Software Structure

In detail when using SPICE for modelling the SLIC, the complete SICOFI software structure is shown in the following **figure 4**:

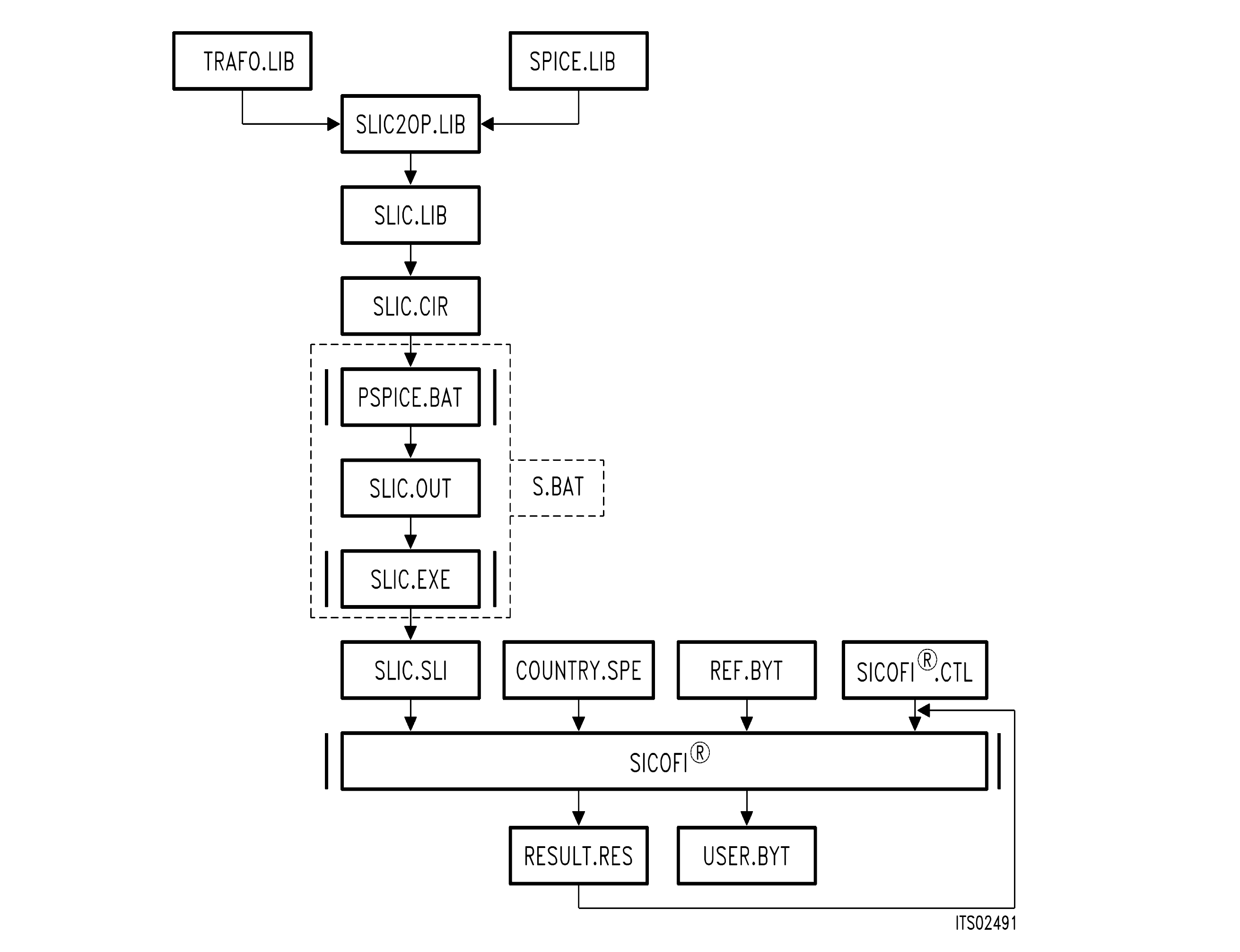


Figure 4
Details of Software Structure

SLIC2OP.LIB
All the specific values concerning the SLIC and its external circuitry (physical data, filter dimensions, ...) are gathered in a SPICE input file SLIC2OP.LIB.
This file gets its non-standard subcircuits (like the transformer data) from the TRAFO.LIB and e.g. the opamp from SPICE library files (LINEAR.LIB).

SLIC.LIB
The file SLIC.LIB provides the description of a particular SLIC circuit. The main advantage of this procedure is, that the file SLIC.LIB acts like a kind of black box containing the actual SLIC: While the black box and its connections remain unchanged, the SLIC circuitry inside the box can easily be replaced by simply changing (the names of) the SLIC sub-circuit and it’s library (’SLIC2OP.LIB’).
In the following the various available library files and their use is reviewed.

TRAFO.LIB contains a description of an arbitrary transformer. The transformer components have to be matched to the actual data.

SLIC.CIR contains the necessary test circuits to generate the SPICE output file.
This file must not be changed.

The SPICE program analyzes the test circuits and calculates voltages and currents from which the M-parameters are deduced.

The SLIC program SLIC.EXE then converts the output of SPICE to a file SLIC.SLI which is compatible to the SICOFI Coefficients Program and which contains the transmission characteristics of the SLIC in the form of the M-parameters.

For easy use, the SPICE and the conversion programs are combined in a batch file S.BAT.
This batch file is run as follows:

S SLIC <ENTER> (Without the .OUT suffix)

SLIC.SLI is a transfer file (output/input file) between the SLIC program and the SICOFI program to introduce the SLIC circuit data (M-parameters) into the SICOFI program.

Auxiliary Files:

COUNTRY.SPE is an input file of the SICOFI program describing the customer specification (CCITT etc. ...) and measurement configuration parameters (e.g. termination impedance).

REF.BYT is an input file of the SICOFI program which defines a frame into which the program can write the newly calculated coefficients together with some predefined commands (required for sending the SICOFI coefficients from the Peripheral Board Controller PBC (PEB 2051) to the SICOFI) and stores them in a USER.BYT file.

SICOFI.CTL is the control file of the SICOFI program. It contains the data controlling the optimization and simulation processes.

The SICOFI program generates the SICOFI coefficients and simulates the theoretical transfer functions of the set SLIC + SICOFI.

RESULT.RES is the output file of the SICOFI program.
It contains the coefficients for programming the SICOFI and a list of the calculated results corresponding to various measurements on the set SICOFI + SLIC. (e.g. return loss, frequency response, echo return loss, etc ...).

3 The Conversion Program SLIC.EXE

3.1 Features

- The Conversion Program is written in MICROSOFT FORTRAN and runs on an IBM PC AT or compatible.
- INPUT: For the input to the Conversion Program serves the circuit description file 'SLIC.OUT' which is generated by SPICE (or a file generated by measurements).
  This file has the format of a SPICE ac analysis containing variable values in the frequency range of 10 to 3990 Hz in steps of 10 Hz. If not all these frequency values are contained (for instance by the use of steps larger than 10 Hz in the SPICE ac analysis in order to reduce the calculation time of SPICE), the missing values and frequencies are **interpolated**.
- OUTPUT: The program converts the SPICE output file into a SLIC file (with suffix .SLI) describing the characteristics of a SLIC, and being suitable as input for the SICOFI coefficients program containing the parameter ZSLI (minimal attenuation of the SLIC at the four wire side) and the M-parameters of the SLIC for each frequency from 10 to 3990 Hz in steps of 10 Hz.
- BATCH MODE Facility: The program can be started from the keyboard or from a **batch file** (the arguments are on the same command line).
- Flexibility: The program processes the input file with flexibility by recognizing keywords in the SPICE output file:
  - **the order** of the different ac analyses is **indifferent**
  - **the ZSLI analysis can be missing** in order to reduce the calculation time (ZSLI is then set to the default value of 0.5).
  - The program recognizes three kinds of circuits: two for the M-parameter and one for the ZSLI parameter calculation. Due to the structure of the circuits being all the same, and only the loads at ring and tip being different, there might be **more circuits** available for the ZSLI calculation, however.

3.2 Batch File S.BAT

For ease of use, the steps always following each other of SLIC circuit analysis by SPICE and adaptation of the resulting output file SLIC.OUT to an input file being compatible to the SICOFI program have been combined to a batch file S.BAT. Thus in applying S.BAT to the circuit description file SLIC.CIR, the resulting output file SLIC.SLI is directly to be used as input to the SICOFI program. Circuit analysis and conversion of the intermediate results is performed by simply calling S SLIC.

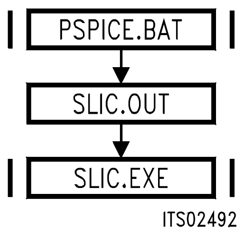


Figure 5
Contents of Program S.BAT

3.3 SLIC Description by Parameters

According to its functionality the SLIC operates as a three port. To describe its electrical properties the parameters to be used in the SICOFI program are the M-parameters and the ZSLI-value. They are defined as follows:

3.3.1 M-Parameters

The SLIC and its external circuitry are accessible through a three port (**see figure 6**).

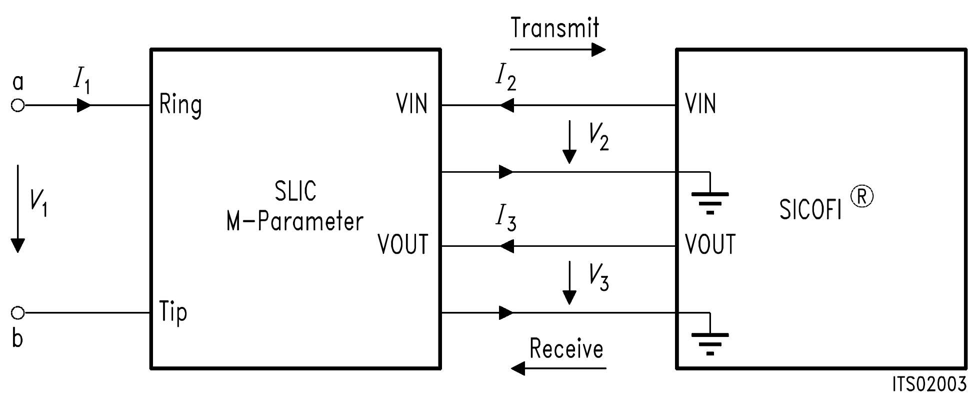
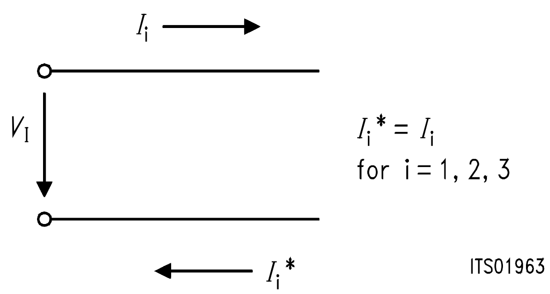


Figure 6
SLIC and its External Circuitry as a Three Port

I_1, I_2 and I_3 are port currents and V_1, V_2 and V_3 are port voltages. This circuit can be described by the following equation system:

(1) $I_1 = M11 \times V_1 + M12 \times V_3 + M13 \times I_2$
(2) $V_2 = M21 \times V_1 + M22 \times V_3 + M23 \times I_2$
(3) $I_3 = M31 \times V_1 + M32 \times V_3 + M33 \times I_2$

Note: Description of a port:



When the SLIC is connected to the SICOFI, we can assume that:

– $I_2 = 0$ because of the high SICOFI input impedance.

(In special cases the SICOFI input impedance can be included in the three-port model).

– I_3 is not relevant in the following calculations because the SICOFI works as an ideal voltage generator.

(The SICOFI output impedance of about 10 Ω may be included in the SLIC model).

According to the above remarks the equation system can be reduced to a pair of equations containing just four M-parameters:

(4) $I_1 = M11 \times V_1 + M12 \times V_3$
(5) $V_2 = M21 \times V_1 + M22 \times V_3$

These parameters M11, M12, M21, M22 fully describe the SLIC and its external circuitry. They are defined as shown in **figures 7** through **10**.

Please verify that circuits of **figures 7** and **9** and of **figures 8** and **10** respectively are identical!

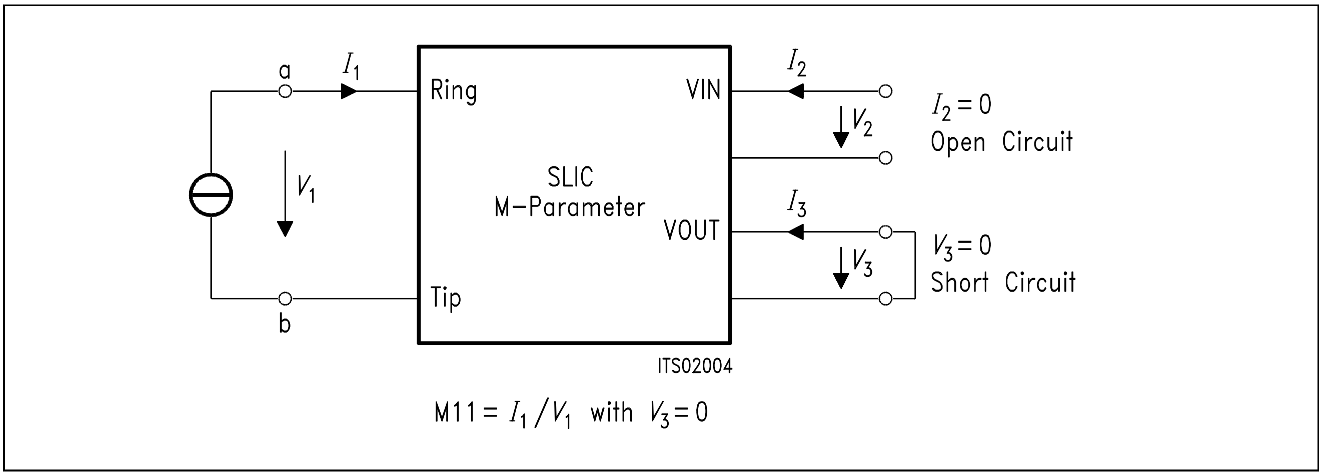


Figure 7
Definition of SLIC M11-Parameter

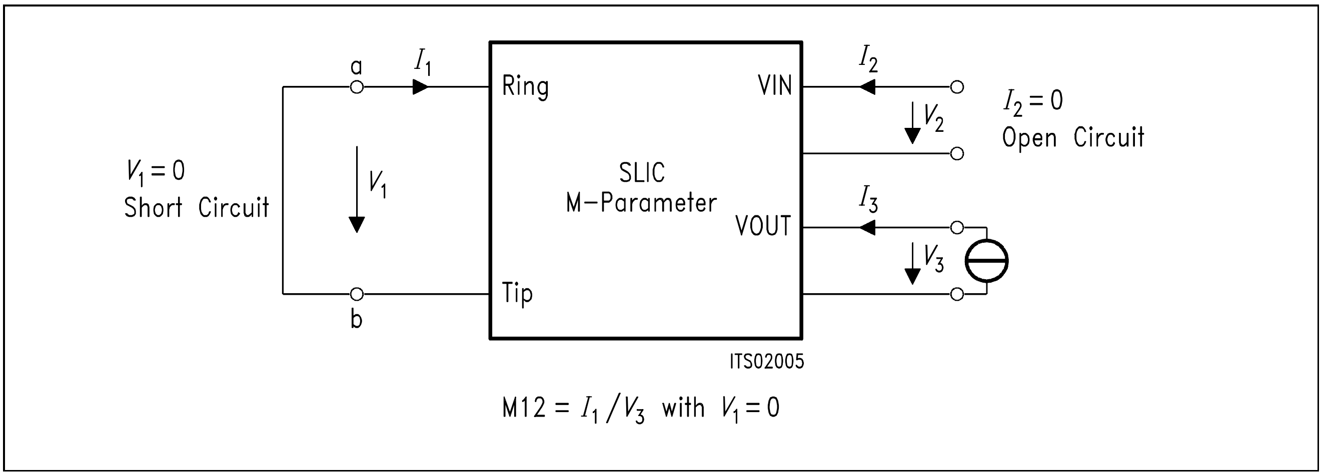


Figure 8
Definition of SLIC M12-Parameter

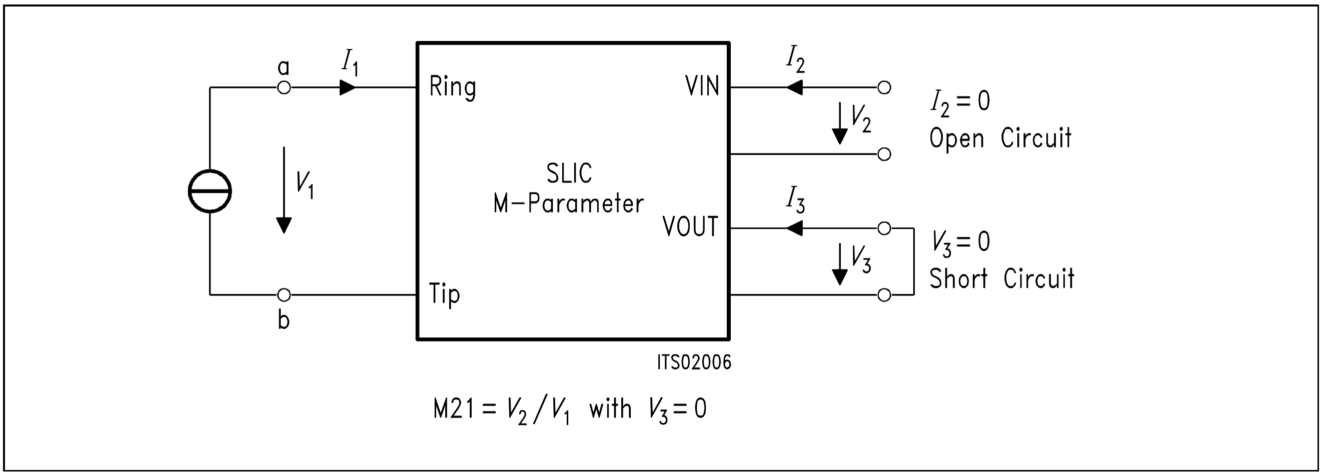


Figure 9
Definition of SLIC M21-Parameter

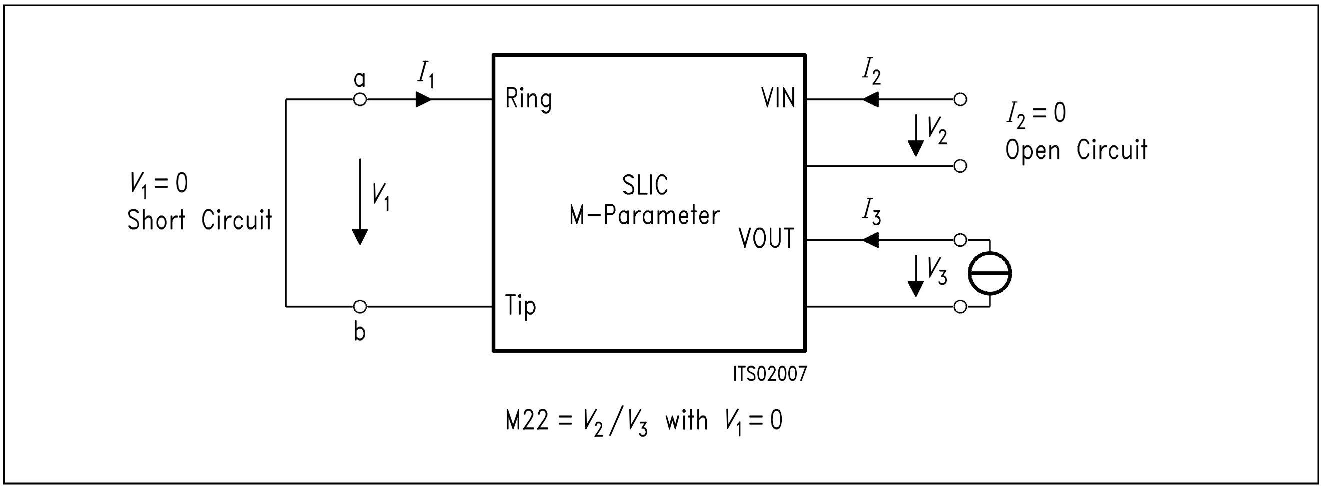


Figure 10
Definition of SLIC M22-Parameter

3.3.2 ZSLI

ZSLI is the **minimal attenuation** (resp. maximal gain) of the SLIC 4-wire side while the a/b lines are terminated by the terminal impedance Z_t.

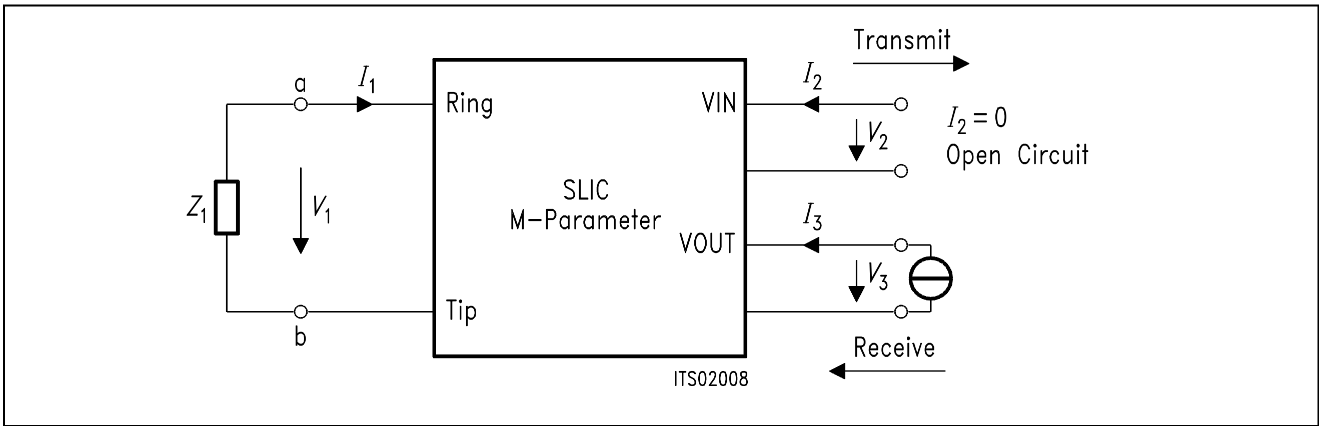


Figure 11
Definition of SLIC ZSLI

ZSLI is used by the SICOFI program during automatic calculation of Z-filter coefficients as a reference to check for possible oscillations in the SICOFI Z-filter + SLIC loop.

The value is in dB and is expressed as attenuation:

$$\text{ZSLI} = -20 \times \log (V_2/V_3)$$

Please verify that as V_2 is larger than V_3, ZSLI is a negative quantity.

In practice the attenuation of the loop "SLIC input to SLIC output" is measured over the whole frequency band 0 – 16 kHz for different terminating impedances Z_t (**see chapter 4.2.1**). The worst case (the smallest attenuation resp. the greatest gain) then is taken for ZSLI.

The use of SPICE allows to obtain the ZSLI value without doing measurements.

Note: According to the Nyquist criteria, the attenuation of the closed loop "Z filter – SLIC" must be greater than 1 (gain < 0 dB) in the frequency band 0 – 16 kHz in order to avoid any oscillation.

4 Example

To exemplify circuit synthesis using SPICE together with the SICOFI program, a circuitry consisting of a transformer SLIC and a SICOFI according to **figure 12** is analyzed. While the SLIC is a real circuit of fixed properties, the SICOFI is tuned by the SICOFI program as to meet particular specifications imposed by country specific requirements.

Results of simulation and measurements on a sample circuit are compared.

4.1 The SLIC

The SLIC used for probing the SPICE program is a transformer SLIC with series feeding and two operational amplifiers, used in certain USA Applications.

With the names of the different nodes filled in, the circuit is shown in figure 12. This circuit is described for SPICE in the file 'SLIC2OP.LIB' (**see Appendix A**).

Most of the components of the SLIC are standard components and can be found in the SPICE library except the transformer. Hence this component has to be modelled separately.

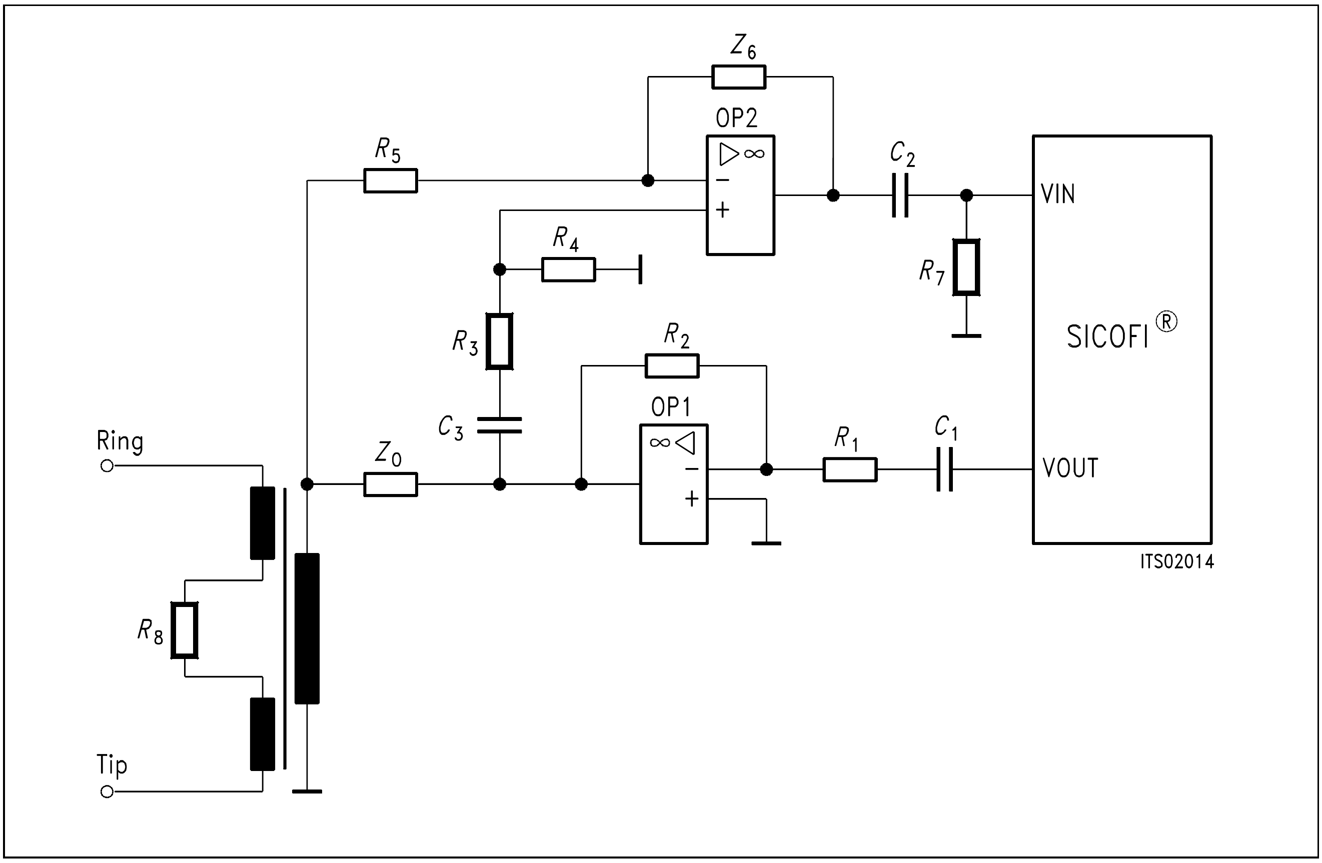


Figure 12
SLIC Circuit

4.1.1 The Transformer

The transformer (Siemens ordering code: V3301-G1023-B194-4 BW/W9) consists of two primary and one secondary coils wound on an iron core Permenorm 5000 H2 1000 NH.

The equivalent circuit data are calculated from measurements.

4.2 Determination of the Equivalent Circuit Components

To determine the equivalent circuit components of the circuitry involved, a series of measurements are taken. As several of these components are not directly accessible by measurement, they are calculated from measured data.

4.2.1 Modelling the Transformer

The transformer can be described in SPICE by an equivalent circuit. In this circuit each coil is substituted by its inductance, in series with its copper resistance and in parallel with its winding capacitance (**see figure 13**). The inductors are coupled by a common coupling factor k.

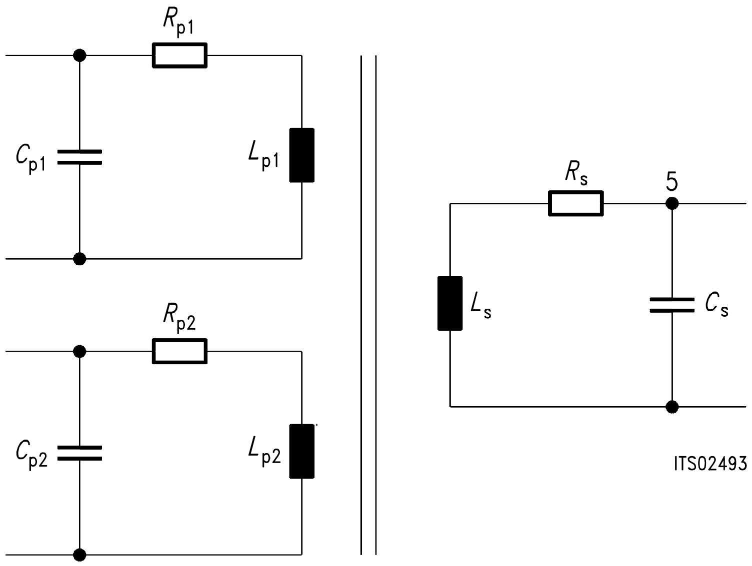


Figure 13
Equivalent Circuit for Transformer Used in SPICE

The values of the different components of this equivalent circuit are calculated from the measurements on the transformer.

4.2.2 Measurements on the Transformer

The whole measurement is done in 4 steps:

1. Measurement of the copper resistances of the two primary and of the secondary coils (R_{p1}, R_{p2} and R_s) using a simple Ohmmeter.

R_{p1} = 33 Ω
R_{p2} = 33 Ω
R_s = 66 Ω

2. Measurement of the respective transformer resonance frequencies (imaginary part = 0), with open circuit at the other coils, by using an impedance analyzer.
[parallel equivalent circuit]

– first primary coil → f_{p1} = 64.03 kHz
– second primary coil → f_{p2} = 63.38 kHz
– secondary coil → f_s = 62.67 kHz

3. Measurement of winding inductances L_{p1m}, L_{p2m} and L_{sm}, with open circuit at the other coils at a low frequency (f_m = 100 Hz).
[series equivalent circuit]

L_{p1m} = 0.374 H
L_{p2m} = 0.374 H
L_{sm} = 1.473 H

4. Measurement of the stray inductances with a short circuit at the other coils at the resonance frequency.
[series equivalent circuit]

– first primary coil at f_{p1} → L_{kp1} = 30.3 µH
– second primary coil at f_{p2} → L_{kp2} = 30.6 µH
– secondary coil at f_s → L_{ks} = 2.108 mH

4.2.3 Calculations on the Transformer

With the measurements of 4.2.2 the only true components determined yet are the copper resistances of the coils; to get the rest of the component values (inductances and capacitances) some calculations have to be performed.

– Determination of correction factors [1]:

$ß_{p1} = f_m / f_{p1}$ $ß_{p2} = f_m / f_{p2}$ $ß_s = f_m / f_s$

$$ß_{p1} = f_m / f_{p1} = 100/64.03E3 = 1.562E–3$$
$$ß_{p2} = f_m / f_{p2} = 100/63.38E3 = 1.578E–3 \quad (6)$$
$$ß_s = f_m / f_s = 100/62.67E3 = 1.596E–3$$

As is to be seen, the β's are rather small quantities compared to unity and may be neglected in many cases.

– Calculation of the actual inductances [1]:

(7) $L_{p1} = L_{p1m}(1 - ß_{p1}^2)$ $L_{p2} = L_{p2m}(1 - ß_{p2}^2)$ $L_s = L_{sm}(1 - ß_s^2)$

$L_{p1} = 0.374$ H
$L_{p2} = 0.374$ H
$L_s = 1.473$ H

– Calculation of the stray factors [1]:

(8)

$$\sigma_{p1} = \frac{L_{kp1}}{L_{p1}} \qquad \sigma_{p2} = \frac{L_{kp2}}{L_{p2}} \qquad \sigma_s = \frac{L_{ks}}{L_s}$$

$\sigma_{p1} = 8.10 \times 10^{-5}$ $\sigma_{p2} = 8.18 \times 10^{-5}$ $\sigma_s = 1.43 \times 10^{-3}$

– Calculation of the turns ratio [1]:

(9)

$$n = \sqrt{\frac{L_s}{L_{p1}}} = \sqrt{\frac{L_s}{L_{p2}}}$$

$n = 1.98$

– Evaluation of the winding capacitances [1]:

(10)

$$C_{p1} = \frac{n}{(2\Pi f_s)^2 L_{p1}\,\sigma_{p1}} \qquad C_{p2} = \frac{n}{(2\Pi f_s)^2 L_{p2}\,\sigma_{p2}} \qquad C_s = \frac{1}{(2\Pi f_{p2})^2 L_s\,\sigma_s n}$$

$C_{p1} = 107$ nF $C_{p2} = 106$ nF $C_s = 5.9$ nF

– Calculation of the coupling factor [1]:

(11)

$$k_{p1} = \frac{L_{p1} - L_{kp1}}{L_{p1}} \qquad k_{p2} = \frac{L_{p2} - L_{kp2}}{L_{p2}} \qquad k_s = \frac{L_s - L_{ks}}{L_s}$$

$k_{p1} = 0.99992$ $k_{p2} = 0.99992$ $k_s = 0.99857$

Because only one coupling factor for all three coils is required by SPICE and because there are small differences among the three calculated coupling factors due to measurement errors, the average of these coupling factors is taken.

$$k = (k_{p1} + k_{p2} + k_s)/3 = 0.999468$$

With the parameters and the names of the different nodes, the equivalent circuit of the transformer is given in **figure 14** below.
This circuit is described in the SPICE file 'TRAFO.LIB' (**see Appendix B**).

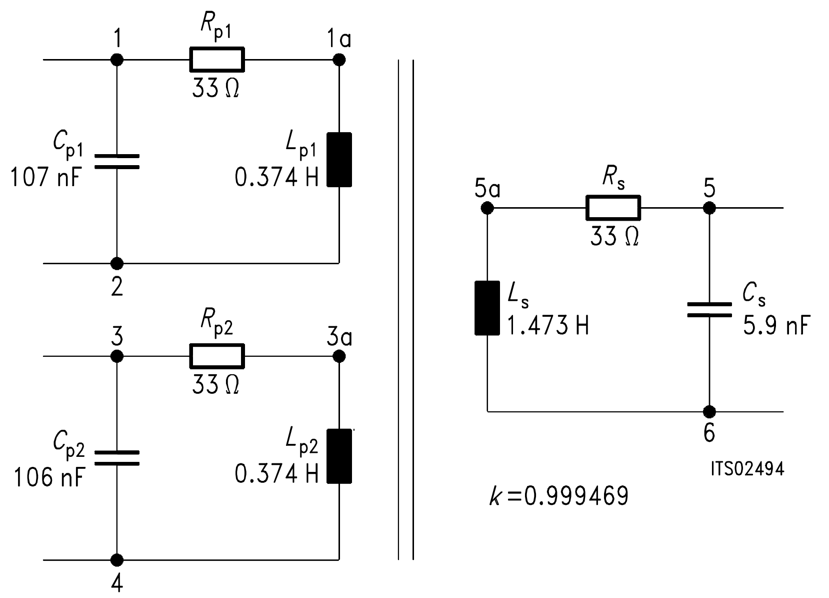


Figure 14
The Complete Equivalent Circuit of the Transformer

4.3 The SPICE Input File 'SLIC.CIR'

The circuit description file SLIC.CIR is the input file from which SPICE generates all the output variables necessary for the Conversion Program.

According to **chapter 3.3** for calculating the M-parameters **two** circuits are simulated, one circuit for the parameters M11 and M21 (**figures 7 and 9**), and one circuit for calculating the parameters M12 and M22 (**figures 8 and 10**).

The M11 and M21 parameters are calculated from the frequency response of the complex variables

V_1, the voltage between "ring" and "tip" (port 1 of the SLIC),
V_2, the voltage at V_{IN} (port 2 of the SLIC), and
I_1, the current flowing into "ring" (into port 1 of the SLIC).

The M12 and M22 parameters are calculated from the frequency response of the complex variables

V_2, the voltage at V_{IN} (port 2 of the SLIC),
V_3, the voltage at V_{OUT} (port 3 of the SLIC), and
I_1, the current flowing into the ring port of the SLIC.

The description for SPICE of these two circuits can be found in the first part of the file '**SLIC.CIR**' (**see Appendix C**).

For gaining the minimal attenuation of the SLIC at the four wire side (ZSLI), accordingly three circuits are simulated with the following terminating conditions at port 1:

one with a short circuit between "ring" and "tip",
one with a 600 Ω load between "ring" and "tip", and
one with an open circuit between "ring" and "tip",

yielding three values

$$\text{ZSLI} = -20 \times \log(V_2/V_3)$$

The magnitudes of the voltages V_2 and V_3 at V_{IN} and V_{OUT} result from a SPICE ac analysis. The minimum value out of these ZSLI's is taken for calculations.

The description for SPICE of these three circuits are found in the second part of the file 'SLIC.CIR' (**see Appendix C**).

4.4 Format of the SPICE Output File

The output file of SPICE generated with the 'SLIC.CIR' circuit description file consists of two to five parts containing a circuit description and a frequency analysis.

Each of the parts is arranged as follows (keywords which are recognized by the Conversion Program are shown in **bold**):

A title line with one or two keywords to identify the circuit. The keywords can be one of the following:

- **M11** and **M21**
- **M12** and **M22**
- **ZSLI**

.

.lib <name of library with the SLIC>
description of test circuit
XSLIC ring tip + 5 V – 5 V VIN VOUT <name of SLIC>

.

commands for starting analysis

.

.end

.

analysis output of SPICE

.

AC ANALYSIS

.

one of these lines:

FREQ VR(VIN) VI(VIN) VR(ring,tip) VI(ring,tip) *or*
FREQ IR(vmeasure) II(vmeasure) *or*
FREQ VR(VIN) VI(VIN) VR(VOUT) VI(VOUT) *or*
FREQ V(VOUT) V(VIN)

d epending on the part of the output

empty line
empty line

1.000E+01 1.000E+00 7.167E– 08 ....

.

all points of ac analysis

.

1.600E+04 1.000E+00 1.993E– 04 ....

line without scientific reals.

In case of M-parameter calculations the second part of the analysis follows:

AC ANALYSIS
.
FREQ IR(vmeasure) II(vmeasure)
empty line
empty line
1.000E+01 1.000E+00 7.167E– 08 ....
.
all points of ac analysis
.
1.600E+04 1.000E+00 1.993E– 04 ....
line without scientific reals

End of file or next part of SPICE output

The first column of the frequency analysis contains the particular frequency value, the adjacent pair of columns contains the corresponding real and imaginary parts of the variable for that frequency.

4.5 How to Use the Conversion Program ’SLIC.EXE’

To calculate the parameters of a SLIC, procede as follows:

1. Set up a library file containing the transformer data.
2. Prepare a library file with the description of the SLIC subcircuit for PSPICE.
3. Put the name of this library file and of the subcircuit to the proper place in the ’SLIC.LIB’ file.
4. Execute the PSPICE program with the ’SLIC.CIR’ file as argument.
5. Execute the Conversion Program ’SLIC.EXE’ with the arguments ’SLIC.OUT SLIC.SLI’
6. Then run the SICOFI program. An example of control file is given in ’SPICE.CTL’

Note: Steps 3 and 4 are put together in the batch file ’S.BAT’.
(Use ’**S SLIC**’ without extension).

Example:
Calculation of a SLIC ’SLIC2OP’ in the library file ’SLIC2OP.LIB’ (to know more about how to use this file, please refer to the manual of PSPICE [2]). Editing of the words in **bold** of the file ’SLIC.LIB’ (**see figure 15**).

Figure 15

The File ’SLIC.LIB’ Before Editing.
Files xxxxxxxx.LIB and yyyyyyyy are renamed to the correct library file name and to the particular SLIC subcircuit name respectively.

```
* file for accessing the proper SLIC with no changes in the
SLIC.CIR file

* change "SLIC2OP.LIB" into the name of the library file with
your particular SLIC

* subcircuit
.LIB xxxxxxx.LIB

* change the model name "SLIC2OP" for the name of your
particular subcircuit
.subckt SLIC   ring tip +5v -5v Vin Vout
xownSLIC       ring tip +5v -5v Vin Vout   yyyyyyyy
.ends SLIC
```

The file after editing is shown in **figure 16**:

Figure 16

The File 'SLIC.LIB' After Editing.

The bold faced words have been changed.

```
* file for accessing the proper SLIC with no changes in the
SLIC.CIR file

* change "SLIC2OP.LIB" to the name of the library file with
your particular SLIC

* subcircuit
.lib SLIC2OP.LIB

* change the model name "SLIC2OP" to the name of your
particular subcircuit
.subckt SLIC   ring tip +5v -5v Vin Vout
xownSLIC       ring tip +5v -5v Vin Vout   SLIC2OP
.ends SLIC
```

Now the batch file 'S.BAT' can be executed and if there are no errors reported, the output file 'SLIC.SLI' can be used in the SICOFI program.
For the use of the SICOFI program please refer to the Software Description of the STS 2060 SICOFI COEFFICIENTS PROGRAM [3]

4.6 Format of the SICOFI® Input File

The SICOFI input file is listed below (keywords are in bold):

```
* PSPICE library used for calculating                         | comment
* .lib SLIC.lib                                               | lines
* PSPICE model used for calculating                           | beginning
* M-parameters                                                | with "*"
* xSLIC ring tip +5v -5v Vin 0 SLIC
ZSLI
.41905
M11-TABLE
       10.000000   2.978000E-03  -8.219000E-04
       20.000000   2.856892E-03  -7.672104E-04
              .................              .........................
......................
       3980.000000 1.671095E-03  -9.220666E-05
       3990.000000 1.671000E-03  -9.240000E-05
M12-TABLE
       10.000000   5.185000E-04   1.064000E-03
       20.000000   6.787197E-04   9.931213E-04
              .................              .........................
......................
       3980.000000 2.234000E-03  -1.258381E-04
       3990.000000 2.234000E-03  -1.262000E-04
M21-TABLE
       10.000000   1.864000E-01  -3.890000E-01
       20.000000   3.144297E-02  -3.902608E-01
              .................              .........................
......................
       3980.000000    -1.515000   9.331572E-02
       3990.000000    -1.515000   9.361000E-02
M22-TABLE
       10.000000   5.157000E-01  -2.201000E-01
       20.000000   3.803514E-01  -2.266998E-01
              .................              .........................
......................
       3980.000000    -1.515000   9.331572E-02
       3990.000000    -1.515000   9.361000E-02
```

The leading comment lines (beginning with "*) document which SLIC is used.
The first column of the M-Parameter Tables indicates the frequency value, from 10 to 3990 Hz in steps of 10 Hz. The second column gives the real part and the third column the imaginary part values.
These three values are separated by at least a single space character. Every real number must contain a decimal point. (Fortran "REAL" format.)

4.7 Results

The SLIC was simulated using the parameters ’SLIC.SLI’ of the SLIC ’SLIC2OP’ in ’SLIC2OP.LIB’ (Appendix B), and coefficients were calculated.
The result file of the SICOFI program was stored in ’SLIC.RES’ and the calculated programming bytes in ’SLIC.BYT’.
With these bytes the SICOFI has been programmed and measurements have been taken with a "PCM 4" from Wandel & Goltermann, using the real SLIC in the STUT 2060 test board as shown in Appendix E.
The measurements comprise the levels in transmit direction (AD) and in receive direction (DA), the attenuation distortion (AD and DA), the transhybrid loss (DD), and the 2-wire impedance return loss.
The plots of measurements can be found in Appendix F.
The plot masks correspond to CCITT Recommendations G.712 and G.714

4.8 Comparison of Measurements and Simulation

The results of the simulation of the return loss with Z-filter OFF (by the means of the SIM option of the SICOFI program) and of the measured data for the return loss are compared in the last diagram of Appendix F. The differences between the respective curves may be due to imperfections of the transformer model.
The measurements show that the specifications of the SLIC for USA applications (Appendix G ’USA.SPE’) are met. Simulated and measured data of the SLIC’s return loss are in good agreement.

Conclusion:
Using this combination of the PSPICE program and of the ’SLIC.EXE’ Conversion Program, correct coefficients for the SICOFI are easily calculated.

5 Literature

[1] Der Übertrager in der Nachrichtentechnik.
Dipl.-Ing. Günter H. Domsch
Akademische Verlagsgesellschaft
Geest & Portig K.-G.
Leipzig

[2] PSPICE
Microsim Corporation
20 Fairbanks, Irvine, California 92718

[3] Software Description STS 2060, SICOFI Coefficients Program
Siemens A.G.

Appendix A

The Library File 'SLIC2OP.LIB'

```
Transformer SLIC for USA-application with 2 opamps
.LIB linear.lib
.LIB trafo.lib
.SUBCKT SLIC2OP ring tip +5V -5V VIN VOUT
*power supply for the 3 opamps
*Vcc  +5v 0   5V
*Vee  0 -5v   5V
C4    +5V 0   1µF
C5    0 -5v   1µF
*Slic, connections are ring and tip
Xtrafo ring 1 2 tip 3 0 trafo
Rtrafo 1 2 220
*Impedance conversion Vin
R5    3 10    20k
R0    3 7     243
C3    7 8     330nF
R3    8 9     15k
R4    9 0     24k
*---------------------------- amplifier ---------------------------
--
*connections:
*             non-inverting input
*             |       inverting input
*             |       |       positive power supply
*             |       |       |       negative power supply
*             |       |       |       |       output
*             |       |       |       |       |       type
*             |       |       |       |       |       |
Xopamp1       9       10      +5V     -5V     11      LM324
R6    10 11   75k
C2    11 VIN  1µF
R7    VIN 0   10k
*Impedance conversion VOUT
Xopamp2 0 12 +5V -5V 7 LM324
R2    7  12   200k
R1    12 13   150k
C1    13 VOUT  1µF
.ENDS
```

Appendix B

The Library File 'TRAFO.LIB'

```
trafo
.subckt trafo 1 2 3 4 5 6
c1   1 2      1.0725E-12
c2   3 4      1.0617E-12
c3   5 6      3.2766E-12
rl1  1 1a     33
rl2  3 3a     33
rl3  5 5a     66
l1   1a 2     0.374
l2   3a 4     0.374
l3   5a 6     1.473
k    l1 l2 l3  0.999468682
.ends
```

Appendix C 1

The Test Circuit File 'SLIC.CIR'

```
circuit for calculating M-parameters M11 M21 (VOUT = 0)
*
*Version 3.0
*
*To change the SLIC to your own SLIC just change in the slic.lib file
all the library and SLIC
*names used in the subcircuit
*
.lib slic.lib
Vcc +5V 0 5V ; Positive Power supply
Vee 0 -5V 5V ; Negative Power supply
xslic ring tip +5V -5V VIN 0 slic
VOSC 1 tip ac 1
Vmeasure 1 ring 0 ; for measurement of current going in ring-port
rdum tip 0 10T ; for rejecting 'floating' errors from spice,see spice
manual
.ac lin 39  10  3990
.print ac  vr([VIN]) vi([VIN]) vr([ring],[tip]) vi([ring]),[tip])
.print ac  ir(Vmeasure) ii(Vmeasure)
.options nomod
.end
circuit for calculating M-parameters M12 M22 (input short circuit)
.lib slic.lib
Vcc +5V 0 5V ; Positive Power supply
Vee 0 -5V 5V ; Negative Power supply
xslic ring tip +5V -5V VIN VOUT slic
Vmeasure tip ring 0 ; for measurement of current going in ring-port
VOSC VOUT 0 ac 1
rdum ring 0 10T ; for rejecting 'floating' errors from spice,see spice
manual
.ac lin 39  10  3990
.print ac  vr([VIN]) vi([VIN]) vr([VOUT]) vi([VOUT])
.print ac  ir(Vmeasure) ii(Vmeasure)
.options nomod
.end
circuit for calculating ZSLI0 (ring and tip short circuit)
.lib slic.lib
Vcc +5V 0 5V ; Positive Power supply
Vee 0 -5V 5V ; Negative Power supply
xslic ring ring +5V -5V VIN VOUT slic
VOSC VOUT 0 ac 1
rdum ring 0 10T ; for rejecting 'floating' errors from spice,see spice
manual
.ac lin 30  10  16.0E3
```

```
.print ac  V([VOUT]) V([VIN])
.options nomod
.end
circuit for calculating ZSLI600 (ring and tip loaded with 600 Ohm)
.lib slic.lib
Vcc +5V 0 5V ; Positive Power supply
Vee 0 -5V 5V ; Negative Power supply
xslic ring tip +5V -5V VIN VOUT slic
VOSC VOUT 0 ac 1
rload ring tip 600
```

Appendix C 2

The Test Circuit File 'SLIC.CIR'

```
rdum ring 0 10T ; for rejecting 'floating' errors from spice,see spice
manual
.ac lin 30  10  16.0E3
.print ac V([VOUT]) V([VIN])
.options nomod
.end
circuit for calculating ZSLIopen (ring and tip open circuit)
.lib slic.lib
Vcc +5V 0 5V ; Positiv Power supply
Vee 0 -5V 5V ; Negativ Power supply
xslic ring tip +5V -5V VIN VOUT slic
VOSC VOUT 0 ac 1
rload ring tip 10T ; for rejecting 'floating' errors from spice,see
spice manual
rdum ring 0 10T
.ac lin 30  10  16.0E3
.print ac  V([VOUT]) V([VIN])
.options nomod
.end
```

Appendix D

The Converting Program in Pseudo Language.

Available on request

Appendix E

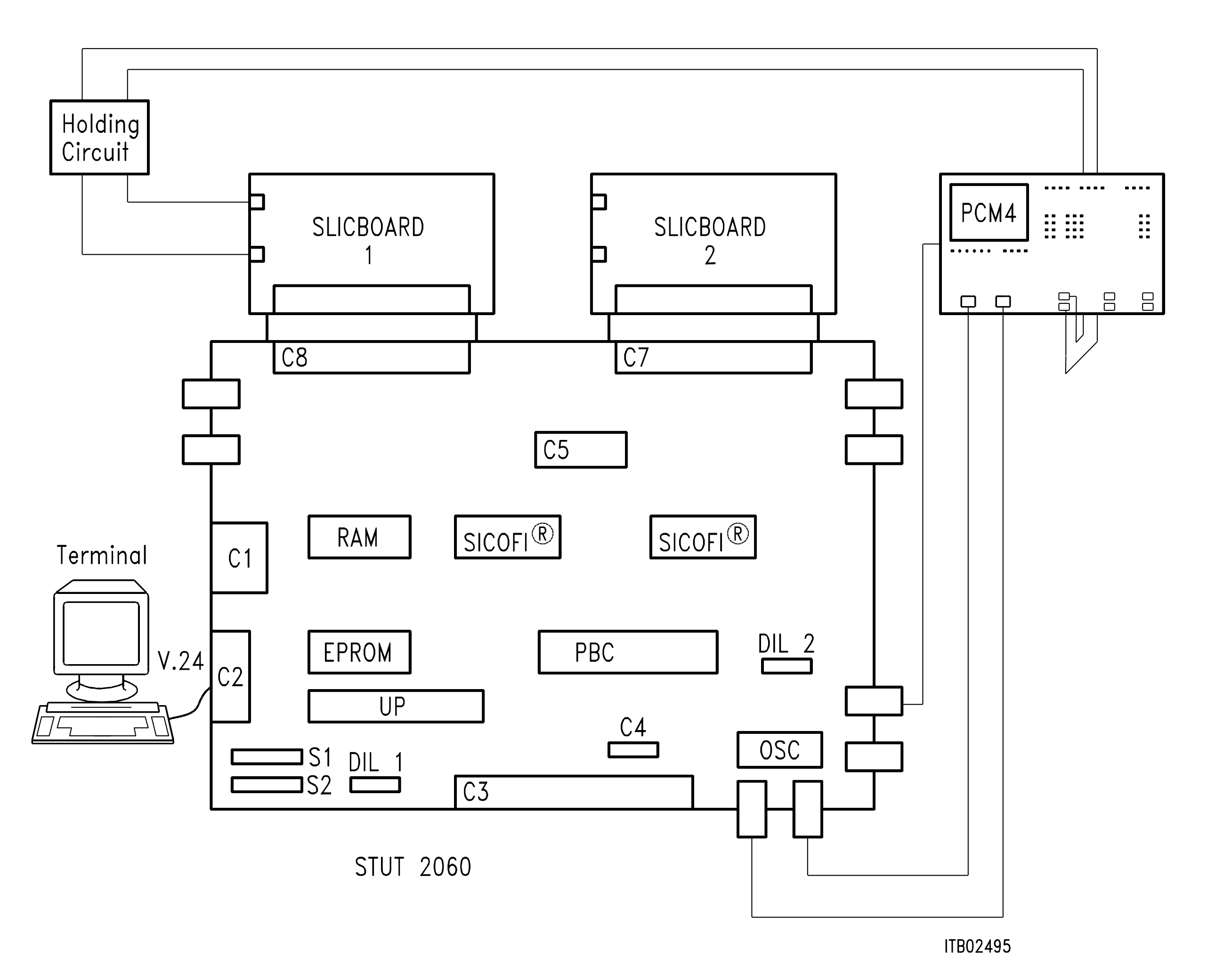


Diagram of the Measurement System

Appendix F

Measurements Results and Correlation

BYTE FILE

Following byte file was loaded into the SICOFI before performing the measurements:

SPICE.BYT

PSR = 36
CAM00 = 41
CAM20 = 40
CIW0 = 26,F4,80
CIW0 = 13,60,B2,3D,73,19,25,E3,2D
CIW0 = 23,70,C8,9F,7F,3B,37,04,A6
CIW0 = 2B,70,B8,AF,72,C3,9F,01,CF
CIW0 = 03,B2,EB,EC,31,22,BB,42,12
CIW0 = 0B,00,1C,3E,12,1B,5B,16,B3
CIW0 = 18,19,19,11,19
CIW0 = 30,51,12,00,BB
SIG0 = C0
CIW0 = 25,00,08,F4,78

MEASUREMENTS

LEVEL MEASUREMENTS:
(With a 1 kHz sine wave)

A-D:	– 3.28 dBm0	correct but would have to be corrected in a real application
D-A:	3.00 dBm0	correct

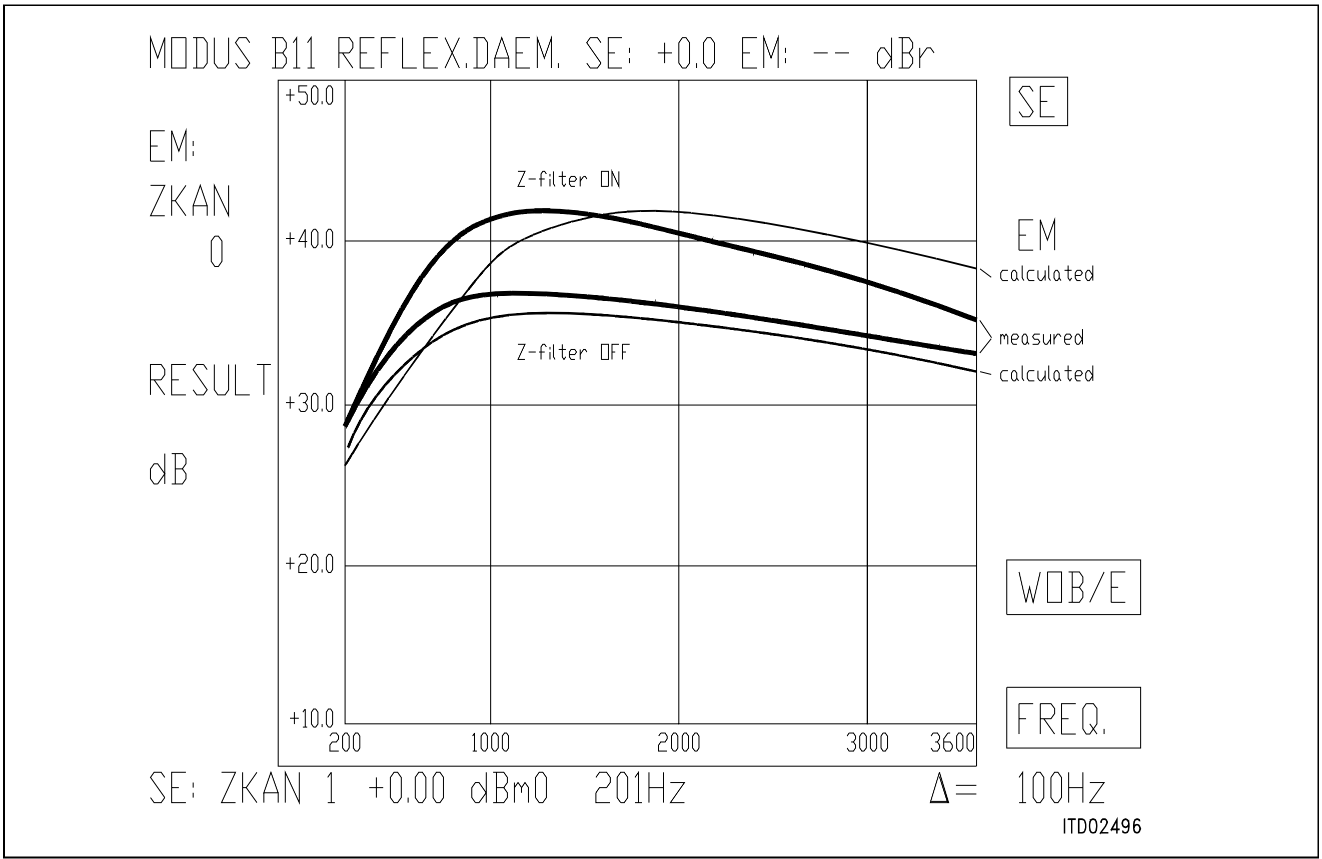
The other measurements results from the PCM4 (Wandel & Goltermann) are shown in the next pages.

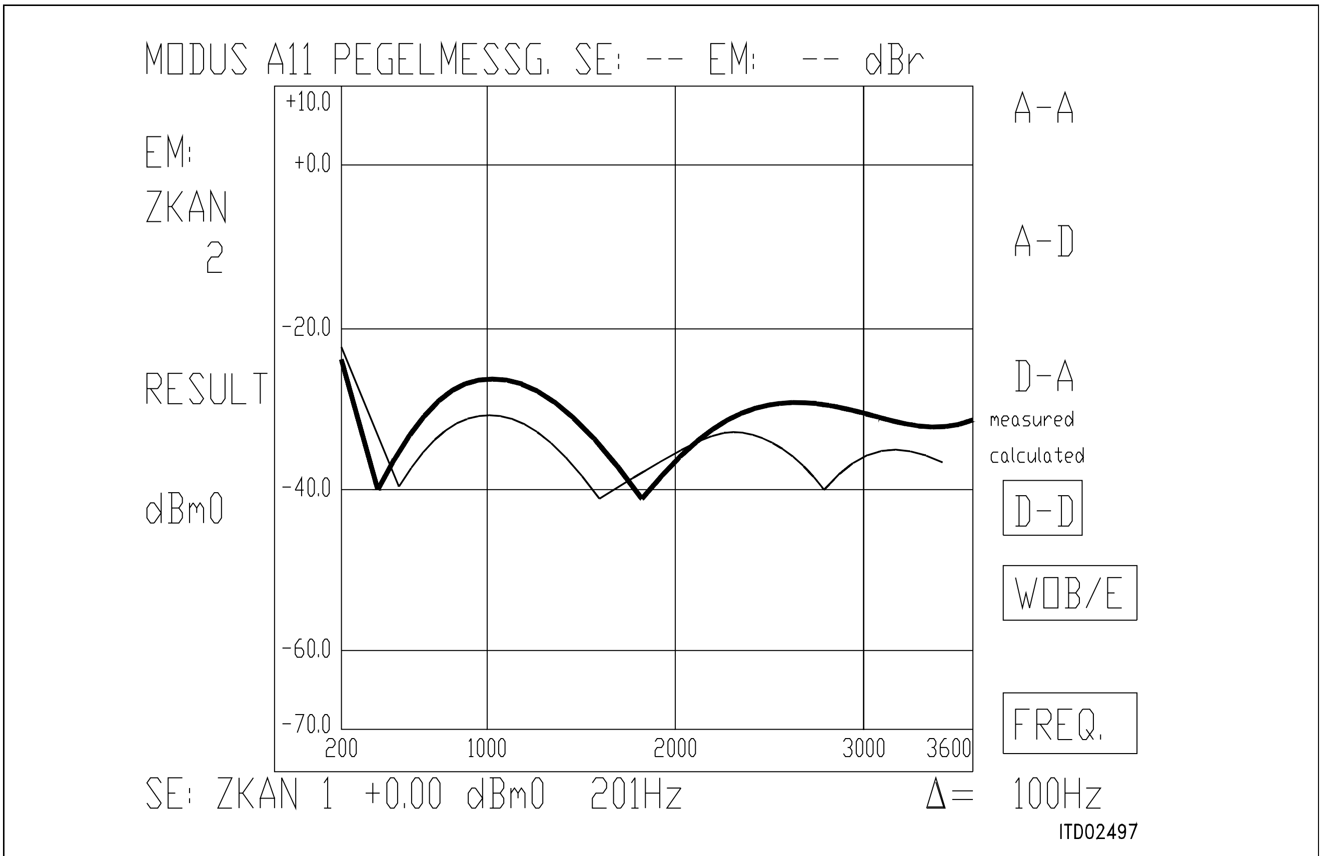
RETURN LOSS
(Reflex.Daem.)
correct

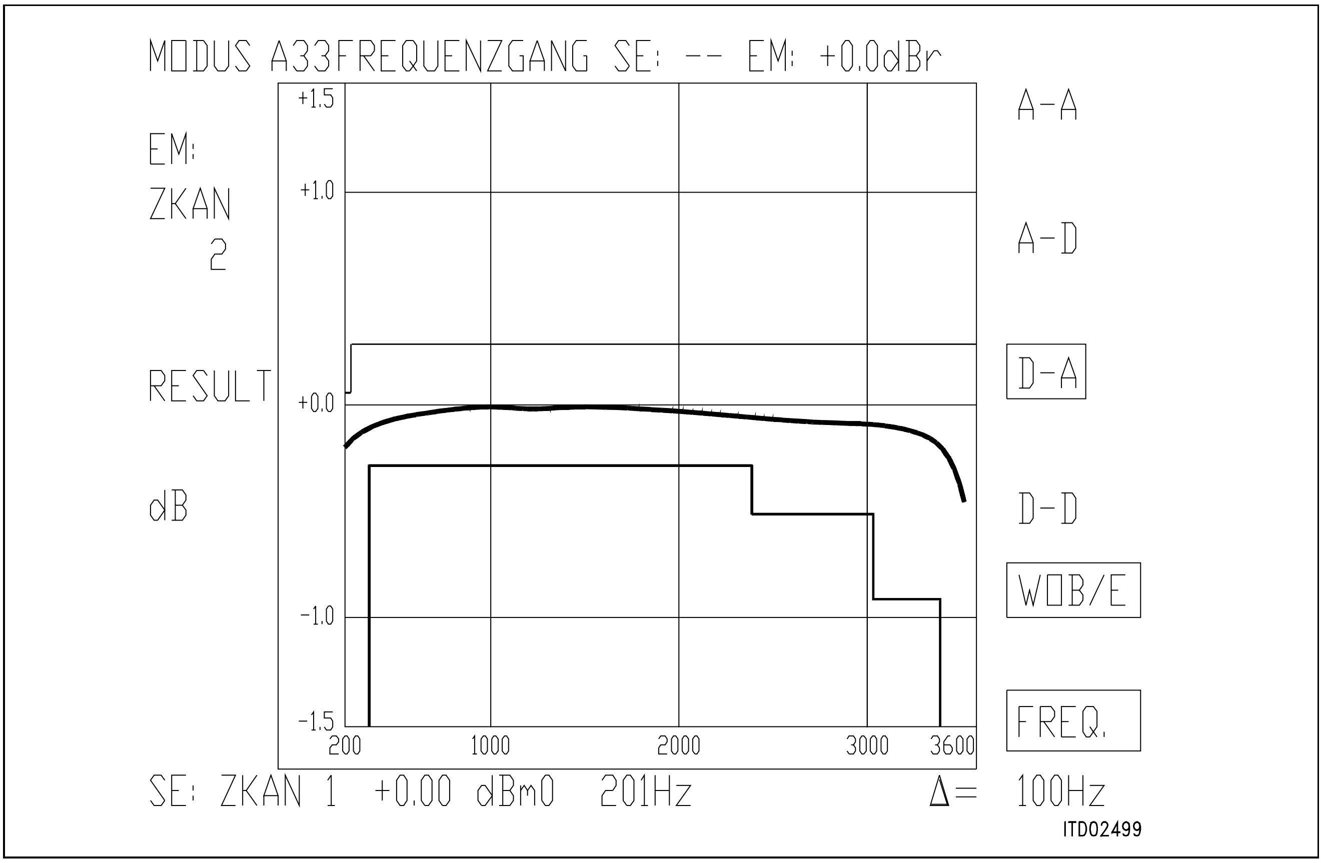
TRANS HYBRID LOSS
(Pegelmess. DD)
correct

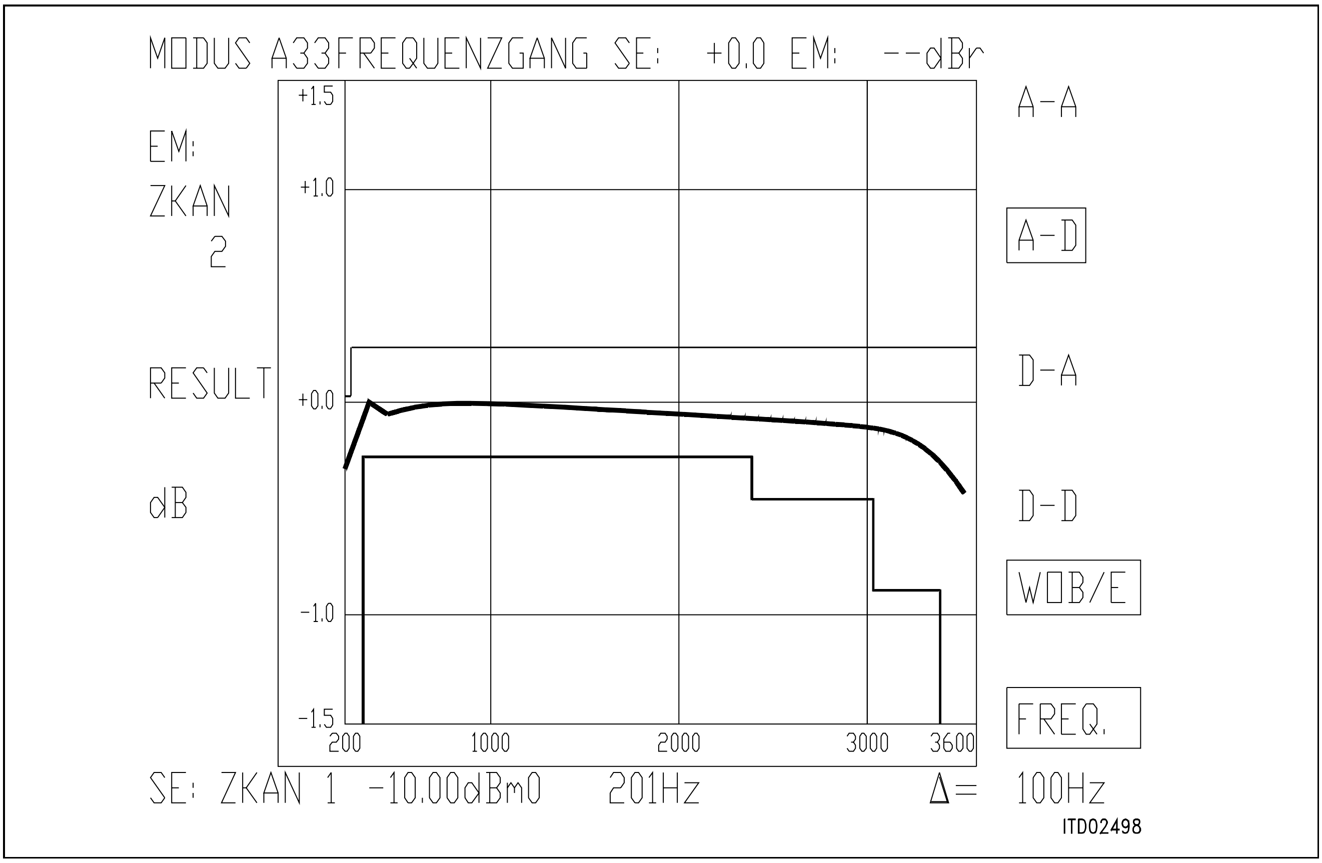
FREQUENCY RESPONSE
(Frequenzgang)
correct

CORRELATION
The correlation between measured results and calculated results can be seen on the plots of return loss and trans hybrid loss.


MODUS B11 REFLEX.DAEM. SE: +0.0 EM: -- dBr
EM:
ZKAN
0
RESULT
dB
+50.0
+40.0
+30.0
+20.0
+10.0
200
1000
2000
3000
3600
Z-filter ON
Z-filter OFF
SE
EM
calculated
measured
calculated
WOB/E
FREQ.
SE: ZKAN 1 +0.00 dBm0 201Hz
Δ= 100Hz
ITD02496


MODUS A11 PEGELMESSG. SE: -- EM: -- dBr
EM:
ZKAN
2
RESULT
dBm0
+10.0
+0.0
-20.0
-40.0
-60.0
-70.0
200
1000
2000
3000
3600
A-A
A-D
D-A
measured
calculated
D-D
WOB/E
FREQ.
SE: ZKAN 1 +0.00 dBm0 201Hz
Δ= 100Hz
ITD02497


MODUS A33FREQUENZGANG SE: -- EM: +0.0dBr
EM:
ZKAN
2
RESULT
dB
+1.5
+1.0
+0.0
-1.0
-1.5
200
1000
2000
3000
3600
A-A
A-D
D-A
D-D
WOB/E
FREQ.
SE: ZKAN 1 +0.00 dBm0 201Hz
Δ= 100Hz
ITD02499


MODUS A33FREQUENZGANG SE: +0.0 EM: --dBr
EM:
ZKAN
2
RESULT
dB
+1.5
+1.0
+0.0
-1.0
-1.5
200
1000
2000
3000
3600
A-A
A-D
D-A
D-D
WOB/E
FREQ.
SE: ZKAN 1 -10.00dBm0 201Hz
Δ= 100Hz
ITD02498

Appendix G

The SICOFI® File 'USA.SPE'

```
FREF = 1014.0 LAW = A
VREF = 0.7750 RLX = -3.0 RLR = +3.0
ABIMP = ZI
ZLRP1 = 600.  ZLCP1 = 0.  ZLRP2 = 0.  ZLCP2 = 0.
ZLRS = 000.   ZLCS = 0.
ZIRP1 = 600.  ZICP1 = 0.  ZIRP2 = 0.  ZICP2 = 0.
ZIRS = 000.   ZICS = 0.
Z3RP1 = 600.  Z3CP1 = 0.  Z3RP2 = 0.  Z3CP2 = 0.
Z3RS = 000.   Z3CS = 0.
ZRRP1 = 600.  ZRCP1 = 0.  ZRRP2 = 0.  ZRCP2 = 0.
ZRRS = 000.   ZRCS = 0.

ZRE
FR    300   500   1k    3.4k
AT-   0     20    30    30
AT+   20    26    30    0

ZMIR
FR    4k    12k
AT-   30    3
AT+   30    3

DA,UPPER
FR    300   500   2.7k  3k    3.4k
AT-   100   .75   .25   .35   .75
AT+   .75   .25   .35   .75   100

DA,LOWER
FR    300   3.4k
AT-   0     -.25
AT+   -.25  0

DA,DELAY
FR    500   600   1k    2.6k  2.8k
GD-   10K   .420  .150  .085  .150
GD+   .420  .150  .085  .150  10K

AD,UPPER
FR    300   500   2.7k  3k    3.4k
AT-   100   .75   .25   .35   .75
AT+   .75   .25   .35   .75   100

AD,LOWER
FR    300   3.4k
AT-   0     -.25
AT+   -.25  0
```

```
AD,DELAY
FR    500   600   1k    2.6k  2.8k
GD-   10k   .420  .150  .085  .150
GD+   .420  .150  .085  .150  10k
DD
FR    300   500   2.5k 3.4k
AT-   0     27    27    23
AT+   23    27    27    0
```

Appendix H

The SICOFI® File 'SPICE.CTL'

```
SPEC = USA.SPE     SLIC = SLIC.SLI
BYTE = REF.BYT     CHNR = 0,A
VERSION = 4.2      REL = N
ON = ALL
OPT = Z+X+R+B      ZXRB = NNNN
ZAUTO = N          PZIN = 11  PSP = 3
FZP = 300.0   500.0   1000.0  1300.0  1500.0
      2000.0  2500.0  2900.0  3000.0  3200.0
      3400.0  7000.0  10000.  14000.
WFZ = 0.100   1.00    2.00    1.50    1.00
      3.00    1.00    1.00    1.00    3.00
      2.80    1.00    1.00    1.00
FR 300.00    3400.0
RDISP = Y    RREFQ = N
FX 300.00    3400.0
XDISP = Y    XREFQ = N
BAUTO = N    PB = 10   GWFB = 0.500E-01   BDF = 1
FBP = 300.0   500.0   700.0   1000.0  1500.0
      2100.0  2300.0  2900.0  3200.0  3300.0
WFB = 4.000   2.000   1.000   5.000   1.000
      2.000   1.000   5.000   1.000   1.000
APRE = 0.0   DPRE = 0.0   APOF = 0.0    DPOF = 0.0
AGR = 00     AGX = 00     TM3 = 000
```

Appendix I 1

The Result File 'SPICE.RES'

```
Input_file_name: SPICE.CTL       Date: 30.06.89  18:24
SPEC = USA.SPE                 SLIC = SLIC.SLI
BYTE = REF.BYT                 CHNR = 0,A
PLQ = N
ON = ALL           VERSION = 4.2         SHORT = N
OPT = Z+X+R+B      ZXRB = NNNN           REL = Y
ZAUTO = Y          ZREP = N    ZSIGN = 1
FZ =    300.00     3400.0      ZLIM = 2.00
                   PZIN = 11   PSP = 3
FZP =   300.00     500.00      1000.0      1300.0      1500.0
        2000.0     2500.0      2900.0      3000.0      3200.0
        3400.0     7000.0      10000.      14000.
WFZ =   .100       1.00        2.00        1.50        1.00
        3.00       1.00        1.00        1.00        3.00
        2.80       1.00        1.00        1.00
FR =    300.00     3400.0
RDISP = Y          RREFQ = N   RREF = .51659E-01
FX =    300.00     3400.0
XDISP = Y          XREFQ = N   XREF = -.17369
BAUTO = Y          BREP = N    BSIGN = 1
FB =    300.00     3400.0      BLIM = 2.00      BDF = 1
                   PB = 10     GWFB = .500E-01
FBP =   300.00     500.00      700.00      1000.0      1500.0
        2100.0     2300.0      2900.0      3200.0      3300.0
WFB =   4.0000     2.0000      1.0000      5.0000      1.0000
        2.0000     1.0000      5.0000      1.0000      1.0000
APRE = .00      DPRE = .00      APOF = .00      DPOF = .00
AGX = 00        AGR = 00        TM3 = 000
XZQ =  -.15014650E-01   .40039060E-01   .19531250E-02
       -.35644530E-01   .19042970E-01
XRQ =   .99267580E+00  -.19531250E-02   .87280270E-02
       -.53710940E-02   .97656250E-03
XXQ =   .10117190E+01   .88500980E-02   .67138670E-02
       -.39367680E-02   .48828130E-03
XBQ =   .85937500E-01  -.10546880E+00   .16406250E+00
       -.61035160E-01  -.10961910E+00
        .10546880E+00   .31982420E-01  -.17968750E+00
        .17187500E+00  -.93261720E-01
XGQ =   .52148440E+00   .18906250E+01
;
```

```
Bytes for Z-Filter (13):            60,B2,3D,73,19,25,E3,2D
Bytes for R-Filter (2B):            70,B8,AF,72,C3,9F,01,CF
Bytes for X-Filter (23):            70,C8,9F,7F,3B,37,04,A6
Bytes for Gain-factors (30):        51,12,00,BB
2nd part of bytes B-Filter (0B):    00,1C,3E,12,1B,5B,16,B3
1st part of bytes B-Filter (03):    B2,EB,EC,31,22,BB,42,12
Bytes for B-filter delay (18):      19,19,11,19

* PSPICE library containing SLIC:
* .lib slic2op.lib
* PSPICE model name of SLIC:
* xownslic     ring tip +5v -5v vin vout   slic2op

Run # 1

Z-FILTER calculation results

  Reference impedance for optimization:
ZIRP1 = 600.   ZICP1 = .000   ZIRP2 = 0.   ZICP2 = .000
ZIRS  =   0.   ZICS  = .000

  Calculated and quantized coefficients:

XZ  =  -.01499   .04049   .00226   -.03554   .01916
XZQ =  -.01501   .04004   .00195   -.03564   .01904
Bytes for Z-Filter (13):   60,B2,3D,73,19,25,E3,2D

RETURN LOSS

FREQ       loss                FREQ       loss
(Hz)       (dB)                (Hz)       (dB)
 100.      19.065              2000.      41.828
 200.      26.269              2100.      41.702
 300.      29.910              2200.      41.502
 400.      32.327              2300.      41.332
 500.      34.117              2400.      41.168
 600.      35.549              2500.      41.007
 700.      36.694              2600.      40.851
 800.      37.657              2700.      40.711
 900.      38.519              2800.      40.586
1000.      39.272              2900.      40.470
1100.      39.931              3000.      40.349
1200.      40.452              3100.      40.215
```

Appendix I 2

The Result File 'SPICE.RES'

```
1300.      40.845                 3200.      40.057
1400.      41.244                 3300.      39.855
1500.      41.552                 3400.      39.627
1600.      41.770                 3500.      39.365
1700.      41.898                 3600.      38.957
1800.      41.942                 3700.      38.460
1900.      41.911                 3800.      37.871

Min. Z-loop reserve:          23.686 dB at frequency:  8500.0 Hz
Min. Z-loop mirror reserve:  28.394 dB at frequency:  9000.0 Hz

Run # 1

X-FILTER calculation results

  Reference impedance for optimization:
ZIRP1 = 600.   ZICP1 = .000   ZIRP2 = 0.   ZICP2 = .000
ZIRS  =   0.   ZICS  = .000

  Calculated and quantized coefficients:

XX  = 1.01201    .00886    .00670    -.00391    .00064
XXQ = 1.01172    .00885    .00671    -.00394    .00049
Bytes for X-Filter (23):   70,C8,9F,7F,3B,37,04,A6

X-filter attenuation function (in dB), (always absolute values)

FREQ        loss     GD                  FREQ        loss      GD
(Hz)        (dB)     (msec)              (Hz)        (dB)      (msec)
 100.       -.204     .002               2000.       -.048     -.001
 200.       -.204     .002               2100.       -.035     -.002
 300.       -.203     .002               2200.       -.023     -.002
 400.       -.201     .002               2300.       -.013     -.003
 500.       -.199     .002               2400.       -.005     -.003
 600.       -.196     .002               2500.        .000     -.003
 700.       -.192     .002               2600.        .002     -.003
 800.       -.187     .002               2700.        .001     -.003
 900.       -.182     .002               2800.       -.003     -.003
1000.       -.175     .002               2900.       -.010     -.002
1100.       -.167     .001               3000.       -.019     -.002
1200.       -.157     .001               3100.       -.031     -.002
1300.       -.147     .001               3200.       -.044     -.001
1400.       -.135     .001               3300.       -.057     -.000
1500.       -.122     .001               3400.       -.071      .000
1600.       -.108     .000               3500.       -.085      .001
1700.       -.093    -.000               3600.       -.097      .001
1800.       -.078    -.001               3700.       -.107      .002
1900.       -.063    -.001               3800.       -.114      .002
```

```
GX results:
All attenuation values (in dB) refer to FREF =   1014. Hz

RLX       SLIC+Z    AGX     VREF/VSIC  XREF       TM3     GX
-3.00 -   -3.65 -   .00 -    6.17 -    -.17 -     .00 =   -5.53 ideal
-3.00 =   -3.65 +   .00 +    6.17 +    -.17 +     .00 +   -5.53 quant

Second byte for Gain:     ,00,BB
Calculation of transmit transfer function (AD)
All attenuation values (in dB) refer to FREF =   1014.0 Hz

TGREF CA =  .052 ms     TGREF CB =   .065 ms
```

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
100.	15.930	3.431	2000.	.038	.209
200.	.445	2.226	2100.	.045	.214
300.	.036	.871	2200.	.048	.219
400.	.043	.527	2300.	.058	.226
500.	.037	.387	2400.	.062	.234
600.	.024	.315	2500.	.065	.243
700.	.014	.274	2600.	.067	.253
800.	.007	.248	2700.	.069	.266
900.	.001	.230	2800.	.073	.281
1000.	-.000	.219	2900.	.079	.299
1100.	-.001	.211	3000.	.088	.321
1200.	-.001	.206	3100.	.104	.348
1300.	-.000	.202	3200.	.134	.382
1400.	.003	.200	3300.	.188	.425
1500.	.007	.200	3400.	.280	.483
1600.	.012	.200	3500.	.435	.563
1700.	.018	.201	3600.	.725	.683
1800.	.025	.203	3700.	1.324	.878
1900.	.031	.206	3800.	2.789	.000

Run # 1

Appendix I 3

The Result File 'SPICE.RES'

```
R-FILTER calculation results
  Reference impedance for optimization:
ZIRP1 = 600.    ZICP1 = .000    ZIRP2 = 0.    ZICP2 = .000
ZIRS  =   0.    ZICS  = .000
  Calculated and quantized coefficients:
XR  = .99291      -.00166   .00870    -.00524    .00138
XRQ = .99268      -.00195   .00873    -.00537    .00098
Bytes for R-Filter (2B):   70,B8,AF,72,C3,9F,01,CF
R-filter attenuation function (in dB), (always absolute values)
FREQ        loss     GD                 FREQ        loss      GD
(Hz)        (dB)     (msec)             (Hz)        (dB)      (msec)
 100.       .043      .000              2000.        .132     -.002
 200.       .043      .000              2100.        .141     -.002
 300.       .043      .000              2200.        .149     -.003
 400.       .043      .001              2300.        .154     -.003
 500.       .044      .001              2400.        .156     -.003
 600.       .044      .001              2500.        .155     -.003
 700.       .045      .001              2600.        .150     -.003
 800.       .046      .001              2700.        .141     -.003
 900.       .048      .001              2800.        .129     -.003
1000.       .051      .001              2900.        .112     -.002
1100.       .055      .001              3000.        .093     -.002
1200.       .060      .001              3100.        .071     -.001
1300.       .066      .001              3200.        .047      .000
1400.       .073      .000              3300.        .022      .001
1500.       .081      .000              3400.       -.002      .002
1600.       .090      .000              3500.       -.024      .003
1700.       .100     -.000              3600.       -.044      .003
1800.       .111     -.001              3700.       -.061      .004
1900.       .122     -.001              3800.       -.074      .004
GR results:
All attenuation values (in dB) refer to FREF = 1014. Hz
-RLR      SLIC+Z    AGR     VSIC/VREF   RREF      GR
3.00 -    3.46 -    .00 -    -6.17 -   .05 =     5.66 ideal
3.00 =    3.46 +    .00 +    -6.17 +   .05 +     5.66 quant
First byte for Gain (30):    51,12
Calculation of receive transfer function (DA)
All attenuation values (in dB) refer to FREF =    1014.0 Hz
```

TGREF CA = .241 ms TGREF CB = .224 ms

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
100.	1.564	.947	2000.	.038	.032
200.	.102	.146	2100.	.045	.037
300.	.047	.045	2200.	.049	.044
400.	.027	.018	2300.	.058	.051
500.	.018	.008	2400.	.063	.060
600.	.014	.003	2500.	.066	.070
700.	.008	.001	2600.	.068	.081
800.	.004	.000	2700.	.070	.095
900.	.002	.000	2800.	.072	.110
1000.	.000	.001	2900.	.076	.129
1100.	-.001	.002	3000.	.083	.152
1200.	-.002	.004	3100.	.100	.179
1300.	-.003	.006	3200.	.131	.213
1400.	-.001	.009	3300.	.183	.257
1500.	.003	.012	3400.	.272	.315
1600.	.008	.015	3500.	.430	.396
1700.	.017	.018	3600.	.726	.517
1800.	.023	.022	3700.	1.329	.712
1900.	.030	.027	3800.	2.799	1.049

Run # 1

B-FILTER calculation results

Reference impedance for optimization:

```
ZLRP1 = 600.    ZLCP1 = .000    ZLRP2 = 0.    ZLCP2 = .000
ZLRS  =   0.    ZLCS  = .000
```

Calculated and quantized coefficients:

```
XB  =   .08614    -.10297    .16350   -.06106    -.10973
        .10419     .03201   -.17924    .17427    -.09337
XBQ =   .08594    -.10547    .16406   -.06104    -.10962
        .10547     .03198   -.17969    .17188    -.09326
```

Appendix I 4

The Result File ’SPICE.RES’

```
2nd part of bytes B-Filter (0B):   00,1C,3E,12,1B,5B,16,B3
1st part of bytes B-Filter (03):   B2,EB,EC,31,22,BB,42,12
```

TRANS HYBRID LOSS

FREQ (Hz)	loss (dB)	FREQ (Hz)	loss (dB)
100.	28.584	2000.	32.789
200.	21.368	2100.	32.011
300.	21.095	2200.	31.770
400.	33.727	2300.	32.031
500.	39.889	2400.	32.757
600.	36.865	2500.	34.043
700.	33.670	2600.	35.901
800.	31.997	2700.	38.039
900.	31.229	2800.	38.729
1000.	31.095	2900.	37.603
1100.	31.565	3000.	35.853
1200.	32.668	3100.	34.491
1300.	34.487	3200.	33.943
1400.	37.010	3300.	34.404
1500.	40.057	3400.	36.180
1600.	41.308	3500.	38.897
1700.	39.164	3600.	37.350
1800.	36.295	3700.	32.824
1900.	34.169	3800.	30.941

```
Additional B-filter delay (in seconds):   .625E-04
Bytes for B-filter delay (18):   19,19,11,19
```

Appendix J

The Batch File 'S.BAT'

```
SET pspicelib = C:\pspice;C:\slic;
               |            |
               |            Location of the customer SPICE libraries
               Location of the SPICE program and libraries

PSPICE1 %1.cir  %1.out
 |      |       |
 |      |       SPICE output file
 |      SPICE input file
SPICE program

SLIC    %1.out  %1.sli
 |      |       |
 |      |       Converting program output = SLIC input file for
 |      |       SICOFI program
 |      Converting program input
Converting program
```

Contents **Page**

Calculating SLIC Transfer Functions of the ERICSSON SLIC PBL 3736 Using K-Parameters and Spice

Preface

A solution to the problem of modeling SLICs and calculating SICOFI coefficients for SLICs is submitted. This is realized by combining an arbitrary **SPICE** program and the **Conversion Program** 'KCONVERT.EXE'. The Conversion Program links the SPICE software to the SICOFI Coefficients Program. In contrast to a former Application Note (2.90), **K-parameters** are used for describing the SLIC. The SLIC treated is the ERICSSON SLIC PBL 3736.

A detailed description of the Conversion Program is given, and its practical use is exemplified.

As an example a hardware setup is shown that meets the German as well as the US-American specifications just by programming the SICOFI correspondingly.

To read this application note with profits, the SICOFI Coefficients Program and generalities about the SLIC file format and the SPICE input files should be known.

1 Introduction

In a digital telephone system the Subscriber Line Interface makes up a very complex structure. In the past it has turned out practical for realization purposes to split one of its main functions, the hybrid function, into the actual two-to-four wire transition (Subscriber Line Interface Circuit: SLIC) and in some means of signal processing, hybrid balancing and impedance matching (Signal Processing Codec Filter: SICOFI). To make the various existing SLIC solutions operate optimally under different country specific conditions the SICOFI may be tuned to the particular SLIC by software ("coefficients" obtained by the SICOFI Coefficients Program). Therefore, however, the transfer functions of the respective SLIC must be known.

There are several ways to describe the behaviour of a SLIC. One method is to use K-parameters. In any case it is necessary to write a new program for each new type of SLIC. This process is not only time consuming but also prone to errors in the software model.

The simulation of analog circuits can also be done by using general programs like **SPICE** (we used a demo version* of the program PSPICE furnished by MICROSIM CORP.). Since the output file provided by SPICE is not suited as input file for the SICOFI Coefficients Program, a Conversion Program was written in FORTRAN. This conversion program converts the SPICE output file into an input file for the SICOFI Coefficients Program. It uses K-parameters in a form that is compatible with the STS 2060 SICOFI Coefficients Program. (C.f. also "Calculating SLIC Parameters Using SPICE").
In particular this Application Note shows how to match the **SICOFI PEB 2060** to the **ERICSSON SLIC PBL 3736**.

Terminology:
SLIC: Subscriber Line Interface Circuit.
SICOFI: Signal processing Codec Filter (PEB2060).
In the following we will call "SLIC" the hardware and software corresponding to the analog components in a subscriber line interface circuit **excluding** the SICOFI chip.
Please note that the Conversion Program, which calculates K-parameters from the SPICE output file, is called KCONVERT.EXE.

*) The demo version is a version of reduced features of PSPICE (c.f. section 4.3). It is available on request on diskette free of charge by Siemens HL IT AT, Balanstr. 73, D-8000 München 80.

2 SICOFI® Software Principle

The main functions of a Subscriber Line Interface Circuit (SLIC) are to provide the BORSHT functions (Battery feeding, Overvoltage protection, Ringing, Signaling, Hybrid function, Testing). In the case of a SLIC being used in combination with the SICOFI, the Hybrid function is split into the two-wire to four-wire conversion realized by the SLIC, and the impedance matching, hybrid balancing and gain adjustment provided by the internal filters of the SICOFI. The other functions (such as off-hook detection, metering, standby mode, ringing) may also affect the speech signal, but will not be considered in the SLIC example described below.
As has been told, the hardware can be split into two parts: The SLIC and its external circuitry on one side and the SICOFI on the other side (**see figure 1**).

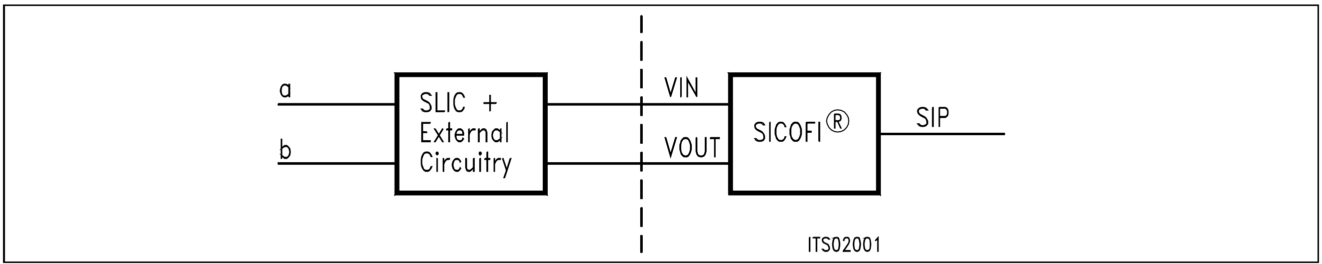


Figure 1
SLIC-SICOFI® Hardware

According to its functions, a SLIC and its periphery make up a rather complicated circuit structure (**see figure 13**). Analyzing the SLIC (e.g. simulating its transfer characteristics) is facilitated in using e.g. PSPICE. In doing so the thus gained SPICE output file is not compatible with the SICOFI program; it may, however, be adapted by using the Conversion Program 'KCONVERT.EXE' (**see figure 3**).

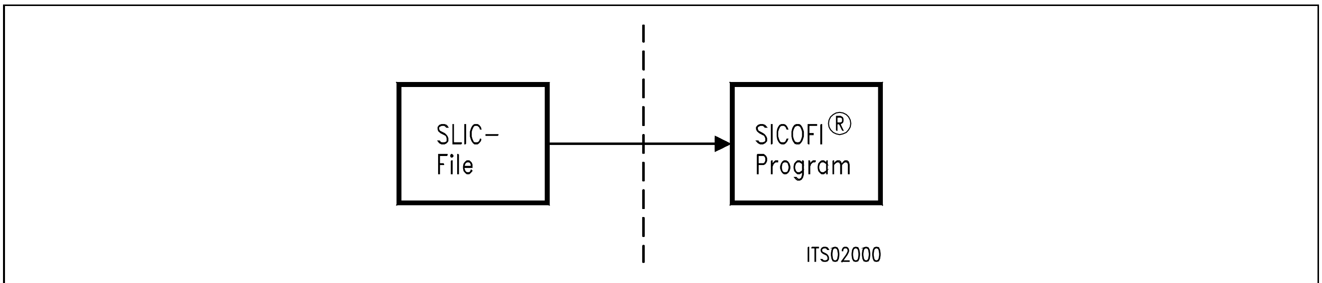


Figure 2
SLIC-SICOFI® Software

In a similar way, the software consists of two major sections: The SLIC description file (.SLI file) and the SICOFI program.

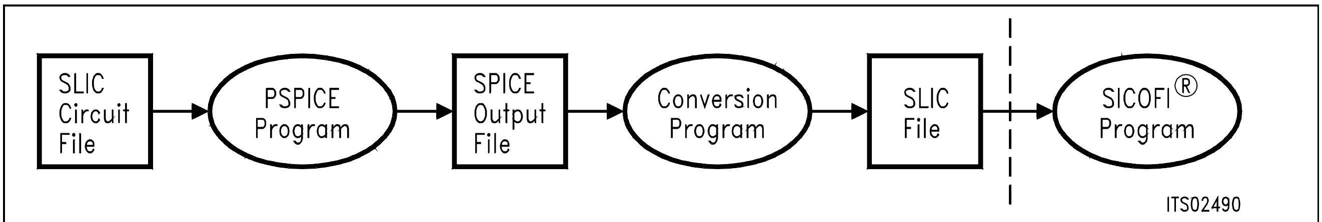


Figure 3
Software Structure

The detailed structure of the SPICE and SICOFI software is shown below (**figure 4**).

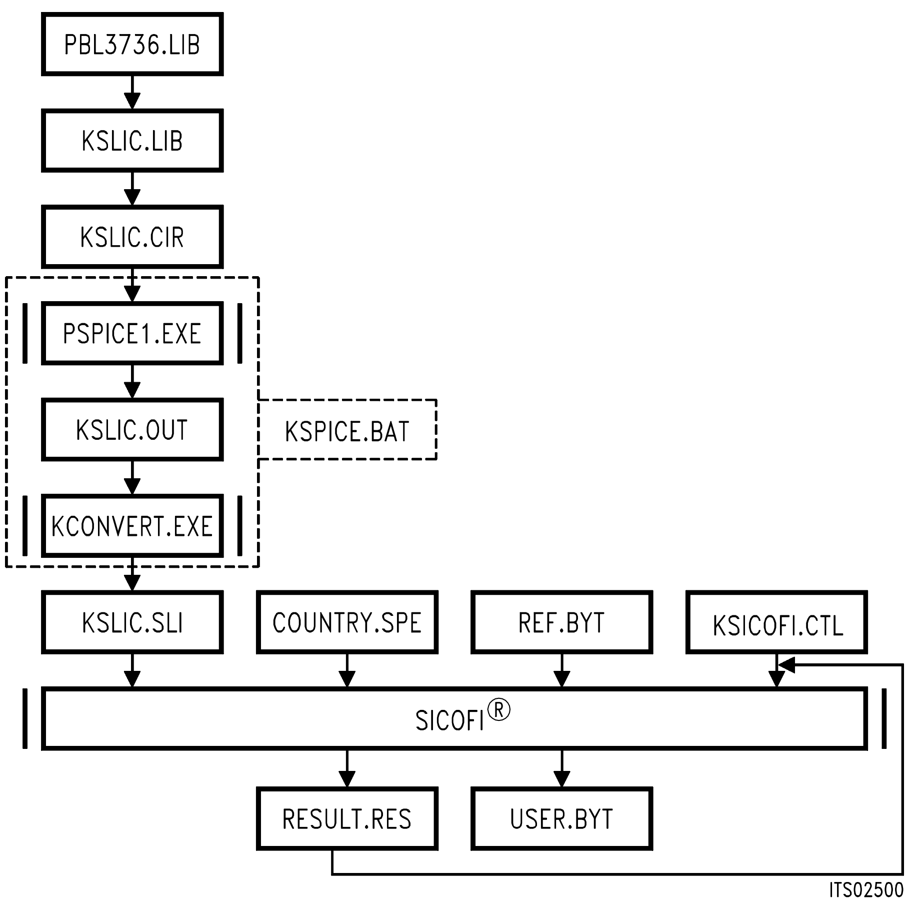


Figure 4
Detailed Software Structure

In the following the various SPICE library files are reviewed.

PBL3736.LIB
All the specific values concerning the SLIC and its external circuitry (physical data, filter dimensions, ...) are gathered in a SPICE input file PBL3736.LIB. If you want to simulate the SLIC with a different external circuitry, you have to make the corresponding changes in this file.

KSLIC.LIB
The file KSLIC.LIB provides the description of a particular SLIC circuit via the file PBL3736.LIB. The main advantage of this procedure is, that the file KSLIC.LIB acts like a black box containing the relevant SLIC: While the black box and its connections remain unchanged, the SLIC circuitry inside the box can easily be replaced by simply changing the names of the SLIC sub-circuit and it’s library PBL3736.LIB.

Example: If you have a model of SLIC No.1 in the file KSLICK1.LIB and a model of SLIC No.2 in the file KSLICK2.LIB, you could do simulations of the respective SLICs by exchanging the expression "KSLICK1.LIB" for the expression "KSLICK2.LIB" (and vice versa) in the file KSLIC.LIB.

KSLIC.CIR contains the test circuits that do the necessary ac-analyses. The result is a SPICE output file. This file has to be changed depending on the line impedance and the generator impedance in your application. For an example **see Appendix B**: The test circuit file 'KSLIC.CIR'.

The SPICE program analyzes the test circuits and calculates voltages and currents from which the K-parameters are deduced.

The program KCONVERT.EXE then converts the output of SPICE into the file KSLIC.SLI which is compatible with the SICOFI Coefficients Program and which contains the transmission characteristics of the SLIC in the form of the K-parameters.

For easy use, the SPICE program and the conversion programs are combined in a batch file KSPICE.BAT.
This batch file is run as follows:

KSPICE KSLIC <Enter> (Without the .CIR suffix)

KSLIC.SLI is a transfer file (output/input file) between the SLIC program and the SICOFI program to introduce the SLIC circuit data (K-parameters) into the SICOFI program.

Auxiliary Files:

COUNTRY.SPE is an input file of the SICOFI program describing the customer specification (CCITT etc. ...) and measurement configuration parameters (e.g. terminating impedance). The actual names used are BRD.SPE and USA.SPE for the German and US-American specifications respectively.

REF.BYT indicates the name of the reference byte file. This file is used as a frame to generate a new byte file. The newly calculated coefficients are written in this frame together with predefined commands. These commands are required for sending the SICOFI coefficients from the Peripheral Board Controller PBC (PEB 2051) to the SICOFI.

KSICOFI.CTL is the control file of the SICOFI program. It contains the data controlling the optimization and simulation processes.

The SICOFI program generates the SICOFI coefficients and simulates the theoretical transfer functions of the set SLIC + SICOFI.

RESULT.RES is the output file of the SICOFI program. It contains the coefficients for programming the SICOFI and a list of the calculated results corresponding to various measurements on the set SICOFI + SLIC (e.g. return loss, frequency response, echo return loss, etc....). The actual names used are K_BRD.RES and K_USA.RES containing the calculation results according to the German and US-American specifications respectively.

3 The Conversion Program KCONVERT.EXE

3.1 Features

- The Conversion Program is written in MICROSOFT FORTRAN and runs on an IBM PC AT or compatible.
- INPUT: The circuit description file 'KSLIC.OUT' which is generated by SPICE (or a file generated from measurement data) serves as an input file for the Conversion Program.
  The file 'KSLIC.OUT' contains the resulting voltages of the AC-analysis executed by the SPICE program. The AC-analysis is done in steps of 10 Hz, starting at a frequency of 10 Hz and ending at a frequency of 3990 Hz. In order to reduce the calculation time frequency steps larger than 10 Hz may be used. In this case the missing values are **interpolated**.
- OUTPUT: The program converts the SPICE output file into a SLIC file (with suffix .SLI). This *.SLI file describing the characteristics of a SLIC is used as an input file for the SICOFI Coefficients Program. The *.SLI file contains the parameter ZSLI (minimal attenuation of the SLIC at the four wire side) and the K-parameters of the SLIC for each frequency from 10 Hz up to 3990 Hz in steps of 10 Hz.
- BATCH MODE Facility: The program can be started by the batch file **KSPICE.BAT**. Just type:

  KSPICE KSLIC <enter> (without the suffix .CIR)

  or else it can be started from the keyboard by typing:

  PSPICE1 KSLIC.CIR KSLIC.OUT <enter>
  KCONVERT KSLIC.OUT KSLIC.SLI <enter>
- Flexibility: The program recognizes keywords in the SPICE output file. That is:
  – the order of the various AC-analyses does not make a difference
  – the ZSLI analysis can be missing in order to reduce the calculation time (ZSLI is then set to the default value of 0.5).
  – The program recognizes three kinds of circuits: two for the K-parameters and one for the ZSLI parameter calculation. Since the ZSLI value is calculated from different load impedances (e.g. 600 Ω, open/short circuit) there are **several circuits** available for the ac-analysis of ZSLI.

3.2 Batch File KSPICE.BAT

For a convenient use of the software, the sequence of steps necessary to run a complete analysis and to do the conversion of the SPICE output file into a SICOFI input file has been combined in a batch file. Thus by starting KSPICE.BAT for the circuit description file KSLIC.CIR, the resulting output file KSLIC.SLI can directly be used as an input for the SICOFI program. Circuit analysis and conversion of the intermediate results is performed by starting the batch file 'KSPICE.BAT' with the proper argument.

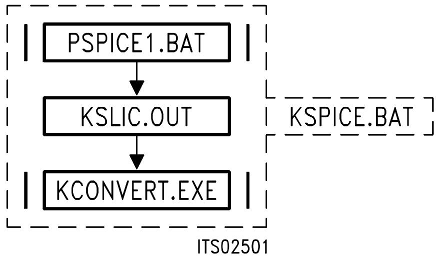


Figure 5
Contents of Program KSPICE.BAT

3.3 SLIC Description by K-Parameters

According to its functionality the SLIC operates as a three port. To describe its electrical properties five parameters are used in the SICOFI program: The four K-parameters and the ZSLI-value.
The ERICSSON SLIC PBL 3736 has a current output. Therefore we need to work with K-Parameters (not M-parameters!) which do not require to short-circuit the output of the SLIC.

3.3.1 K-Parameters

A SLIC with a generator V_g and a line impedance Z_g across the a/b lines can be considered as a three port. It can be described by the currents and voltages at these three ports: V_1, I_1, V_2, I_2, V_3, I_3 (**see figure 6**).

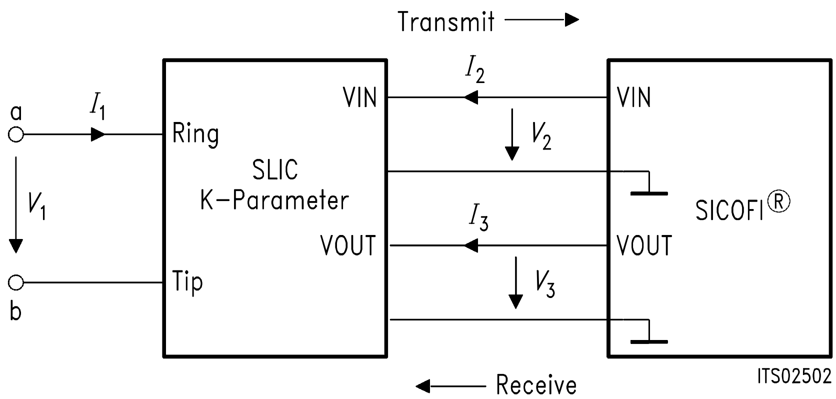


Figure 6
SLIC and its External Circuitry as a Three Port

Three equations are sufficient to describe the SLIC completely and any linear combination of the variables is possible.
Taking account of the symmetry at the a/b port let us take the following substitution:

(1) $a_1 = V_1 + Z_g \times I_1$
(2) $b_1 = V_1 - Z_g \times I_1$

Using these new variables the following equations can now be written:

(3) $b_1 = K11 \times a_1 + K12 \times V_3 + K13 \times I_2$
(4) $V_2 = K21 \times a_1 + K22 \times V_3 + K23 \times I_2$
(5) $I_3 = K31 \times a_1 + K32 \times V_3 + K33 \times I_2$

When the SLIC is connected to the SICOFI, we can assume that:

- $I_2 = 0$ because the input impedance of the SICOFI is very high.
- I_3 is not relevant in the SICOFI calculations because the SICOFI works as an ideal voltage generator.

According to these remarks, the equations system can be simplified as follows:

(6) $b_1 = K11 \times a_1 + K12 \times V_3$
(7) $V_2 = K21 \times a_1 + K22 \times V_3$

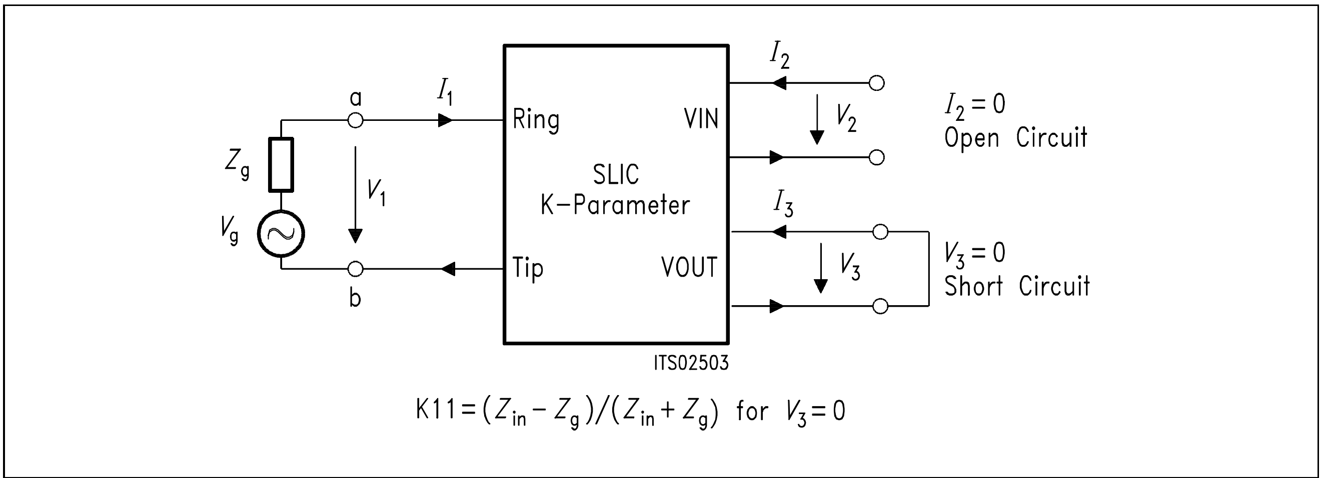


Figure 7
Definition of SLIC K11-Parameter

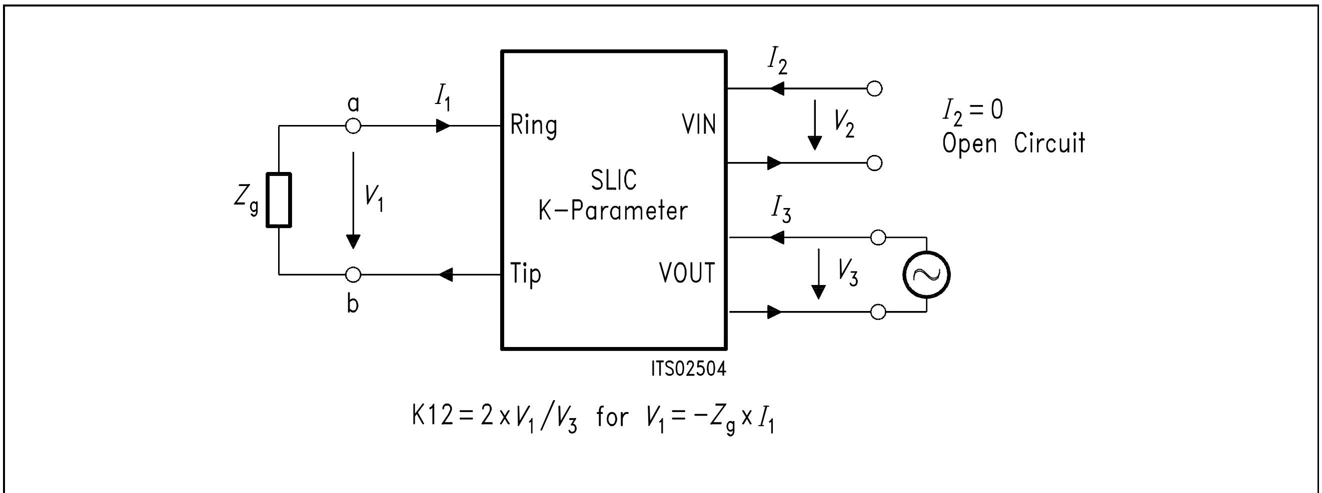


Figure 8
Definition of SLIC K12-Parameter

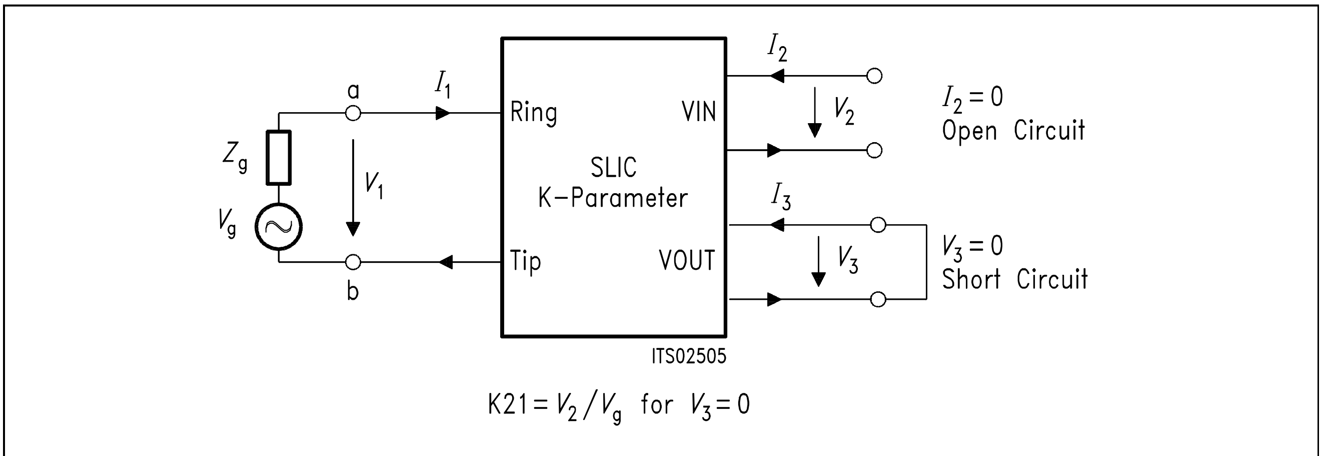


Figure 9
Definition of SLIC K21-Parameter

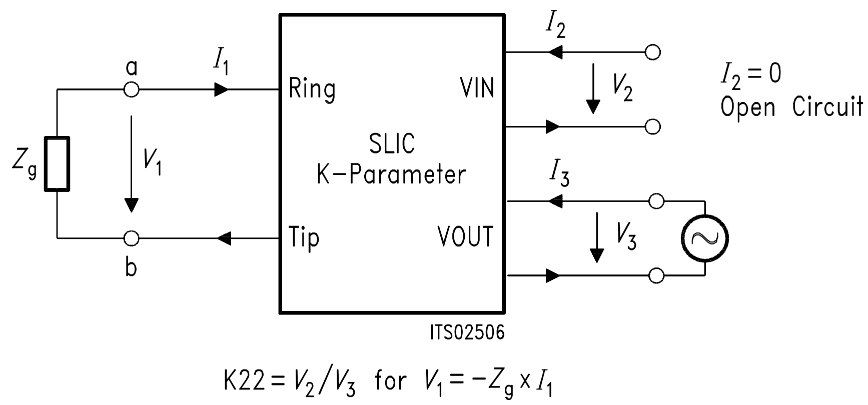


Figure 10
Definition of SLIC K22-Parameter

3.3.2 ZSLI

ZSLI is the **minimal attenuation** (resp. maximal gain) of the SLIC 4-wire side while the a/b lines are terminated by the terminal impedance Z_t (**see section 4.4**).

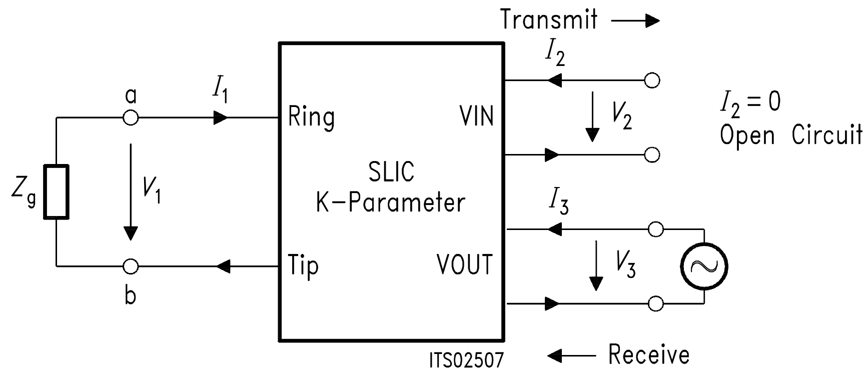


Figure 11
Definition of ZSLI

ZSLI is used by the SICOFI program during automatic calculation of Z-filter coefficients as a reference to check for possible oscillations in the SICOFI Z-filter + SLIC loop.

The value is in dB and is expressed as attenuation:

$$ZSLI = -20 \times \log (V_2/V_3)$$

→ Please verify that as V_2 is larger than V_3, ZSLI is a negative quantity.

In practice the attenuation of the loop "SLIC input to SLIC output" is **measured** over the whole frequency band 0 – 16 kHz for different terminating impedances Z_t. The **worst case** (the smallest attenuation resp. the greatest gain) then is taken for ZSLI.
The use of SPICE allows to obtain the ZSLI value without doing measurements.

Note: According to the Nyquist criteria, the attenuation of the closed loop "Z filter – SLIC" must be greater than 1 (gain < 0 dB) in the frequency band 0 – 16 kHz in order to avoid any oscillation.

4 Example

To exemplify the synthesis of SPICE and the SICOFI program, a circuitry consisting of the ERICSSON SLIC PBL 3736 and a SICOFI is analyzed. While the SLIC is a real circuit of fixed properties, the SICOFI is tuned by the SICOFI program as to meet particular specifications imposed by country specific requirements.

The results of the simulation and of the measurements of a sample circuit are compared.

4.1 Basic Set-up of SICOFI® and SLIC PBL 3736

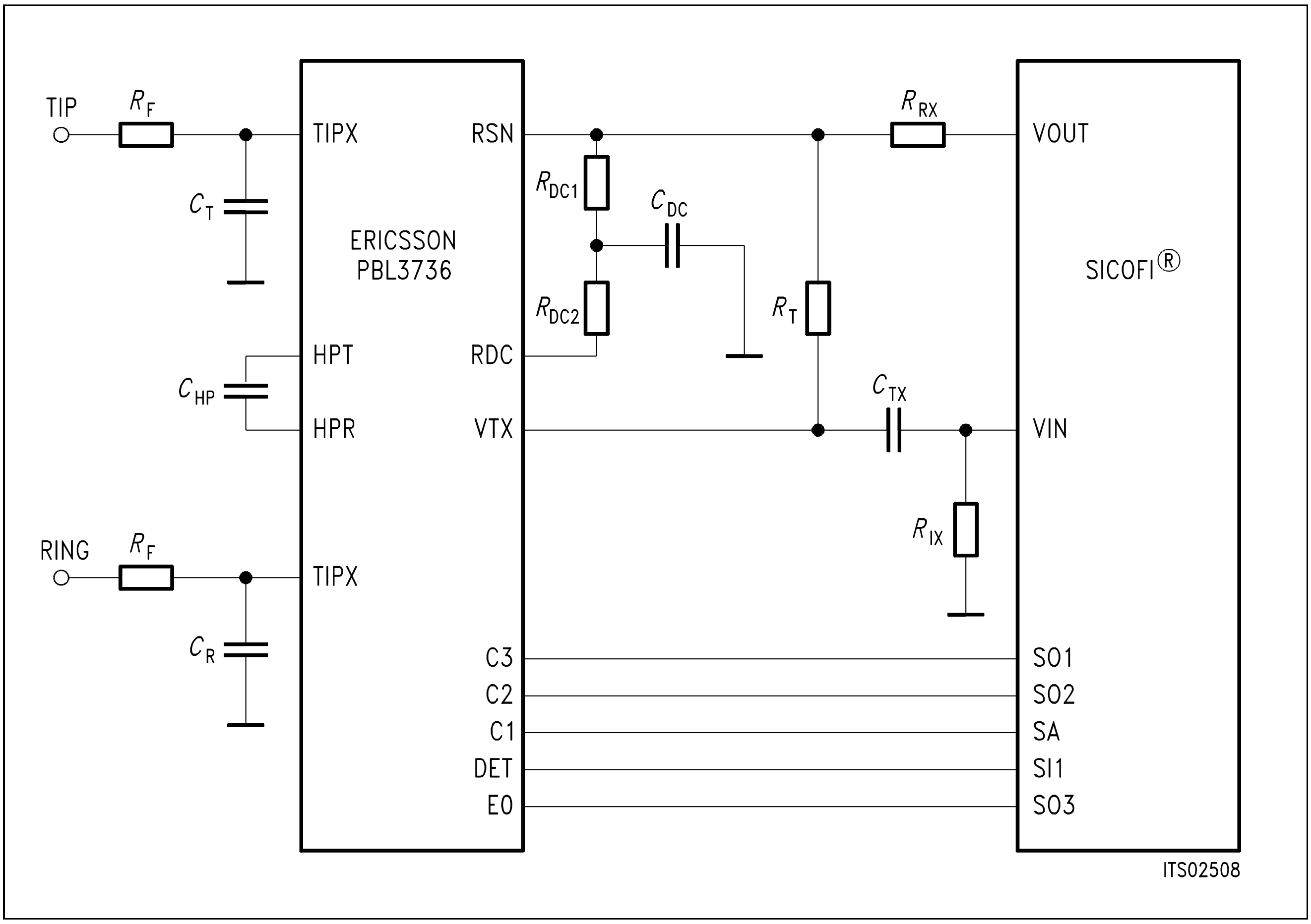


Figure 12
Basic Set-Up of SICOFI® and ERICSSON SLIC PBL 3736

The values of the components in **figure 12** are:

Capacitors:

C_R	=	2.2 nF
C_T	=	2.2 nF
C_{HP}	=	0.2 µF
C_{DC}	=	0.15 µF
C_{TX}	=	1 µF

Resistors: (1/4 W, 10% unless specified otherwise)

R_F	=	20 Ω
R_T	=	560 kΩ 0.5%
R_{RX}	=	300 kΩ 0.5%
R_{DC1}	=	20 kΩ
R_{DC2}	=	20 kΩ
R_{IX}	=	22 kΩ

Note: No attention has been paid to the overvoltage protection, signaling and loop monitoring functions in this Application Note because they should not influence the transmission characteristics.
The B-filters of the SICOFI allow for the adjustment of the transhybrid balance. Therefore we do not need to utilize the resistor R_B (connected between VIN and VOUT) for the transhybrid function (**see data sheet of the ERICSSON SLIC PBL 3736**).

4.2 Model of the SLIC PBL 3736

The simplified model of the SLIC is shown inside the dashed line in **figure 13**. This SLIC model as well as the external circuitry that is connected to the SLIC is listed in the SPICE file 'PBL3736.LIB' (**see Appendix A**).

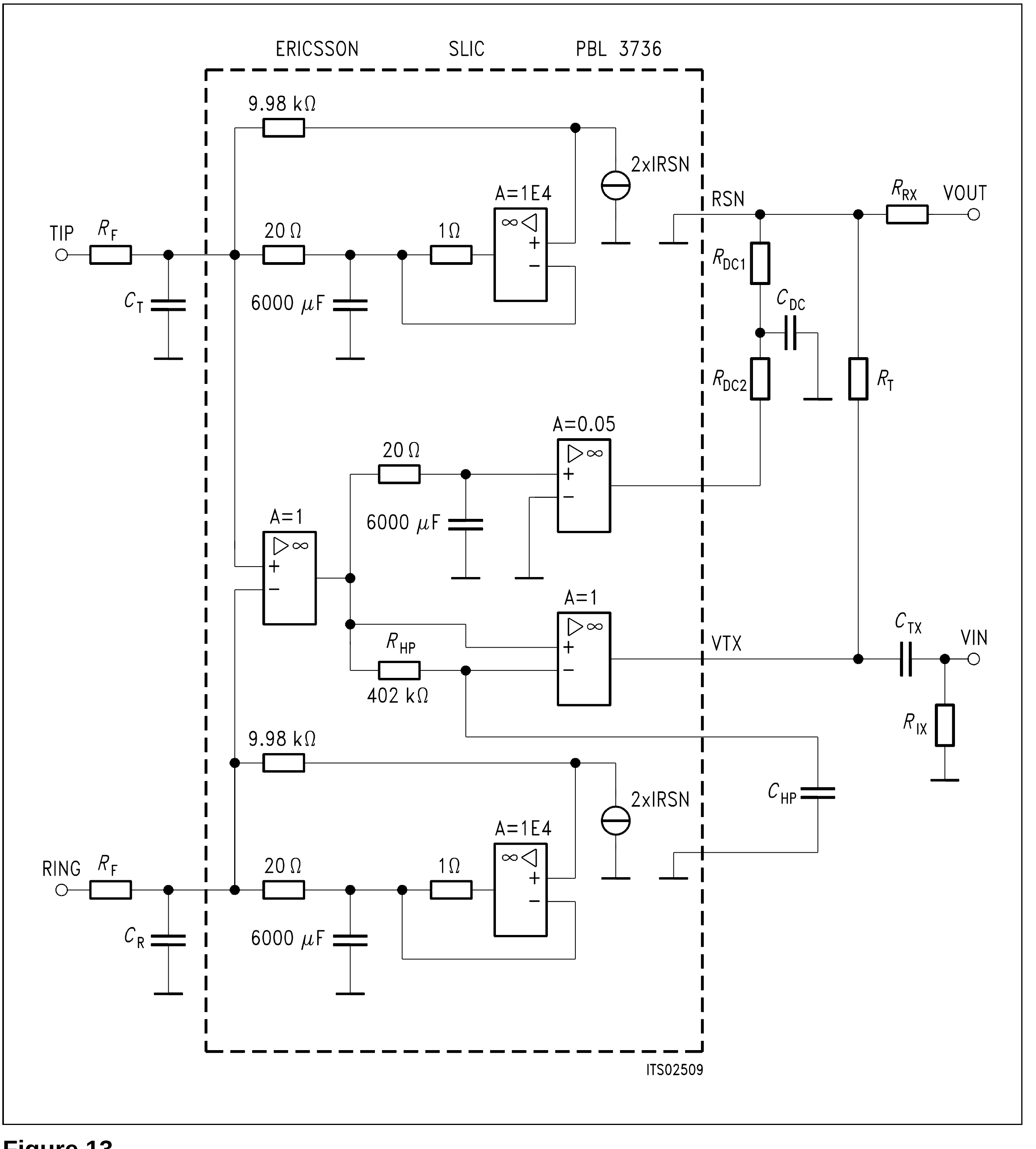


Figure 13
SLIC Model and External Circuitry

The values of the different components of **figure 13** are listed below:

R_F	=	20 Ω	fuse resistors
C_T	=	2.2 nF	
C_R	=	2.2 nF	
R_{DC1}	=	20 kΩ	DC path
R_{DC2}	=	20 kΩ	DC path
C_{DC}	=	0.15 µF	DC path
C_{HP}	=	0.2 µF	high pass filter in transmit direction
R_T	=	560 kΩ	matching impedance
R_{RX}	=	300 kΩ	gain impedance
C_{TX}	=	1 µF	high pass filter
R_{IX}	=	22 kΩ	high pass filter

4.3 How to Edit the Library File PBL3736.LIB

This chapter describes how to define a SLIC-circuit in a library file. The library file can be edited with any text editor, unless it creates embedded control characters. For this example we refer to the file PBL3736.LIB, which is listed in the appendix.

The **rules for the format of SPICE files** are:

– The first line is a title line, which is not part of the circuit but is used only for documentation purposes or comment.
– The last line is the .END statement.
– comment lines start with an "*" in the first column.
– continuation lines start with a "+" in the first column.

The **names of parts** in the circuit must begin with a letter. The following characters can be letters or numbers (example: 'RXY123' is the name of a resistor).

The **nodes** to which the parts are attached to can be names made up of letters and/or numbers (example: VOUT, VIN, 1, 2, 3).
Nodes "0" stand for ground.

Component values may be written in floating-point notation (example: 1.2E–6, 1.8E6) or with a scale suffix (example: 1.2 µ, 1.8 MEG).
Valid scale suffixes are:

F	=	10^{-15}	femto
P	=	10^{-12}	pico
N	=	10^{-9}	nano
U	=	10^{-6}	micro
M	=	10^{-3}	milli
K	=	10^{+3}	kilo
MEG	=	10^{+6}	mega
G	=	10^{+9}	giga
T	=	10^{+12}	tera

The SLIC circuit described in the file PBL3736.LIB is written in the subcircuit ERICSSONSLIC:

.SUBCKT ericssonslic ring tip + 12 V – 12 V vin vout

The number of nodes (here: ring, tip, + 12 V, – 12 V, vin, vout) in the calling program must be the same as in the subcircuit itself.

The .SUBCKT statement is followed by a listing of the components in the SLIC circuit. Itemized below are the components that can be used with the demo version of PSPICE. Elements like transistors, diodes etc. are not available. To simulate more elaborate SLIC circuits you will need the full-featured version of PSPICE.

Notation:

(name)	Comment
[item]	Optional item
[item]*	Zero or several items
<item>	Required item
<item>*	One or several items

The most commonly used parts are:

Capacitor
general form:

```
C<name> <(+)node> <(–)node> <value>
```

example:

```
* Capacitor (first letter "C") situated between
* |           node tipx
* |           |      and ground
* |           |      |      value of the capacitor (in Farad)
* |           |      |      |
CT            tipx   0      2.2 nF
```

Voltage-Controlled Voltage Source (Ideal Operational Amplifier)
general form:

```
E<name> <(+)node> <(–)node> <(+ controlling) node> + <(– controlling)  node> <gain>
```

example:

```
* E(name)     (+)node     (–)node     
* |           |           |           (+controlling) node
* |           |           |           |                    (-controlling) node
* |           |           |           |                    |         gain
* |           |           |           |                    |         |
E1            2           0           3                    1         1.0E4
```

Current-Controlled Current Source
general form:

```
PF<name> <(+)node> <(–)node> <(controlling V device) name> <gain>
```

example:

```
* F(name)     (+)node     (–)node     (controlling
* |           |           |           V device)name
* |           |           |           |
* |           |           |           |
* |           |           |           |                    gain
* |           |           |           |                    |
* |           |           |           |                    |
F1            3           0           VRSN                 2
```

Inductor Coupling
general form:

```
K<name> L<(inductor) name> <L<(inductor)name>*
+ <(coupling) value>
```

example:

```
* inductive coupling between
*             inductance L2 and
*             |      inductance L3 with the
*             |      |      coupling factor K23
*             |      |      |
K23           L2     L3     0.997
```

the coupling factor must be between 0 and 1.

Inductor

general form:

```
L<name> <(+)node> <(–)node> [<(model) name>] <value>
```

example:

```
* Inductor (first letter "L") situated between
* |            node 1 and
* |            |      node 2
* |            |      |      value of the inductance (in Henry)
* |            |      |      |
L2             1      2      1.23H
```

Resistor

general form:

```
R<name> <(+)node> <(–)node> [(model) name] <value>
```

example:

```
* Resistor (first letter "R") situated between
* |            node tip and
* |            |      node tipx
* |            |      |      value of the resistor (in Ohm)
* |            |      |      |
RF1            tip    tipx   20
```

Independent Voltage Source

general form:

```
V<name> <(+)node> <(–)node> + [[DC] <value>][AC <(magnitude) value> [(phase) value]]
```

example:

```
* V(name)      (+)node      (–)node      (dc)value
* |            |            |            |
* |            |            |            |
VRSN           .RSN         0            DC2
```

4.4 The SPICE Input File 'KSLIC.CIR'

The circuit description file KSLIC.CIR is the input file from which SPICE generates all the output variables necessary for the Conversion Program.

According to chapter 3.3 two circuits are simulated, one circuit for the parameters K11 and K21 (**figures 7 and 9**), and one circuit for calculating the parameters K12 and K22 (**figures 8 and 10**).

The K11 and K21 parameters are calculated from the frequency response of the complex variables

V_1, the voltage between "ring" and "tip" (port 1 of the SLIC),
V_2, the voltage at VIN (port 2 of the SLIC), and
$V_{(1a,ring)}$, voltage across line/generator AC impedance (across Z_g).

The K12 and K22 parameters are calculated from the frequency response of the complex variables

V_1, the voltage between "ring" and "tip" (port 1 of the SLIC),
V_2, the voltage at VIN (port 2 of the SLIC),
V_3, the voltage at VOUT (port 3 of the SLIC).

The SPICE listing of these two circuits can be found in the first part of the file '**KSLIC.CIR**' (Appendix B).
In order to find the minimal attenuation of the SLIC at the four wire side (ZSLI), three circuits are simulated with the following terminating conditions at port 1:

one with a short circuit between "ring" and "tip",
one with a 600 Ω or a complex load between "ring" and "tip",
and
one with an open circuit between "ring" and "tip".

This yields three values for

$$ZSLI = -20 \times \log(V_2/V_3)$$

The magnitudes of the voltages V_2 and V_3 at VIN and VOUT result from a SPICE AC-analysis. The smallest attenuation value out of these ZSLI's is then used for the calculations.

The SPICE listing of these three circuits are found in the second part of the file 'KSLIC.CIR' (Appendix B).

4.5 Format of the SPICE Output File

The output file of SPICE generated by the circuit description file 'KSLIC.CIR' consists of the AC-analyses for the K-parameters and the AC-analyses for the ZSLI values.

Each of these AC-analyses is arranged as follows (keywords which are recognized by the Conversion Program are printed in **bold** types):

a) A title line with one or two keywords to identify the circuit. The keywords can be one of the following:

- **K11** and **K21**
- **K12** and **K22**
- **ZSLI**

.

b) Name of the library with the SLIC
.lib <name of library with the SLIC>

c) description of test circuit
XSLIC ring tip + 5 V – 5V VIN VOUT <name of SLIC>

.

commands for starting analysis

.

.end

d) AC-analysis output of SPICE
AC ANALYSIS

.

one of these lines:

FREQ	**VR(VIN)**	**VI(VIN)**	**VR(ring,tip)**	**VI(ring,tip)**	*or*
FREQ	**VR(VIN)**	**VI(VIN)**	**VR(VOUT)**	**VI(VOUT)**	*or*
FREQ	**VR(1a,ring)**	**VI(1a,ring)**			*or*
FREQ	**VR(ring,tip)**	**VI(ring,tip)**			*or*
FREQ	**V(VOUT)**	**V(VIN)**	*depending on the part of the output*		

empty line
empty line
1.000E+01 1.000E+00 7.167E– 08 ....

.

all points of ac analysis

.

1.600E+04 1.000E+00 1.993E– 04 ....
line without scientific reals.

End of file or next part of SPICE output.

The first column of the AC-analysis shows the frequency value, the adjacent columns contain the corresponding real and imaginary parts of the variable for that particular frequency.

The Conversion Program will use this Spice output data to calculate the four K-parameters. The SPICE output contains only voltages. All K-parameters can easily be calculated from these voltages. As K11 originally is represented by impedances (**see figure 7**), the equivalence of the representation by voltages and impedances is shown below.

$$\text{K11} = \frac{V_{(\text{ring,tip})} - V_{(\text{1a,ring})}}{V_{(\text{ring,tip})} + V_{(\text{1a,ring})}} = \frac{\dfrac{V_1}{I_1} - \dfrac{V_{(\text{1a,ring})}}{I_1}}{\dfrac{V_1}{I_1} + \dfrac{V_{(\text{1a,ring})}}{I_1}} = \frac{Z_{\text{in}} - Z_{\text{g}}}{Z_{\text{in}} + Z_{\text{g}}}$$

4.6 How to Use the Conversion Program 'KCONVERT.EXE'

To calculate the parameters of a SLIC, procede as follows:

1. Set up a library file containing the SLIC data.
2. Prepare a library file with the description of the SLIC subcircuit for SPICE.
3. Put the name of this library file and of the subcircuit to the proper place in the 'KSLIC.LIB' file.
4. Execute the SPICE program with the 'KSLIC.CIR' file as argument.
5. Execute the Conversion Program 'KCONVERT.EXE' with the arguments 'KSLIC.OUT KSLIC.SLI'
6. Then run the SICOFI program. An example of a control file is given in 'KSICOFI.CTL'

Note: Steps 3 and 4 are put together in the batch file 'KSPICE.BAT'.
(Type: '**KSPICE KSLIC**' <enter> without extension).

Example:
Calculation of the SLIC 'PBL3736' in the library file 'PBL3736.LIB' (for more information on how to use this file, please refer to the manual of PSPICE [2]).
Words to be edited in the file 'KSLIC.LIB' are printed in **bold** types (**see figure 14**).

Figure 14
The File 'KSLIC.LIB' Before Editing. The spaces for xxxxxxxx.LIB and yyyyyyyy are to be filled with the correct library file name and the particular SLIC subcircuit name.

```
* file for accessing the proper SLIC with no changes in the
* KSLIC.CIR file
*
* change  "xxxxxxx.LIB" into the name of the library file
* with your particular SLIC subcircuit
.LIB xxxxxxx.LIB
* change the model name "yyyyyyyy" into the name of your
* particular subcircuit
.subckt SLIC   ring tip +5V -5V VIN VOUT
xownSLIC       ring tip +5V -5V VIN VOUT   yyyyyyy
.ENDS KSLIC
```

After editing, the file looks as follows (**see figure 15**):

Figure 15
The File 'KSLIC.LIB' After Editing. The bold typed words have been changed.

```
* file for accessing the proper SLIC with no changes in the *
KSLIC.CIR file
*
* change "KSLIC.LIB" into the name of the library file with
* your particular SLIC subcircuit
.LIB KSLIC.LIB
* change the model name "ERICSSONSLIC" to the name of your
* particular subcircuit
.subckt SLIC   ring tip +5V -5V VIN VOUT
xownSLIC       ring tip +5V -5V VIN VOUT     ERICSSONSLIC
.ENDS KSLIC
```

Now the batch file 'KSPICE.BAT' can be executed and unless errors are reported, the output file 'KSLIC.SLI' can be used in the SICOFI program.
For the use of the SICOFI program please refer to the Software Description of the STS 2060 SICOFI COEFFICIENTS PROGRAM [3]

4.7 Format of the SICOFI® Input File

The SICOFI input file is listed below (keywords are set in bold type):

```
       * PSPICE library used for calculating | comment
       * .lib KSLIC.lib                      | lines
       * PSPICE model used for calculating   | start
       * K-parameters                        | with "*"
       * xSLIC ring tip +5v -5v Vin 0 SLIC

ZSLI   .41905
K11-TABLE
       10.000000   2.978000E-03   -8.219000E-04
       20.000000   2.856892E-03   -7.672104E-04
     ..............  ..................  .......................
     3980.000000   1.671095E-03   -9.220666E-05
     3990.000000   1.671000E-03   -9.240000E-05
K12-TABLE
       10.000000   5.185000E-04    1.064000E-03
       20.000000   6.787197E-04    9.931213E-04
     ..............  ..................  .......................
     3980.000000   2.234000E-03   -1.258381E-04
     3990.000000   2.234000E-03   -1.262000E-04
K21-TABLE
       10.000000   1.864000E-01   -3.890000E-01
       20.000000   3.144297E-02   -3.902608E-01
     ..............  ..................  .......................
     3980.000000      -1.515000    9.331572E-02
     3990.000000      -1.515000    9.361000E-02
K22-TABLE
       10.000000   5.157000E-01   -2.201000E-01
       20.000000   3.803514E-01   -2.266998E-01
     ..............  ..................  .......................
     3980.000000      -1.515000    9.331572E-02
     3990.000000      -1.515000    9.361000E-02
```

The leading comment lines (starting with an "*") document which SLIC is being used.
The first column of the K-parameter tables indicates the frequency value, running from 10 Hz to 3990 Hz in steps of 10 Hz. The second column gives the values of the real parts and the third column the values of the imaginary parts of the K-parameters.
The three values listed in one line are separated by at least one space character. Each real number must contain a decimal point. (FORTRAN "REAL" format.)

4.8 Results

After simulating the SLIC, listed in the file PBL3736.LIB, the SICOFI Coefficients Program calculates the programming bytes. The result files of the SICOFI program are stored in ’K_USA.RES’ and ’K_BRD.RES’, the calculated programming bytes are stored in the files ’K_USA.BYT’ and ’K_BRD.BYT’.
With these bytes the SICOFI has been programmed and measurements have been taken with the Ericsson SLIC PBL3736 plugged into the STUT 2060 test board as shown in Appendix C. The measurements comprise the levels in transmit direction (AD) and in receive direction (DA), the attenuation distortion (AD and DA), the transhybrid loss (DD), and the 2-wire impedance return loss.
The plots of the measurements can be found in Appendix D.
The plot masks for the return loss correspond to the German and the US-American specifications, respectively. In our example these two different country specifications are met with just one hardware setup.

4.9 Comparison between Measurement Results and Simulation Results

In Appendix D simulation results of the return loss and the transhybrid loss are compared with the measurement results.
For the Z-filter switched off, the calculated curves for the return loss are in very good agreement with the measured curves. With the Z-filters switched on, there are differences between the simulated curves and the measured curves. The same is true for the transhybrid loss. When the B-filter is switched off, the measured transhybrid loss is close to the calculated curve. With the B-filter switched on, the measured result differs from the calculated result.

The differences between the respective curves may be due to the fact that a simplified transmission model of the SLIC was used.

Conclusion:

– Using the SPICE simulation program one can model a SLIC efficiently. In combination with the Conversion Program 'KCONVERT.EXE' the K-parameters are calculated.
  With the K-parameters as an input to the SICOFI Coefficients Program one can compute coefficients for the SICOFI.
– A single hardware setup can meet the specifications of different countries just by programming the SICOFI with the corresponding sets of coefficients.

5 Literature

[1] PSPICE
Microsim Corporation
20 Fairbanks, Irvine, California 92718

[2] Software Description STS 2060, SICOFI Coefficients Program
Version 3.x, January 1989
Siemens A.G.

Appendix A
Library File 'PBL3736.LIB'

```
ERICSSON Slic PBL3736
*
* Version 1.0 by M. Beck (based on simulations done by T. Selden (Rolm)
* and M. van Buuren)
*
* If you want to change the external circuitry of the SLIC PBL 3736, you have to make
* changes in this file (see external circuitry)
* example:          instead of having a 299 kΩ resistor between the nodes RSN and VOUT
*                   you would like to have a 200 kΩ resistor. In this case you would
*                   replace the line
*                   RRX    rsn    vout    299 k
*                   by the line
*                   RRX    rsn    vout    200 k
*
*                          RING   TIP     VCC     VEE     VIN     VOUT
*                          |      |       |       |       |       |
*                          |      |       |       |       |       |
.SUBCKT ericssonslic       ring   tip     +12 V   –12 V   vin     vout
*
* Resistances to avoid "floating nodes"
*
Rdummy1             +12 V  0      10G
Rdummy2             –12 V  0      10G
*******************************************************************
* External Circuitry
*
* Resistor (first letter "R") situated between
* |        node1
* |        |      and node2
* |        |      |      value of the resistor (in Ω)
* |        |      |      |
RF1        tip    tipx   20
RF2        ring   ringx  20
RDC1       rdc    9      20 k
RDC2       9      rsn    20 k
RT         vtx    rsn    560 k
RIX        vin    0      21.92 k
RRX        rsn    vout   299 k
*
```

```
* Capacitor (first letter "C") situated between
* |         node1
* |         |         and node2
* |         |         |         value of the capacitor (in Farad)
* |         |         |         |
CT          tipx      0         2.2 nF
CR          ringx     0         2.2 nF
CDC         9         0         0.15 µF
CTX         vtx       vin       0.981 µF
CHP         10        0         0.2205 µF
**********************************************************************
* simplified ac transmission circuit of the SLIC
*
* Resistor (first letter "R") situated between
* |         node1
* |         |         and node2
* |         |         |         value of the resistor (in Ω)
* |         |         |         |
RF1a        tipx      1         20
RF2a        ringx     4         20
ROP1        1         2         1
ROP2        4         5         1
ROP3        tipx      3         9.98 k
ROP4        ringx     6         9.98 k
RHP         7         10        401.9 k
RLP1        7         7a        20
*
* Capacitor (first letter "C") situated between
* |         node1
* |         |         and node2
* |         |         |         value of the capacitor (in Farad)
* |         |         |         |
C7          1         0         6000 µF
C8          4         0         6000 µF
C9          7a        0         6000 µF
*
* Independent Voltage Source
*
* V(name)   (+)node   (–)node   (dc)value
* |         |         |         |
* |         |         |         |
VRSN        RSN       0         DC 0
*
* Current controlled Current Source
*
```

```
* F(name)   (+)node  (–)node  (controlling V device)name
* |         |        |        |
* |         |        |        |
* |         |        |        |         gain
* |         |        |        |         |
* |         |        |        |         |
F1          3        0        VRSN      2
F2          0        6        VRSN      2
*
* Voltage-controlled Voltage Sources
*
* E(name)   (+)node  (–)node
* |         |        |        (+controlling) node
* |         |        |        |         (–controlling) node
* |         |        |        |         |         gain
* |         |        |        |         |         |
E1          2        0        3         1         1.0E4
E2          5        0        6         4         1.0E4
E3          7        0        tipx      ringx     1.0
E4          rdc      0        7a        0         0.05
E5          vtx      0        7         10        1.0
.ENDS ericssonslic
.END
```

Appendix B
Test Circuit 'KSLIC.CIR'

```
circuit for calculating K-parameters
*
* This program does an ac-analysis of the SLIC circuit. The results of the ac-analysis are
* used to calculate the K-parameters of the SLIC circuit (see chapter 3.3.1 K-parameters).
*
* Version 3.1 by Ed van Leeuwen
* Version 3.2 by Mark van Buuren
* Version 3.3 by Klaus Kliese, Manfred Beck
*
* Note:
* This ac-analysis is valid for a 600 Ω impedance (USA requirements). If you wish to
* do calculations for other country specifications, you have to change the generator
* impedance Rg and the load impedance Rload. To give you an example, the
* generator and the load impedances according to the German requirements (complex
* impedances) are written as comment lines below the impedances of the US-American
* requirements
*
* circuit for calculating K-parameters K11 K21 (vout = 0)
.lib kslic.lib
vcc +12V 0 12V
vee 0 –12V 12V
xslic ring tip +12V –12V vin vout SLIC
vg 1a tip ac 1.0
vosc vout 0 dc 0
* generator impedance according to US-American requirements
Rg 1a ring 600
* generator impedance according to German requirements
* Rgs 1a 1b 220
* Rgp 1b ring 820
* Cgp 1b ring 115 nF
.ac lin 399   10   3990
.print ac vr([vin]) vi([vin]) vr([ring],[tip]) vi([ring],[tip])
.print ac vr([1a,ring]) vi([1a,ring])
.options nomod
.probe ; *ipsp*
.end
circuit for calculating K-parameters K12 K22 (V1 = –Zg.i1)
.lib kslic.lib
vcc +12V  0 12V
vee  0 –12V 12V
xslic ring tip +12v –12v vin vout slic
vosc vout 0 ac 1.0
* generator impedance according to US-American requirements
```

```
Rg ring tip 600
* generator impedance according to German requirements
* Rgs ring 1a 220
* Rgp 1a tip 820
* Cgp 1a tip 115 nF
.ac lin 399   10   3990
.print ac vr([vin]) vi([vin]) vr([vout]) vi([vout])
.print ac vr([ring],[tip]) vi([ring],[tip])
.options nomod
.probe
.end
circuit for calculating ZSLI0 (ring and tip short circuit)
.lib kslic.lib
Vcc +12v 0 12v
Vee 0 –12v 12v
xslic ring tip +12v –12v vin vout slic
vosc vout 0 ac 1.0
vload ring tip 0
.ac lin 30   10   16.0E3
.print ac v([vout]) v([vin])
.options nomod
.probe
.end
circuit for calculating ZSLIload (load impedance between ring and tip)
.lib kslic.lib
Vcc +12v 0 12v
Vee 0 –12v 12v
xslic ring tip +12v –12v vin vout slic
vosc vout 0 ac 1.0
* load impedance according to US-American requirements
rload ring tip 600
* load impedance according to German requirements
* Rloads ring 1a 220
* Rloadp 1a tip 820
* Cloadp 1a tip 115 nF
.ac lin 30   10   16.0E3
.print ac v([vout]) v([vin])
.options nomod
.probe
.end
circuit for calculating ZSLIopen (ring and tip open circuit)
.lib kslic.lib
Vcc +12v 0 12v
Vee 0 –12v 12v
xslic ring tip +12v –12v vin vout slic
vosc vout 0 ac 1.0
rload ring tip 10T ; for rejecting 'floating' errors from spice, see spicemanual
.ac lin 30   10   16.0E3
```

```
.print ac v([vout]) v([vin])
.options nomod
.end
```

Appendix C

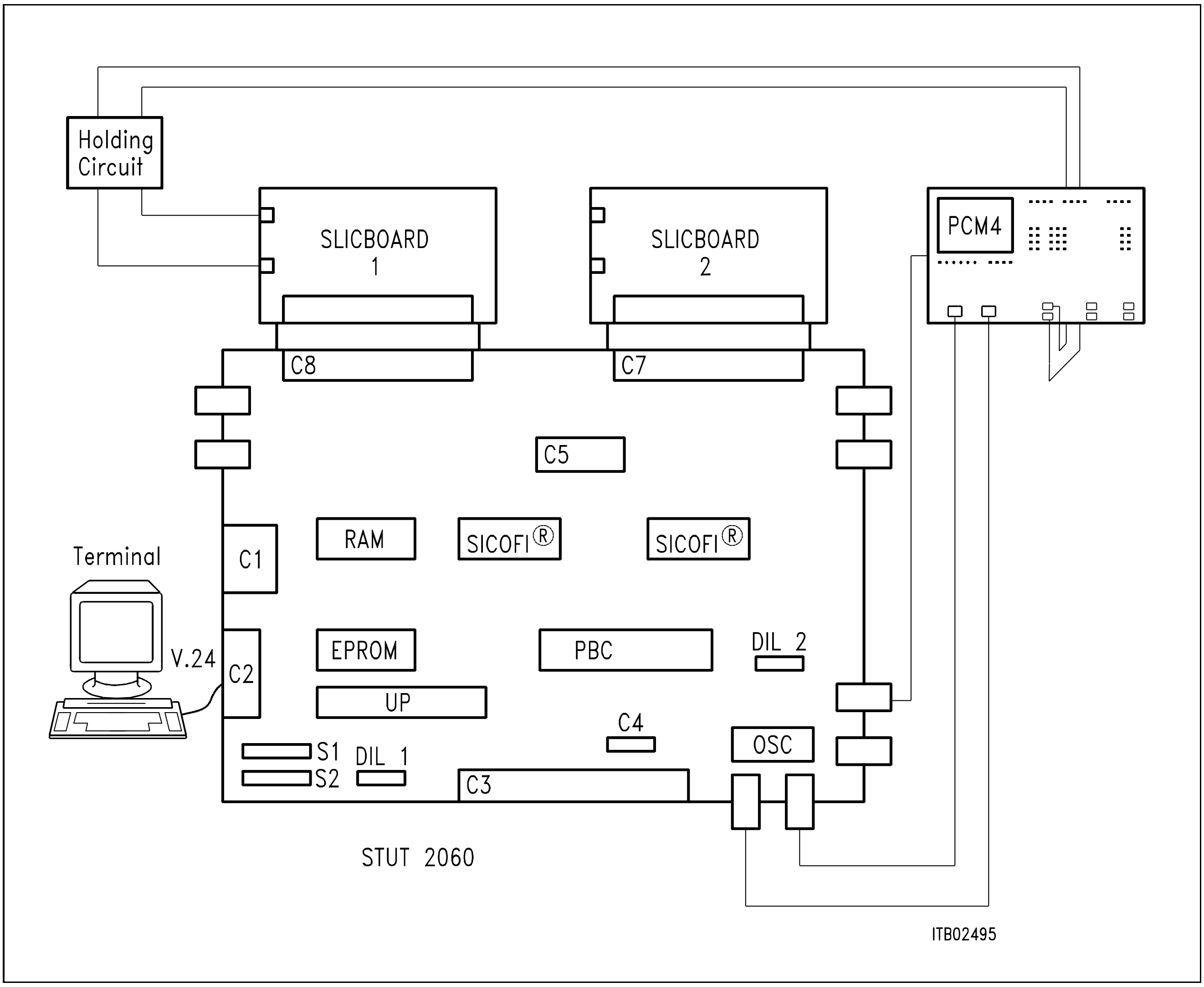
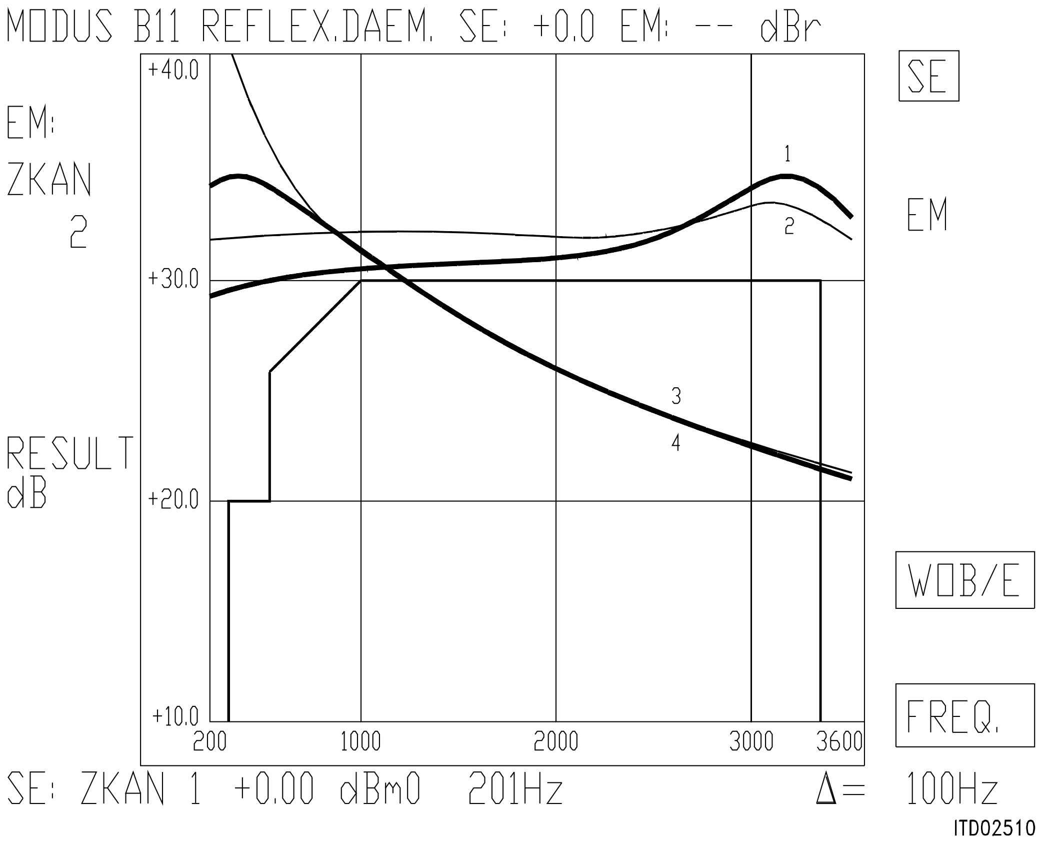


Diagram of the Measurement System

Appendix D



Plots of Measurements USA Specification: Return Loss

1 Measured, Filters ON
2 Calculated, Filters ON
3 Measured, Filters OFF
4 Calculated, Filters OFF

MODUS A11 PEGELMESSG. SE: -- EM: -- dBr

EM: ZKAN 2

RESULT

dBm0

1

FREQ/Hz	RES/dBm0	FREQ/Hz	RES/dBm0
201	−0.38	2208	−0.16
301	−0.06	2309	−0.19
402	−0.12	2409	−0.20
502	−0.10	2509	−0.19
602	−0.08	2610	−0.20
703	−0.06	2710	−0.21
803	−0.04	2811	−0.22
903	−0.05	2911	−0.23
1004	−0.06	3011	−0.24
1104	−0.06	3112	−0.27
1205	−0.06	3212	−0.30
1305	−0.08	3312	−0.36
1405	−0.09	3413	−0.45
1506	−0.10	3513	−0.63
1606	−0.11		
1706	−0.12		
1807	−0.14		
1907	−0.13		
2008	−0.14		
2108	−0.16		

A−A

A−D

D−A

D−D

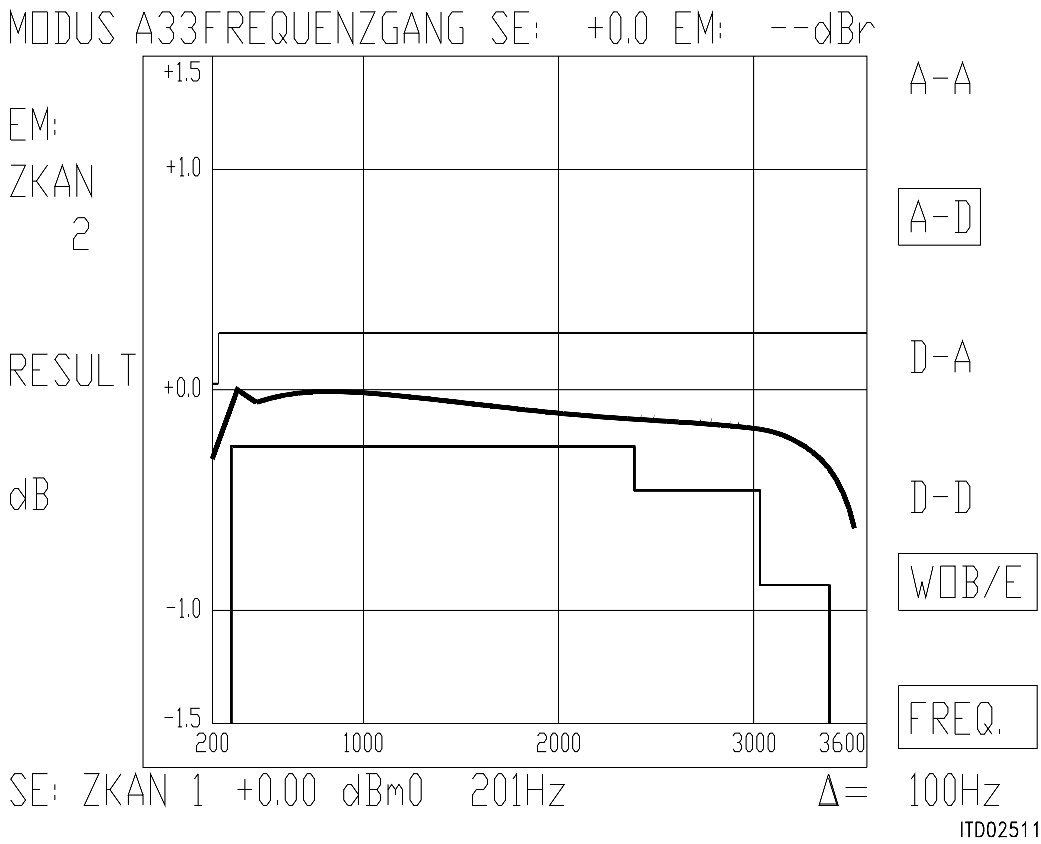
WOB/E

FREQ.

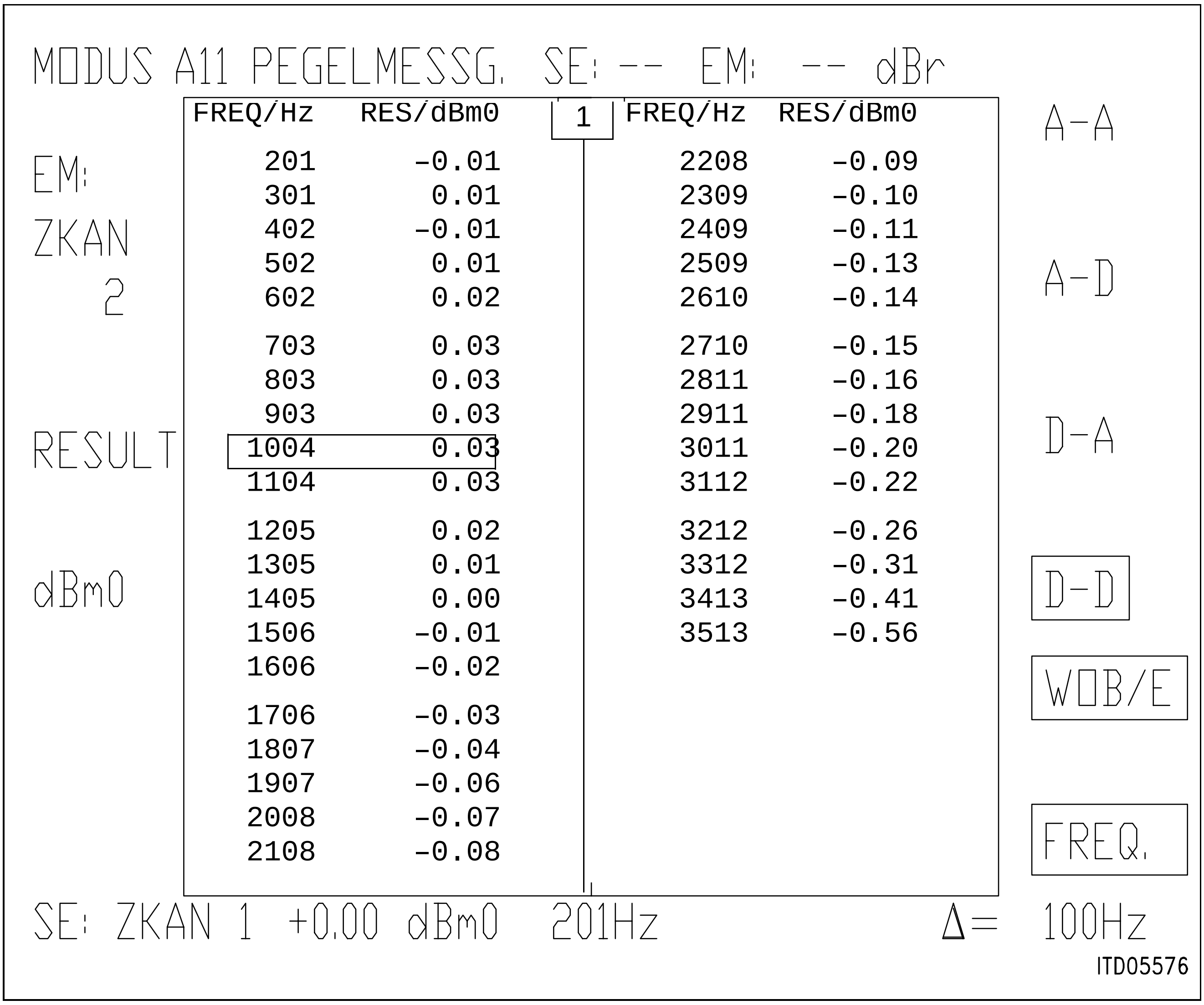
SE: ZKAN 1 +0.00 dBm0 201Hz Δ= 100Hz

ITD05575

USA Specification: Transmit Level (A–D)

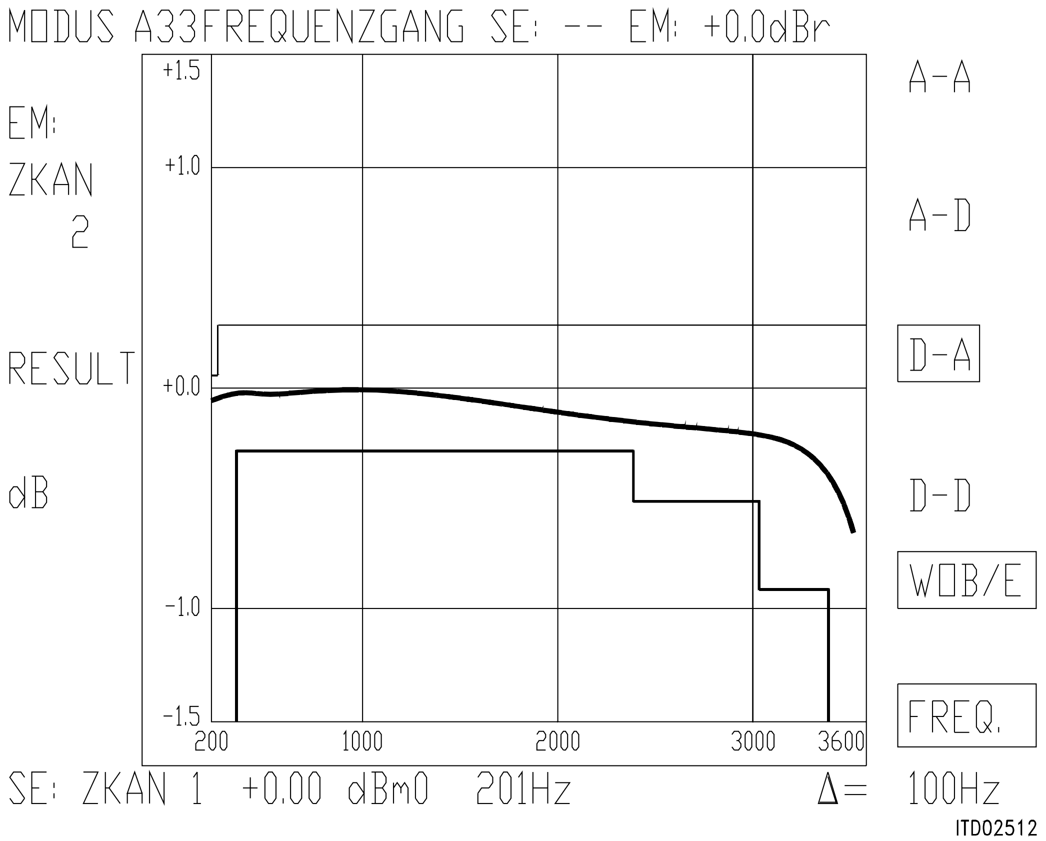


USA Specification: Deviation from Reference Level (0 dB), Transmit Direction

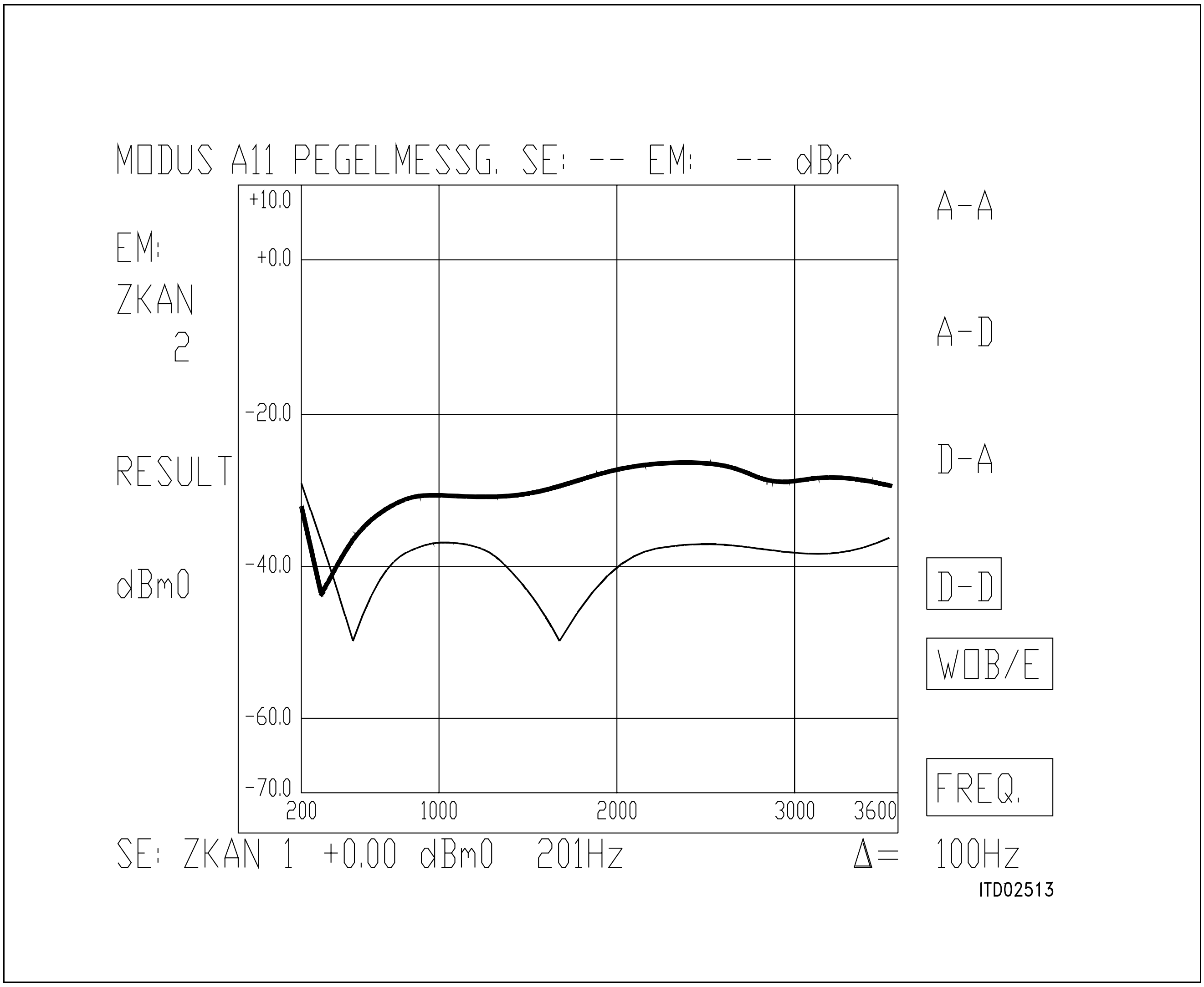


FREQ/Hz	RES/dBm0	FREQ/Hz	RES/dBm0
201	–0.01	2208	–0.09
301	0.01	2309	–0.10
402	–0.01	2409	–0.11
502	0.01	2509	–0.13
602	0.02	2610	–0.14
703	0.03	2710	–0.15
803	0.03	2811	–0.16
903	0.03	2911	–0.18
1004	0.03	3011	–0.20
1104	0.03	3112	–0.22
1205	0.02	3212	–0.26
1305	0.01	3312	–0.31
1405	0.00	3413	–0.41
1506	–0.01	3513	–0.56
1606	–0.02		
1706	–0.03		
1807	–0.04		
1907	–0.06		
2008	–0.07		
2108	–0.08		

USA Specification: Level in Receive Direction (D–A)

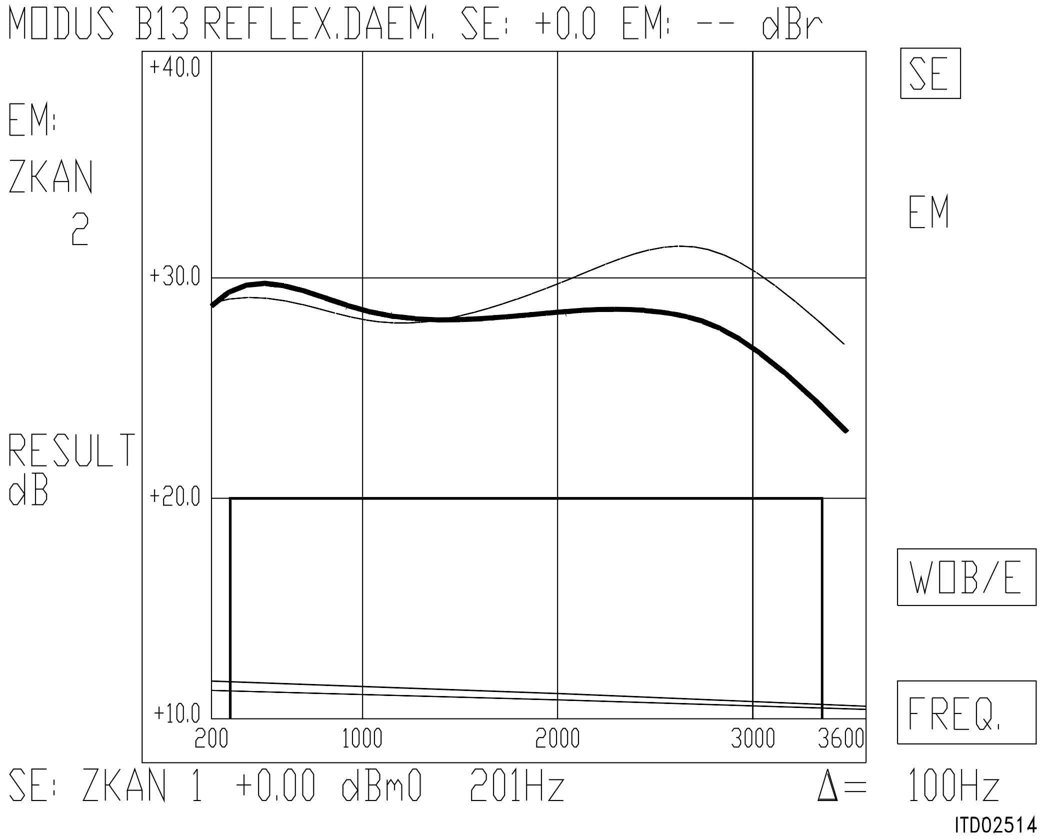


USA Specification: Deviation from Reference Level (0 dB), Receive Direction



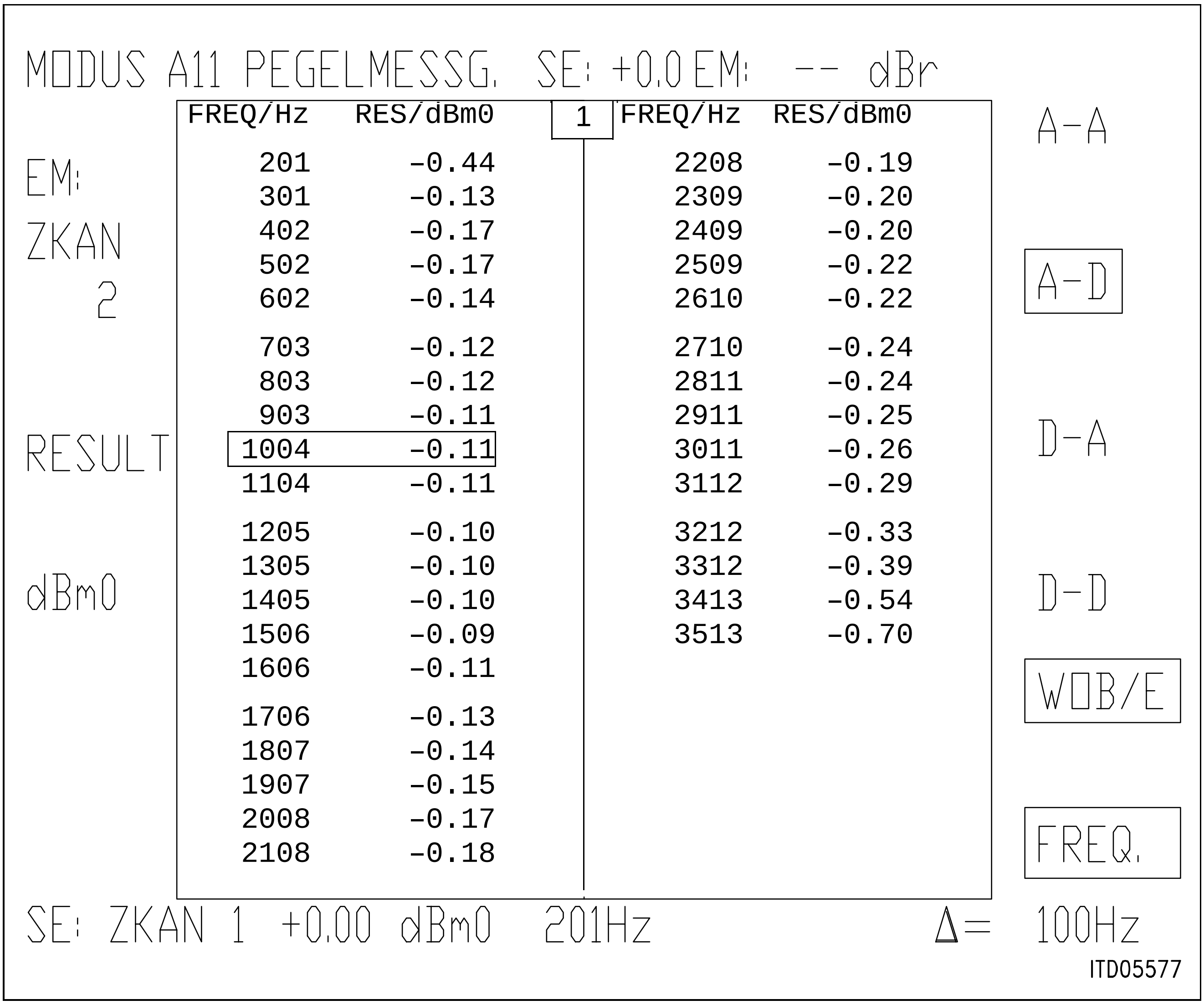
USA Specification: Transhybrid Loss (D–D)

1	Measured
2	Calculated

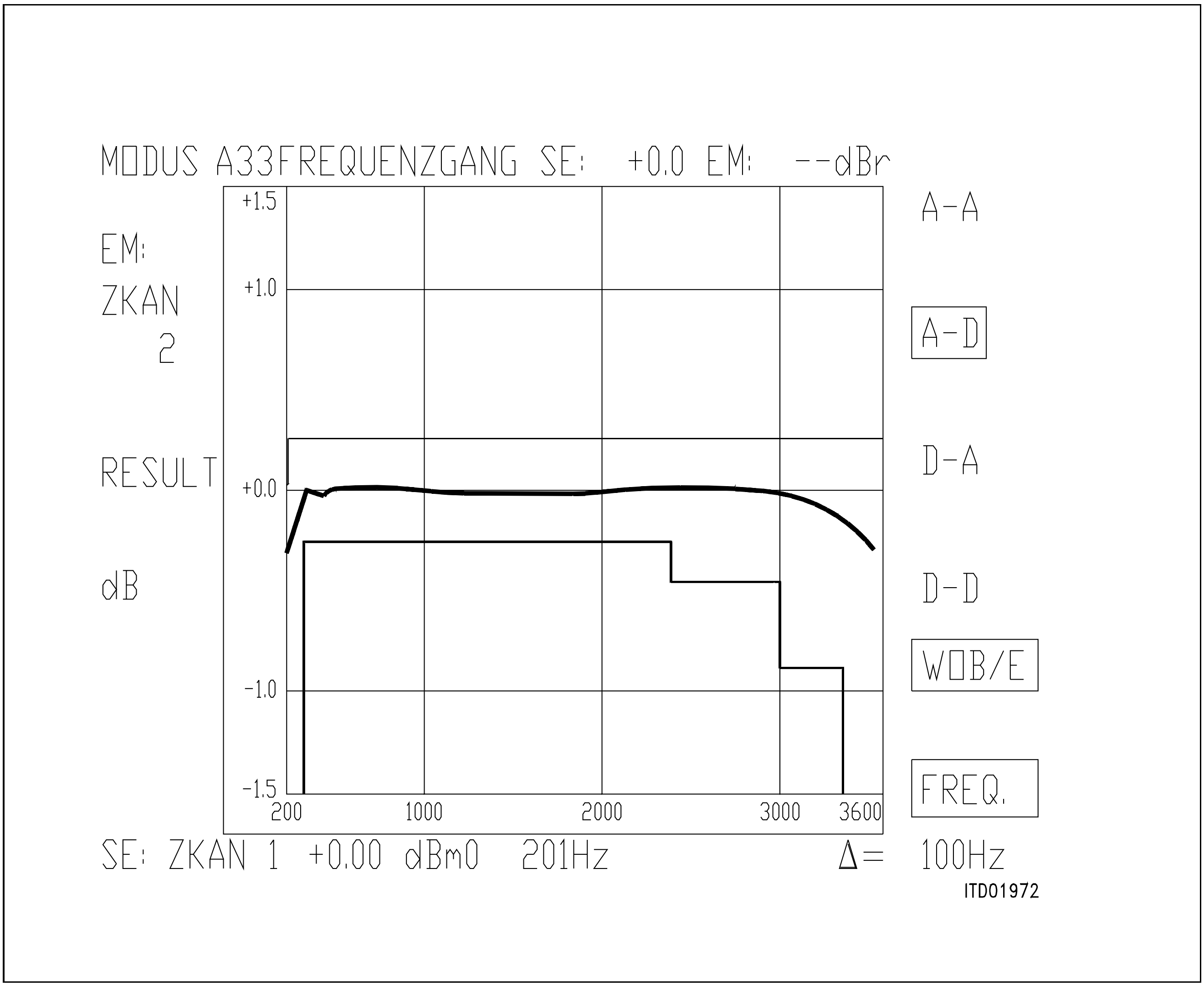


German Specification: Return Loss

1	Measured, Filters ON
2	Calculated, Filters ON
3	Measured, Filters OFF
4	Calculated, Filters OFF



German Specification: Transmit Level (A–D)



German Specification: Deviation from Reference Level (0 dB), Transmit Direction

MODUS A11 PEGELMESSG. SE: +0.0 EM: -- dBr

EM: ZKAN 2

RESULT dBm0

FREQ/Hz	RES/dBm0
201	–6.97
301	–6.96
402	–7.00
502	–7.01
602	–7.03
703	–7.04
803	–7.04
903	–7.04
1004	–7.03
1104	–7.02
1205	–7.01
1305	–6.99
1405	–6.98
1506	–6.97
1606	–6.97
1706	–6.98
1807	–6.99
1907	–7.01
2008	–7.03
2108	–7.06

1

FREQ/Hz	RES/dBm0
2208	–7.08
2309	–7.10
2409	–7.11
2509	–7.12
2610	–7.13
2710	–7.14
2811	–7.14
2911	–7.14
3011	–7.15
3112	–7.18
3212	–7.23
3312	–7.31
3413	–7.45
3513	–7.68

A–A

A–D

D–A

D–D

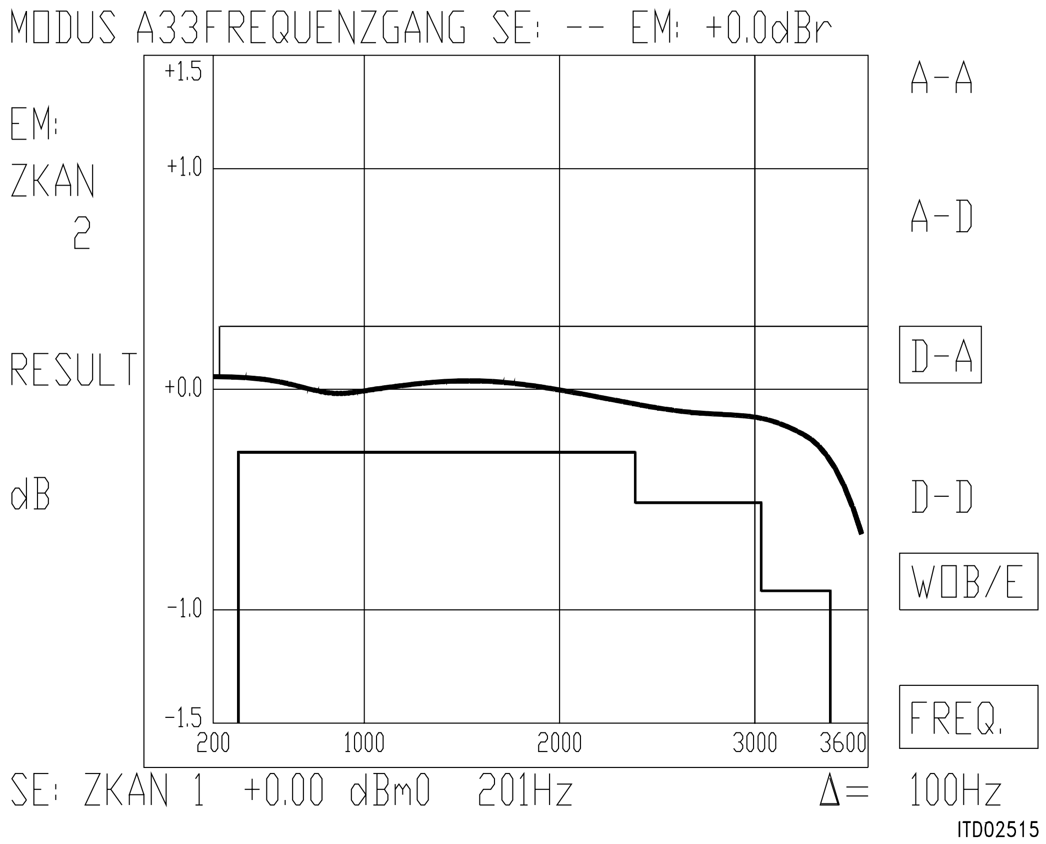
WOB/E

FREQ.

SE: ZKAN 1 +0.00 dBm0 201Hz Δ= 100Hz

ITD05577

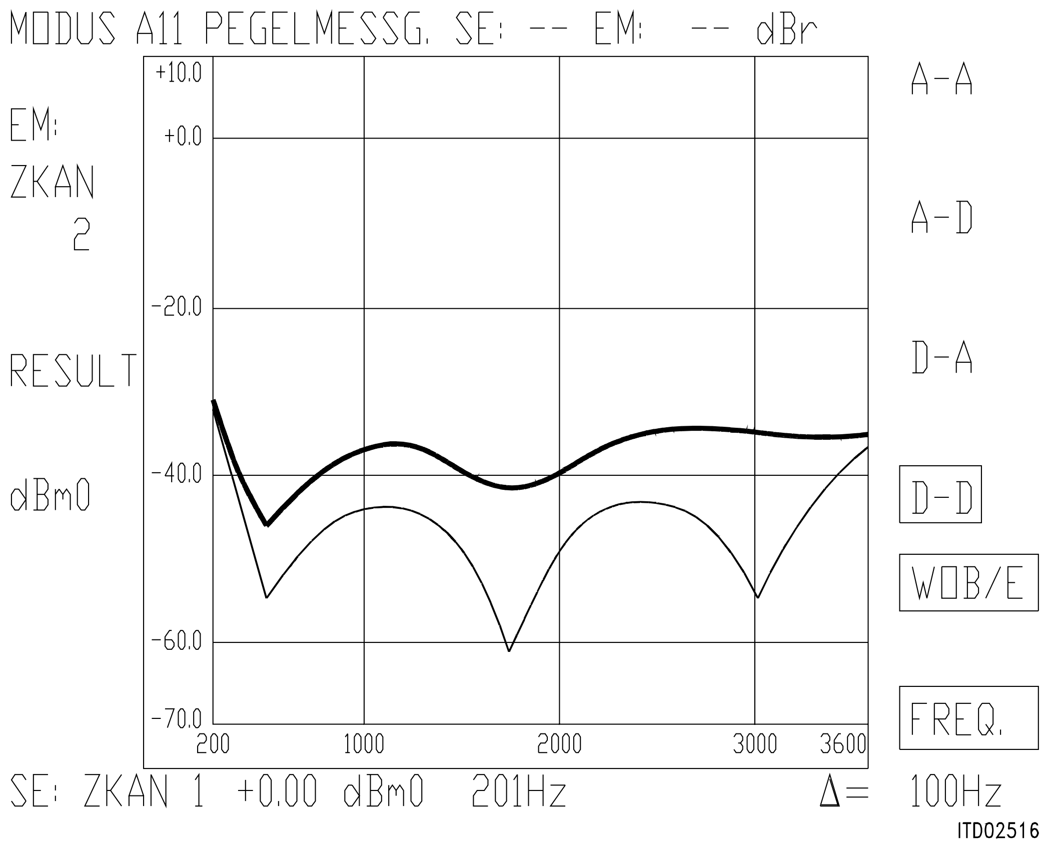
German Specification: Level in Receive Direction (D–A)



German Specification: Deviation from Reference Level (– 7 dB), Receive Direction

German Specification: Transhybrid Loss (D–D)

1 Measured
2 Calculated



German Specification: Transhybrid Loss (D–D)

1	Measured
2	Calculated

Appendix E

SICOFI® File 'USA.SPE'

```
FREF = 1014.0 LAW = A
VREF = 0.7750 RLX = 0. RLR = 0.0
ABIMP = ZI
ZLRP1 = 000.   ZLCP1 = 0.   ZLRP2 = 0.   ZLCP2 = 0.
ZLRS  = 600.   ZLCS  = 0.
ZIRP1 = 000.   ZICP1 = 0.   ZIRP2 = 0.   ZICP2 = 0.
ZIRS  = 600.   ZICS  = 0.
Z3RP1 = 000.   Z3CP1 = 0.   Z3RP2 = 0.   Z3CP2 = 0.
Z3RS  = 600.   Z3CS  = 0.
ZRRP1 = 000.   ZRCP1 = 0.   ZRRP2 = 0.   ZRCP2 = 0.
ZRRS  = 600.   ZRCS  = 0.
ZRE
FR          300      500      1K       3.4k
AT–         0        20       30       30
AT+         20       26       30       0
ZMIR
FR          4k       12k
AT–         30       3
AT+         30       3
DA,UPPER
FR          300      500      2.7k     3k       3.4k
AT–         100      .75      .25      .35      .75
AT+         .75      .25      .35      .75      100
DA,LOWER
FR          300      3.4k
AT–         0        –.25
AT+         –.25     0
DA,DELAY
FR          500      600      1k       2.6k     2.8k
GD–         10k      .420     .150     .085     .150
GD+         .420     .150     .085     .150     10k
AD,UPPER
FR          300      500      2.7k     3k       3.4k
AT–         100      .75      .25      .35      .75
AT+         .75      .25      .35      .75      100
AD,LOWER
FR          300      3.4k
AT–         0        –.25
AT+         –.25     0
AD,DELAY
FR          500      600      1k       2.6k     2.8k
GD–         10k      .420     .150     .085     .150
GD+         .420     .150     .085     .150     10k
DD
FR          300      500      2.5K     3.4K
AT–         0        27       27       23
AT+         23       27       27       0
```

SICOFI® File 'BRD.SPE'

```
FREF = 1014.0 LAW = A
VREF = 0.948 RLX = 0. RLR = –7.0
ABIMP = ZI
ZLRP1 = 820.    ZLCP1 = 0.    ZLRP2 = 0.    ZLCP2 = 0.115E–6
ZLRS  = 220.    ZLCS  = 0.
ZIRP1 = 820.    ZICP1 = 0.    ZIRP2 = 0.    ZICP2 = 0.115E–6
ZIRS  = 220.    ZICS  = 0.
Z3RP1 = 820.    Z3CP1 = 0.    Z3RP2 = 0.    Z3CP2 = 0.115E–6
Z3RS  = 220.    Z3CS  = 0.
ZRRP1 = 820.    ZRCP1 = 0.    ZRRP2 = 0.    ZRCP2 = 0.115E–6
ZRRS  = 220.    ZRCS  = 0.
ZRE
FR          300       500       3.4k
AT–         0         20        20
AT+         16        20        0
ZMIR
FR          4k        12k
AT–         30        3
AT+         30        3
DA,UPPER
FR          300       500       2.7k      3k        3.4k
AT–         100       .75       .25       .35       .75
AT+         .75       .25       .35       .75       100
DA,LOWER
FR          300       3.4k
AT–         0         –.25
AT+         –.25      0
DA,DELAY
FR          500       600       1k        2.6k      2.8k
GD–         10K       .420      .150      .085      .150
GD+         .420      .150      .085      .150      10K
AD,UPPER
FR          300       500       2.7k      3k        3.4k
AT–         100       .75       .25       .35       .75
AT+         .75       .25       .35       .75       100
AD,LOWER
FR          300       3.4k
AT–         0         –.25
AT+         –.25      0
AD,DELAY
FR          500       600       1k        2.6k      2.8k
GD–         10k       .420      .150      .085      .150
GD+         .420      .150      .085      .150      10k
DD
FR          300       500       2.5k      3.4k
AT–         0         27        27        23
AT+         23        27        27        0
```

Appendix F
Control File ’KSICOFI.CTL’

```
SPEC = USA.SPE          SLIC = KSLIC.SLI
BYTE = REF1.BYT         CHNR = 0,A
PEB = 2060   VERSION = 4.4       REL = Y
ON = ALL
OPT = Z+X+R+B           ZXRB = NNNN
PZIN = 11  PSP = 3
FZP =         300.0      500.0     1000.0    1300.0    1500.0
              2000.0     2500.0    2900.0    3000.0    3200.0
              3400.0     7000.0    10000.    14000.
WFZ =         0.100      1.00      2.00      1.50      1.00
              3.00       1.00      1.00      1.00      3.00
              2.80       1.00      1.00      1.00
ZAUTO = Y     FZ = 300 3400
FR 300.00     3400.0
RDISP = N     RREFQ = N
FX 300.00     3400.0
XDISP = N     XREFQ = N
PB = 10        GWFB = 0.500E-01          BDF = 1
FBP =         300.0      500.0     700.0     1000.0    1500.0
              2100.0     2300.0    2900.0    3200.0    3300.0
WFB =         4.000      2.000     1.000     5.000     1.000
              2.000      1.000     5.000     1.000     1.000
BAUTO = Y     FB = 300 3400
APRE = 0.0     DPRE = 0.0    APOF = 0.0    DPOF = 0.0
AGR = 00     AGX = 00      TM3 = 000
```

Appendix G
Result File 'K_USA.RES'

```
Input_file_name: KSICOFI.CTL                     Date:13.03.91  09:37
SPEC = USA.SPE      SLIC = KSLIC.SLI
BYTE = REF.BYT      CHNR = 0,A
PLQ = N
ON = ALL            PEB = 2060   VERSION = 4.4 SHORT = N
OPT = Z+X+R+B       ZXRB = NNNN                 REL = Y
ZAUTO = Y           ZREP = N     ZSIGN = 1
FZ = 300.00   3400.0     ZLIM = 2.00
             PZIN = 11   PSP = 3
FZP =         300.00     500.00    1000.0    1300.0    1500.0
              2000.0     2500.0    2900.0    3000.0    3200.0
              3400.0     7000.0    10000.    14000.
WFZ =         .100       1.00      2.00      1.50      1.00
              3.00       1.00      1.00      1.00      3.00
              2.80       1.00      1.00      1.00
FR = 300.00   3400.0
RDISP = N     RREFQ = N  RREF = .31626E-01
FX = 300.00   3400.0
XDISP = N     XREFQ = N  XREF = -.42733
BAUTO = Y     BREP = N   BSIGN = 1
FB = 300.00   3400.0   BLIM = 2.00   BDF = 1
             PB = 10     GWFB = .500E-01
FBP =         300.00     500.00    700.00    1000.0    1500.0
              2100.0     2300.0    2900.0    3200.0    3300.0
WFB =         4.0000     2.0000    1.0000    5.0000    1.0000
              2.0000     1.0000    5.0000    1.0000    1.0000
APRE = .00     DPRE = .00  APOF = .00  DPOF = .00
AGX = 00      AGR = 00   TM3 = 000
XZQ =        -.11523440E+00   .22656250E+00    .34179690E-01
             -.21093750E+00   .93994140E-01
XRQ =         .97265630E+00   .31250000E-01   -.29296880E-02
              .48828130E-03  -.19531250E-02
XXQ =         .10273440E+01   .30883790E-01   -.19531250E-02
              .97656250E-03  -.19531250E-02
XBQ =        -.14453130E+00  -.71875000E+00   -.25341800E+00
              .15234380E+00   .52734380E-01
             -.97656250E-01   .13183590E-01    .78613280E-01
             -.80078130E-01   .37109380E-01
XGQ =         .53808590E+00   .21562500E+01
;
```

```
Bytes for Z-Filter (13):          30,FA,BA,52,14,C2,B1,2C
Bytes for R-Filter (2B):          F0,19,87,FC,29,16,00,BD
Bytes for X-Filter (23):          F0,19,87,FB,19,E5,0A,B5
Bytes for Gain-factors (30):      41,B2,00,23
2nd part of bytes B-Filter (0B): 00,35,C1,32,24,65,2B,AB
1st part of bytes B-Filter (03): 4B,2B,23,AB,B6,19,BB,23
Bytes for B-filter delay (18):   19,19,11,19
* PSPICE simulation of SLIC using K-parameters
* converted with the program KCONVERT V1.1

Run # 1

Z-FILTER calculation results

 Reference impedance for optimization:
ZIRP1 = .000     ZICP1 = .000    ZIRP2 = .000    ZICP2 = .000
ZIRS  = 600.     ZICS  = .000

 Calculated and quantized coefficients:

XZ  =   –.11501   .22666   .03412   –.20779   .09395
XZQ =   –.11523   .22656   .03418   –.21094   .09399
Bytes for Z-Filter (13)            30,FA,BA,52,14,C2,B1,2C

RETURN LOSS
```

FREQ (Hz)	loss (dB)	FREQ (Hz)	loss (dB)
100.	32.313	2000.	32.204
200.	32.155	2100.	32.181
300.	32.156	2200.	32.157
400.	32.136	2300.	32.173
500.	32.257	2400.	32.247
600.	32.319	2500.	32.404
700.	32.387	2600.	32.584
800.	32.527	2700.	32.819
900.	32.594	2800.	33.070
1000.	32.651	2900.	33.368
1100.	32.688	3000.	33.611
1200.	32.709	3100.	33.743
1300.	32.705	3200.	33.660
1400.	32.678	3300.	33.253
1500.	32.627	3400.	32.523
1600.	32.566	3500.	31.463
1700.	32.489	3600.	30.237
1800.	32.361	3700.	28.912
1900.	32.299	3800.	27.550

```
Min. Z-loop reserve:              26.008 dB at frequency: 8500.0 Hz
Min. Z-loop mirror reserve:       30.692 dB at frequency: 9000.0 Hz
```

```
Run # 1

X-FILTER calculation results

 Reference impedance for optimization:
ZIRP1 = .000     ZICP1 = .000    ZIRP2 = .000    ZICP2 = .000
ZIRS  = 600.     ZICS  = .000

 Calculated and quantized coefficients:

XX  =   1.02808   .03087   –.00199   .00098   –.00187
XXQ =   1.02734   .03088   –.00195   .00098   –.00195
Bytes for X–Filter (23):            F0,19,87,FB,19,E5,0A,B5

GX results:
All attenuation values (in dB) refer to FREF = 1014. Hz

RLX   SLIC+Z  AGX     VREF/VSIC   XREF    TM3     GX
.00 – .78 –   .00 –   6.17 –      –.43 –  .00 =   –6.70 ideal
.03 = .78 +   .00 +   6.17 +      –.43 +  .00 +   –6.67 quant

Second byte for PEB 2060 transmit gain: ,00,23
Calculation of transmit transfer function (AD)
All attenuation values (in dB) refer to FREF = 1014.0 Hz

TGref CA = .052 ms     TGref CB = .065 ms
```

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
100.	13.836	2.827	2000.	.043	.209
200.	.345	2.009	2100.	.048	.213
300.	.017	.796	2200.	.051	.219
400.	.041	.489	2300.	.054	.226
500.	.039	.365	2400.	.054	.233
600.	.028	.301	2500.	.056	.243
700.	.019	.264	2600.	.060	.253
800.	.009	.241	2700.	.063	.265
900.	.003	.226	2800.	.067	.280
1000.	–.000	.216	2900.	.075	.298
1100.	–.001	.208	3000.	.088	.319
1200.	–.000	.204	3100.	.106	.345
1300.	.002	.201	3200.	.138	.378
1400.	.007	.199	3300.	.186	.420
1500.	.012	.199	3400.	.268	.476
1600.	.018	.199	3500.	.410	.556
1700.	.026	.200	3600.	.676	.676
1800.	.032	.202	3700.	1.240	.871
1900.	.039	.205	3800.	2.655	.000

```
Run # 1

R-FILTER calculation results

 Reference impedance for optimization:
ZIRP1 = .000     ZICP1 = .000    ZIRP2 = .000    ZICP2 = .000
ZIRS  = 600.     ZICS  = .000

 Calculated and quantized coefficients:

XR  =   .97294   .03127   -.00286   .00037   -.00198
XRQ =   .97266   .03125   -.00293   .00049   -.00195
Bytes for R-Filter (2B):           F0,19,87,FC,29,16,00,BD

GR results:
All attenuation values (in dB) refer to FREF = 1014. Hz

-RLR   SLIC+Z  AGR     VSIC/VREF  RREF   GR
.00 -  .76 -   .00 -   -6.17 -    .03 =  5.38 ideal
.00 =  .76 +   .00 +   -6.17 +    .03 +  5.38 quant

First byte for PEB 2060 receive gain (30): 41,B2
Calculation of receive transfer function (DA)
All attenuation values (in dB) refer to FREF = 1014.0 Hz

TGref CA = .184 ms     TGref CB = .167 ms
```

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
100.	.029	.000	2000.	.039	.053
200.	.040	.007	2100.	.043	.059
300.	.039	.009	2200.	.047	.065
400.	.035	.011	2300.	.049	.073
500.	.029	.012	2400.	.052	.081
600.	.022	.014	2500.	.054	.091
700.	.015	.016	2600.	.056	.102
800.	.008	.017	2700.	.060	.115
900.	.003	.019	2800.	.065	.131
1000.	-.001	.021	2900.	.072	.148
1100.	-.002	.023	3000.	.085	.170
1200.	-.002	.025	3100.	.105	.196
1300.	.000	.028	3200.	.135	.229
1400.	.004	.030	3300.	.184	.271
1500.	.009	.033	3400.	.267	.328
1600.	.014	.036	3500.	.408	.408
1700.	.022	.039	3600.	.675	.526
1800.	.028	.043	3700.	1.238	.723
1900.	.033	.048	3800.	2.654	1.060

```
Run # 1

B-FILTER calculation results

 Reference impedance for optimization:
ZLRP1 = .000     ZLCP1 = .000    ZLRP2 = .000   ZLCP2 = .000
ZLRS  = 600.     ZLCS  = .000

 Calculated and quantized coefficients:

XB  =   -.14825   -.71061   -.25357   .15054   .05259
        -.09832    .01320    .07862  -.07985   .03775
XBQ =   -.14453   -.71875   -.25342   .15234   .05273
        -.09766    .01318    .07861  -.08008   .03711
2nd part of bytes B-Filter (0B):    00,35,C1,32,24,65,2B,AB
1st part of bytes B-Filter (03):    4B,2B,23,AB,B6,19,BB,23

TRANS HYBRID LOSS

FREQ        loss                FREQ       loss
(Hz)        (dB)                (Hz)       (dB)
 100.       34.515              2000.      40.546
 200.       28.677              2100.      39.164
 300.       34.913              2200.      38.275
 400.       43.719              2300.      37.712
 500.       52.062              2400.      37.445
 600.       42.911              2500.      37.399
 700.       39.398              2600.      37.484
 800.       37.744              2700.      37.598
 900.       36.977              2800.      37.641
1000.       36.864              2900.      37.537
1100.       37.292              3000.      37.359
1200.       38.247              3100.      37.168
1300.       39.698              3200.      36.982
1400.       41.846              3300.      36.732
1500.       44.876              3400.      36.160
1600.       48.419              3500.      34.939
1700.       48.770              3600.      33.277
1800.       45.555              3700.      31.896
1900.       42.603              3800.      32.162

Additional B-filter delay (in seconds): .625E-04
Bytes for B-filter delay (18):         19,19,11,19
```

```
Result File 'K_BRD.RES'
Input_file_name:    KSICOFI.CTL           Date: 13.03.91   09:51
SPEC = BRD.SPE      SLIC = KSLIC.SLI
BYTE = REF.BYT      CHNR = 0,A
PLQ = N
ON = ALL            PEB = 2060   VERSION = 4.4 SHORT = N
OPT = Z+X+R+B       ZXRB = NNNN  REL = Y
ZAUTO = Y           ZREP = N     ZSIGN = 1
FZ = 300.00   3400.0     ZLIM = 2.00
             PZIN = 11   PSP = 3
FZP =         300.00     500.00    1000.0    1300.0    1500.0
              2000.0     2500.0    2900.0    3000.0    3200.0
              3400.0     7000.0    10000.    14000.
WFZ =         .100       1.00      2.00      1.50      1.00
              3.00       1.00      1.00      1.00      3.00
              2.80       1.00      1.00      1.00
FR = 300.00   3400.0
RDISP = N     RREFQ = N  RREF = 5.6169
FX = 300.00   3400.0
XDISP = N     XREFQ = N  XREF = -.12375E-01
BAUTO = Y     BREP = N   BSIGN = 1
FB =          300.00     3400.0    BLIM = 2.00 BDF = 1
PB = 10       GWFB = .500E-01
FBP =         300.00     500.00    700.00    1000.0    1500.0
              2100.0     2300.0    2900.0    3200.0    3300.0
WFB =         4.0000     2.0000    1.0000    5.0000    1.0000
              2.0000     1.0000    5.0000    1.0000    1.0000
APRE = .00    DPRE = .00 APOF = .00 DPOF = .00
AGX = 00      AGR = 01   TM3 = 000
XZQ =         -.37695310E+00  -.32812500E+00   .61279300E-01
               .22656250E+00  -.89843750E-01
XRQ =          .68750000E+00  -.27343750E+00   .59082030E-01
              -.21484380E-01   .92773440E-02
XXQ =          .10175780E+01  -.26367190E-01   .18554690E-01
              -.63476560E-02   .19531250E-02
XBQ =         -.66894530E-01  -.32031250E+00  -.30468750E+00
              -.10925290E+00  -.22460940E-01
              -.47851560E-01  -.22460940E-01   .25390630E-01
              -.27465820E-01   .13916020E-01
XGQ =          .68359380E+00   .16875000E+01
;
```

```
Bytes for Z-Filter (13):          C0,B1,C2,41,2E,2A,92,EA
Bytes for R-Filter (2B):          70,13,2E,41,BC,4A,11,12
Bytes for X-Filter (23):          70,19,BF,61,13,BD,02,36
Bytes for Gain-factors (30):      21,C1,10,12
2nd part of bytes B-Filter (0B): 00,B6,DB,DB,B5,E1,B1,AC
1st part of bytes B-Filter (03): EC,B1,BB,A7,B2,2A,C3,34
Bytes for B-filter delay (18):    9,19,11,19
* PSPICE simulation of SLIC using K-parameters
* converted with the program KCONVERT V1.1

Run # 1

Z-FILTER calculation results

 Reference impedance for optimization:
ZIRP1 = 820.     ZICP1 = .000    ZIRP2 = .000    ZICP2 = .115E-06
ZIRS  = 220.     ZICS  = .000

 Calculated and quantized coefficients:

XZ  =   -.37740   -.32749   .06130   .22499   -.08919
XZQ =   -.37695   -.32813   .06128   .22656   -.08984
Bytes for Z-Filter (13):             C0,B1,C2,41,2E,2A,92,EA

RETURN LOSS
```

FREQ (Hz)	loss (dB)	FREQ (Hz)	loss (dB)
100.	27.280	2000.	29.735
200.	28.873	2100.	29.978
300.	29.137	2200.	30.346
400.	29.107	2300.	30.692
500.	29.029	2400.	30.988
600.	28.887	2500.	31.257
700.	28.698	2600.	31.418
800.	28.615	2700.	31.409
900.	28.492	2800.	31.322
1000.	28.400	2900.	31.025
1100.	28.374	3000.	30.598
1200.	28.354	3100.	30.020
1300.	28.399	3200.	29.324
1400.	28.444	3300.	28.584
1500.	28.579	3400.	27.795
1600.	28.728	3500.	26.976
1700.	28.913	3600.	26.197
1800.	29.144	3700.	25.398
1900.	29.395	3800.	24.658

```
Min. Z-loop reserve:          27.109 dB at frequency: 6000.0 Hz
Min. Z-loop mirror reserve:   30.685 dB at frequency: 6000.0 Hz
```

```
Run # 1

X-FILTER calculation results

 Reference impedance for optimization:
ZIRP1 = 820.     ZICP1 = .000    ZIRP2 = .000    ZICP2 = .115E–06
ZIRS  = 220.     ZICS  = .000

 Calculated and quantized coefficients:

XX  =   1.01740   –.02620   .01872   –.00629   .00217
XXQ =   1.01758   –.02637   .01855   –.00635   .00195
Bytes for X-Filter (23):            70,19,BF,61,13,BD,02,36

GX results:
All attenuation values (in dB) refer to FREF = 1014. Hz

RLX    SLIC+Z  AGX     VREF/VSIC  XREF    TM3    GX
.00 –  –.01 –  .00 –   4.41 –     –.01 –  .00 =  –4.58 ideal
–03 =  –.01 +  .00 +   4.41 +     –.01 +  .00 +  –4.54 quant

Second byte for PEB 2060 transmit gain: ,10,12
Calculation of transmit transfer function (AD)
All attenuation values (in dB) refer to FREF = 1014.0 Hz

TGREF CA = .052 ms     TGREF CB = .065 ms
```

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
100.	13.845	2.881	2000.	.026	.208
200.	.340	2.019	2100.	.036	.212
300.	.010	.798	2200.	.042	.216
400.	.034	.488	2300.	.049	.222
500.	.036	.364	2400.	.054	.229
600.	.028	.298	2500.	.060	.237
700.	.019	.261	2600.	.063	.250
800.	.010	.238	2700.	.064	.266
900.	.005	.223	2800.	.067	.277
1000.	.001	.212	2900.	.071	.297
1100.	–.003	.206	3000.	.079	.319
1200.	–.005	.201	3100.	.095	.346
1300.	–.008	.195	3200.	.126	.379
1400.	–.007	.199	3300.	.181	.423
1500.	–.006	.193	3400.	.274	.480
1600.	–.001	.196	3500.	.438	.564
1700.	.005	.200	3600.	.738	.680
1800.	.010	.197	3700.	1.350	.878
1900.	.018	.202	3800.	2.829	.000

```
Run # 1

R-FILTER calculation results

 Reference impedance for optimization:
ZIRP1 = 820.     ZICP1 = .000    ZIRP2 = .000    ZICP2 = .115E-06
ZIRS  = 220.     ZICS  = .000

 Calculated and quantized coefficients:

XR  =   .69865   -.27517   .05921   -.02170   .00928
XRQ =   .68750   -.27344   .05908   -.02148   .00928
Bytes for R-Filter (2B):           70,13,2E,41,BC,4A,11,12

GR results:
All attenuation values (in dB) refer to FREF = 1014. Hz

-RLR    SLIC+Z   AGR     VSIC/VREF  RREF    GR
7.00 -  -3.54 -  6.03 -  -4.41 -    5.62 =  3.31 ideal
7.00 =  -3.54 +  6.03 +  -4.41 +    5.62 +  3.30 quant

First byte for PEB 2060 receive gain (30): 21,C1
Calculation of receive transfer function (DA)
All attenuation values (in dB) refer to FREF = 1014.0 Hz

TGREF CA = .212 ms     TGREF CB = .195 ms

FREQ       loss      GD           FREQ      loss      GD
(Hz)       (dB)      (msec)       (Hz)      (dB)      (msec)
 100.      -.083     .050         2000.     -.040      .047
 200.      -.077     .013         2100.     -.024      .053
 300.      -.050     .006         2200.     -.008      .056
 400.      -.034     .003         2300.       .003      .066
 500.      -.007     .002         2400.       .010      .074
 600.       .010     .000         2500.       .010      .085
 700.       .022     .001         2600.       .005      .098
 800.       .030     .002         2700.     -.004      .113
 900.       .025     .004         2800.     -.013      .129
1000.       .013     .005         2900.     -.021      .151
1100.      -.004     .010         3000.     -.021      .177
1200.      -.028     .017         3100.     -.008      .206
1300.      -.042     .014         3200.       .028      .243
1400.      -.063     .025         3300.       .099      .288
1500.      -.076     .025         3400.       .222      .349
1600.      -.075     .028         3500.       .430      .429
1700.      -.077     .038         3600.       .790      .550
1800.      -.068     .035         3700.     1.478      .747
1900.      -.055     .039         3800.     3.051     1.086
```

```
Run # 1

B-FILTER calculation results

 Reference impedance for optimization:
ZLRP1 = 820.     ZLCP1 = .000    ZLRP2 = .000    ZLCP2 = .115E-06
ZLRS  = 220.     ZLCS  = .000

 Calculated and quantized coefficients:

XB  =   -.06671   -.32085   -.30579   -.10920   -.02212
        -.04818   -.02290    .02514   -.02751    .01381
XBQ =   -.06689   -.32031   -.30469   -.10925   -.02246
        -.04785   -.02246    .02539   -.02747    .01392
2nd part of bytes B-Filter (0B):     00,B6,DB,DB,B5,E1,B1,AC
1st part of bytes B-Filter (03):     EC,B1,BB,A7,B2,2A,C3,34

TRANS HYBRID LOSS

FREQ         loss                FREQ        loss
(Hz)         (dB)                (Hz)        (dB)
 100.        39.028              2000.       47.626
 200.        32.840              2100.       45.454
 300.        38.311              2200.       43.686
 400.        44.327              2300.       42.872
 500.        53.796              2400.       42.486
 600.        52.398              2500.       42.673
 700.        47.530              2600.       43.375
 800.        45.172              2700.       44.823
 900.        43.673              2800.       47.284
1000.        42.808              2900.       51.668
1100.        42.819              3000.       55.841
1200.        43.199              3100.       49.939
1300.        44.446              3200.       45.016
1400.         5.997              3300.       41.837
1500.        48.904              3400.       39.716
1600.        52.613              3500.       38.317
1700.        61.033              3600.       37.560
1800.        58.078              3700.       37.649
1900.        51.198              3800.       39.487

Additional B-filter delay (in seconds):  .625E-04
Bytes for B-filter delay (18):           19,19,11,19
```

Appendix H
The Batch File 'K.BAT'

```
IF EXIST *.IND DEL *.IND

PSPICE1    %1.cir   %1.out
  |          |        |
  |          |        SPICE output file
  |          SPICE input file
  SPICE program

KCONVERT          %1.out    %1.sli
  |                 |         |
  |                 |         Conversion program output
  |                 |         = SLIC input file for SICOFI program
  |                 Conversion program input
Conversion program
```

SICOFI® Test Board STUT 2060

Contents **Page**

1 Introduction

Using the SICOFI Testboard STUT 2060 facilitates measurement of the transfer functions of the SLIC in connection with the SICOFI. Via a RS 232 interface to a microprocessor programming the PBC or PIC, the SICOFI and SLIC is made possible. The SLIC circuit is placed on a separate board which can be connected through 64-pins connectors CON6 and CON7 to the testboard. This set-up aids in making the following investigations:

- testing the SLIC hardware
- verifying the programmed coefficients, which have been calculated with the SICOFI coefficients program
- speeding up evaluation of different SLICs

2 Hardware

The SICOFI Testboard can be broken down into the functional parts:

- power supply section
- clock supply section
- microprocessor section
- PBC/PIC section
- SICOFI section including SLIC Connectors CON6 and CON7, and CON5

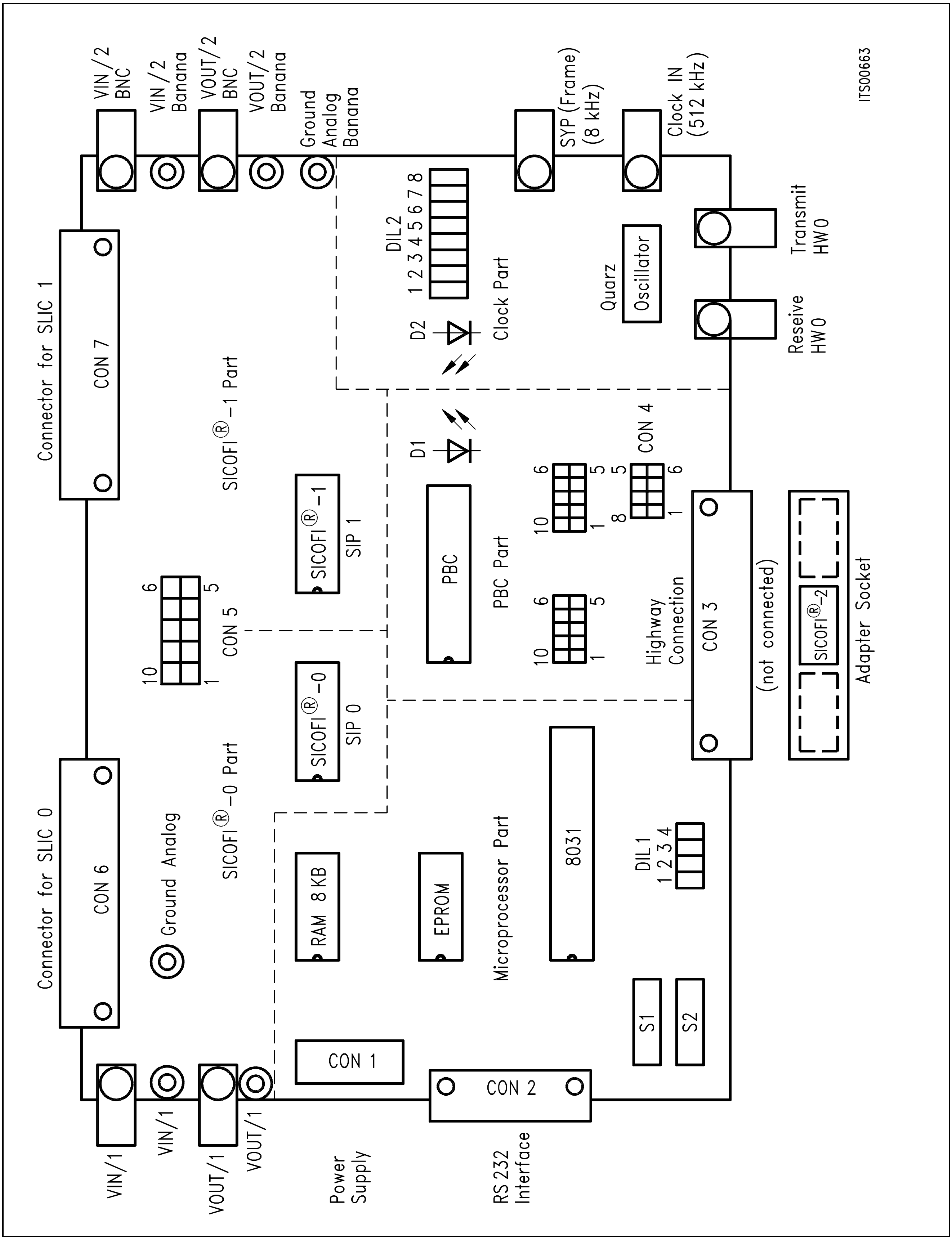


Figure 1
Floor Plan of the SICOFI® Testboard STUT 2060

2.1 Power Supply Section

The board needs an external power supply. On board there is a connector (CON 1) with the following pinning:

pin	terminal
1	+ 5 V
2	digital ground (DGND)
3	+ 12 V
4	analog ground (AGND)
5	– 48 V
6	battery ground (BGND)
7	– 5 V
8	ring ground (RGND) not connected
9	– 12 V
10	ring (NC)
11	– 70 V

2.2 Clock Supply Section

The clock supply provides several modes:

– external clock, external frame

– external clock, internal frame

– internal clock, internal frame

With the switch DIL 2 of the clock part, you can set up these 3 modes:

DIL2	ON	OFF
S1	internal clock	external clock
S2	internal frame	external frame

By switching-on S1 of DIL2 (internal clock) the LED D2 is ON. External clock may be supplied at 1.536 MHz, 2.048 MHz, 3.072 MHz, or 4.096 MHz.

DIL2	Clock 1.5 MHz	Clock 2 MHz	Clock 3 MHz	Clock 4 MHz
S3	OFF	ON	ON	ON
S4	ON	ON	OFF	ON
S5	OFF	OFF	ON	ON

When just using external clock and external frame, only DIL-switches S1 and S2 are to be set (both to position OFF). – The DIL-switches S6, S7 and S8 are not connected.

2.3 Microprocessor Section

There is a 8031 microprocessor, a 16 Kbyte EPROM, 8 Kbyte RAM and a RS232 interface on the board. The RAM is not used in this version. You can also use different types of EPROMs (8 K, 16 K, 32 K bytes). In that case you have to change a few solder straps. Further information can be found in **chapter 2.7** Solder Straps.

In the microprocessor part there are two switches S1 and S2 and a DIL-switch (DIL1). Switch S1 changes the direction receive/transmit of the RS232-interface. Switch S2 performs the hardware-reset.

The microprocessor is connected via the MAX 232-IC to the RS232-interface. With the four DIL1-switches the parity is set. The DIL1-switches S1 and S2 are switched to ON. The switches S3 and S4 have the following functions:

DIL1	OFF	ON
S3	no parity	parity
S4	odd parity	even parity

We only work with even parity and therefore both switches are in ON position.

The microprocessor program has an autobaud, which has to be to started first. We recommend to use only a transmission rate of 9600 Baud. All examples given refer to 9600 Baud.

Additional information can be found in **chapter 3**. Starting the Board.

2.4 PBC/PIC Section

The PBC or PIC has a PCM highway 0 and 1, both with highway drivers. These drivers may be optimized by using external resistors. You may connect the receive and transmit paths of highway 0 and 1 to connector CON4 (**see figure 1**) in using jumpers. This allows for a speech connection of subscriber 0 (SICOFI0 and SLIC0) to subscriber 1 (SICOFI1 and SLIC1). Via the connector CON3 you can connect the board to the older PBC board (STU 2050). The LED D1 indicates an interrupt from the PBC. In this case you have to check the clock and frame and you have to restart the system.

The SIP-lines SIP0 and SIP1 are connected to SICOFI 0 and 1. The SIP-line SIP3 is connected to the SLIC-connectors CON6 and CON7.

2.5 SICOFI® Section

There are two SICOFIs on the board. They are connected via the SLD-interface to the PBC.

If you have connected external hardware at the SIP-line in addition to the SICOFI, and there is a timing collision of these both circuits, a series resistor protects the SICOFI. In this case cut the solder strap near the SICOFI at the soldering side and connect the other solder point of pin 17 of the SICOFI (s**ee figure 4 in chapter 2.7** Solder Straps), then you have added the resistor to the circuit.

All SICOFI signaling pins are connected to the pertining SLIC connectors. On board the analog input/output line have both a banana- and a BNC-plug for measurement, and they are connected to the SLIC connectors, too.

2.5.1 SLIC Connectors CON6 and CON7 (pin-outs)

The connectors CON6 and CON7 have 64 pins.

Pin	Connection	Pin	Connection
A 1	Bridge to other SLIC board	C 1	
A 2	Bridge to other SLIC board	C 2	– 12 V
A 3	Bridge to other SLIC board	C 3	
A 4	Bridge to other SLIC board	C 4	+ 12 V
A 5	Bridge to other SLIC board	C 5	
A 6	DIR	C 6	
A 7	SCLK	C 7	Port 1.4
A 8	SIGS	C 8	Port 1.5
A 9	MCLK	C 9	Port 1.6
A 10	SYP	C 10	Port 1.7
A 11	SIP-wire	C 11	
A 12	Digital ground (DGND)	C 12	Port 0.0
A 13	+ 5 V	C 13	Port 0.1
A 14	Ring AC 65 V	C 14	Port 0.2
A 15	– 5 V	C 15	Port 0.3
A 16	RESET	C 16	Port 0.4
A 17	– 70 V	C 17	Port 0.5
A 18		C 18	Port 0.6
A 19	– 48 V	C 19	Port 0.7
A 20	SIP3	C 20	
A 21	SO1	C 21	SA
A 22	SO2	C 22	SB
A 23	SO3	C 23	SC
A 24	SI1	C 24	SD
A 25	SI2	C 25	
A 26	SI3	C 26	
A 27		C 27	
A 28	Analog ground (AGND)	C 28	
A 29	VIN (SICOFI input)	C 29	
A 30	Analog ground (AGND)	C 30	
A 31	VOUT (SICOFI output)	C 31	
A 32	Analog ground (AGND)	C 32	

2.5.2 Connector CON5

The ports 1.4 ... 1.7 of the microprocessor are used as inputs. Ports 0.0 ... 0.7 are switched by the microprocessor via a latch and may be programmed in bidirectional mode. The addresses of the latch range from 32 K to 64 K. If you want to use these 12 ports you have to modify the EPROM and write some new routines for the program.

With the connector CON5 you can cut the connection (no jumper) or set the connection (set jumper) between pins A1 ... A5 of SLIC-connectors CON6 and CON7.

Bridge	Jumper
A 1	1 - 10
A 2	2 - 9
A 3	3 - 8
A 4	4 - 7
A 5	5 - 6

Via this connection you may send signals from one SLIC-board to the other. In this case you need the external hardware only on a single SLIC-board. For programming external SLIC hardware you may use SIP-line 3.

2.5.3 SICOFI®-2 Adaptor

There is also an adaptor available which fits into the SICOFI sockets SIP0 and SIP1 to connect a SICOFI-2.

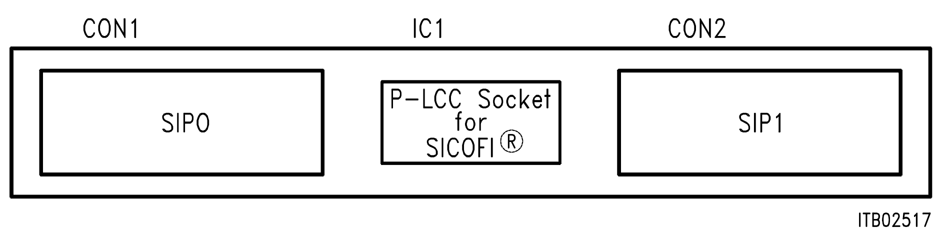


Figure 2
SICOFI®-2 Adaptor

2.6 Solder Straps for EPROM and SICOFI®

On the board at the soldering side there are several solder straps. These lead to the EPROM pins 26 and 27 and to the SICOFI pins 3 and 5. The EPROM type is set with solder straps.

EPROM	Pin 26	Pin 27
8 Kbyte	+ 5 V	+ 5 V
16 Kbyte	A13	+ 5 V
32 Kbyte	A13	A14

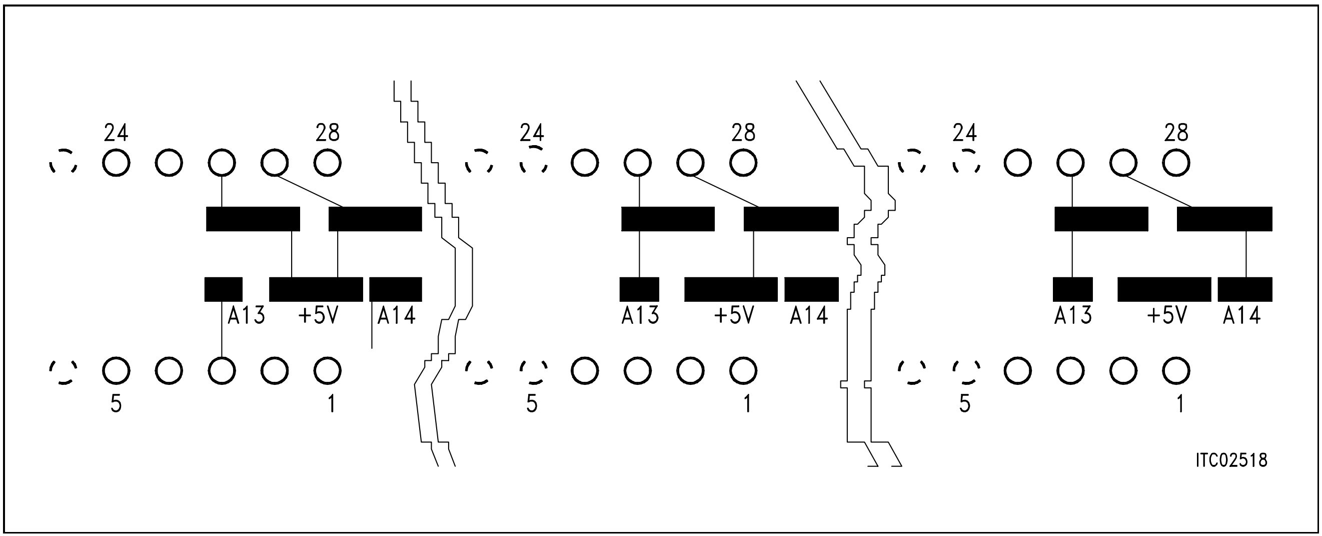


Figure 3

Solder straps underneath the EPROM to set the EPROM: Left 8 K EPROM (2764), middle 16 K EPROM (27128), right 32 K EPROM (27256)

With version 3.1 of the SICOFI you may connect analog and digital ground with a solder strap between pins 3 and 5 of the SICOFI. The solder straps for the resistor in the SIP-line are close to the SICOFI (**see figure 4**).

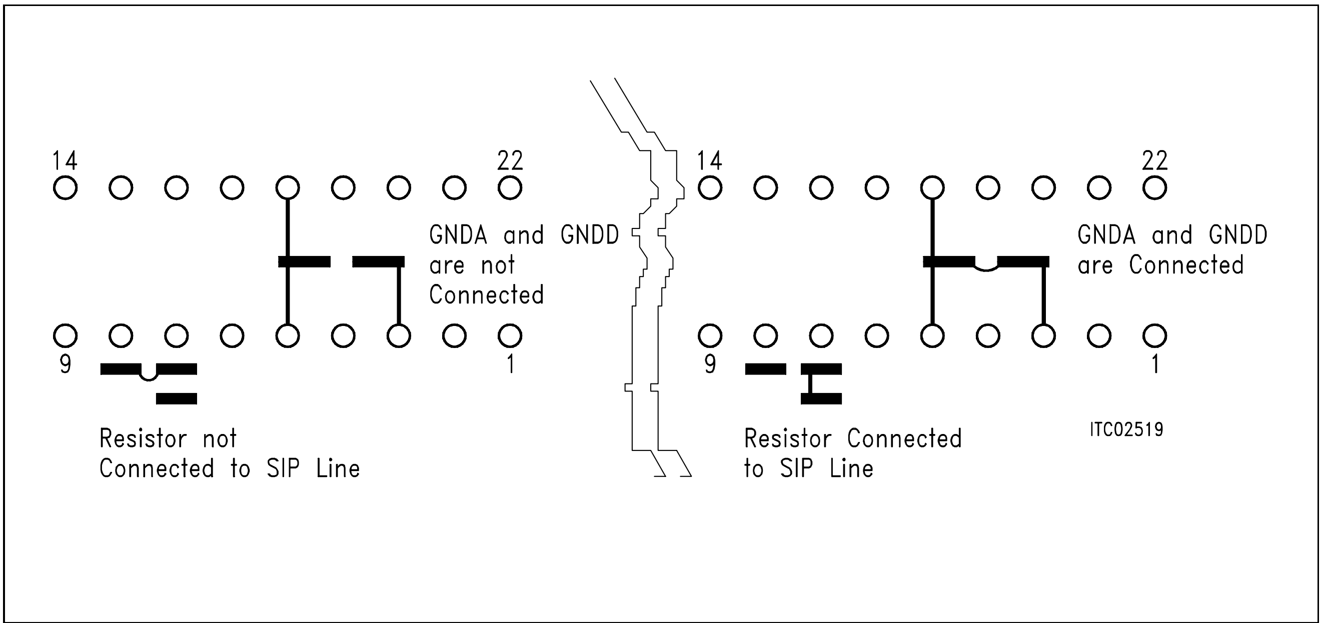


Figure 4

Solder straps near the SICOFI for ground connection and protection resistor insertion. Left: analog and digital ground not connected, resistor not inserted, right: analog and digital ground connected, resistor inserted.

2.7 Connecting SICOFI® Testboard to PCM4

For setting up a measurement system with the Wandel & Goltermann PCM4 you have access to following BNC-plugs:

– CLOCK IN
– FRAME OUT – SYP IN
– HIGHWAY 0 TRANSMIT
– HIGHWAY 0 RECEIVE
– SICOFI IN 1/2
– SICOFI OUT 1/2

The SICOFI input, output and the analog ground also have a banana-plug.
It is possible to set up the system in two different timing modes. In the first mode the PCM4 (Master) sends FRAME and CLOCK signals to the SICOFI testboard.

The alternative mode uses the internal CLOCK and FRAME of the SICOFI board (Master) to synchronize the PCM4.

The PCM4 (Wandel & Goltermann) is the measurements system to measure the transfer functions from an analog line card. The system has at the digital side a PCM input and output and on the analog side a 4-wire and a 2-wire in- and output. It delivers or needs the clocks to or from the test object. When the system gets the clocks it is the slave and at the other way it is the master. Both ways are possible with our SICOFI testboard (STUT 2060). The SICOFI testboard is able to generate the clock signals (frame and SCLK) or gets them from the PCM4.

Clock generation on the testboard

The DIP-switches on the testboard are set to
DIL 2.1 closed
DIL 2.2 closed
DIL 2.3 closed
DIL 2.4 closed
DIL 2.5 open

The PCM4 input for the frame is the plug 64 (external frame) on the backplane. Additionally a bridge from frame trigger output (plug 61) to external frame (plug 63) is set. The BNC2 plug (PCM highway input of testboard) has to be connected to the output of the PCM highway of the PCM4 and the input of the PCM-highway of PCM4 with the BNC1 of the SICOFI testboard.

The analog front end is connected with the analog input or output of the PCM4.

The phase shift for the PBC is PSR = 36.

Clock generation in the PCM4

The DIP-switches on the testboard are set to
DIL 2.1 open
DIL 2.2 open
DIL 2.3 closed
DIL 2.4 closed
DIL 2.5 open

The PCM4 output for the frame is the plug 61 (frame trigger output) on the backplane. Additionally a bridge from frame trigger output (plug 61) to external frame (plug 63) is set. The BNC2 plug (PCM highway input) has to be connected to the output of the PCM highway of the PCM4 and the input of the PCM-highway of PCM4 with the BNC1 of the SICOFI testboard.

The analog front end is connected with the analog input or output of the PCM4.

The phase shift for the PBC is in this case PSR = 2D.

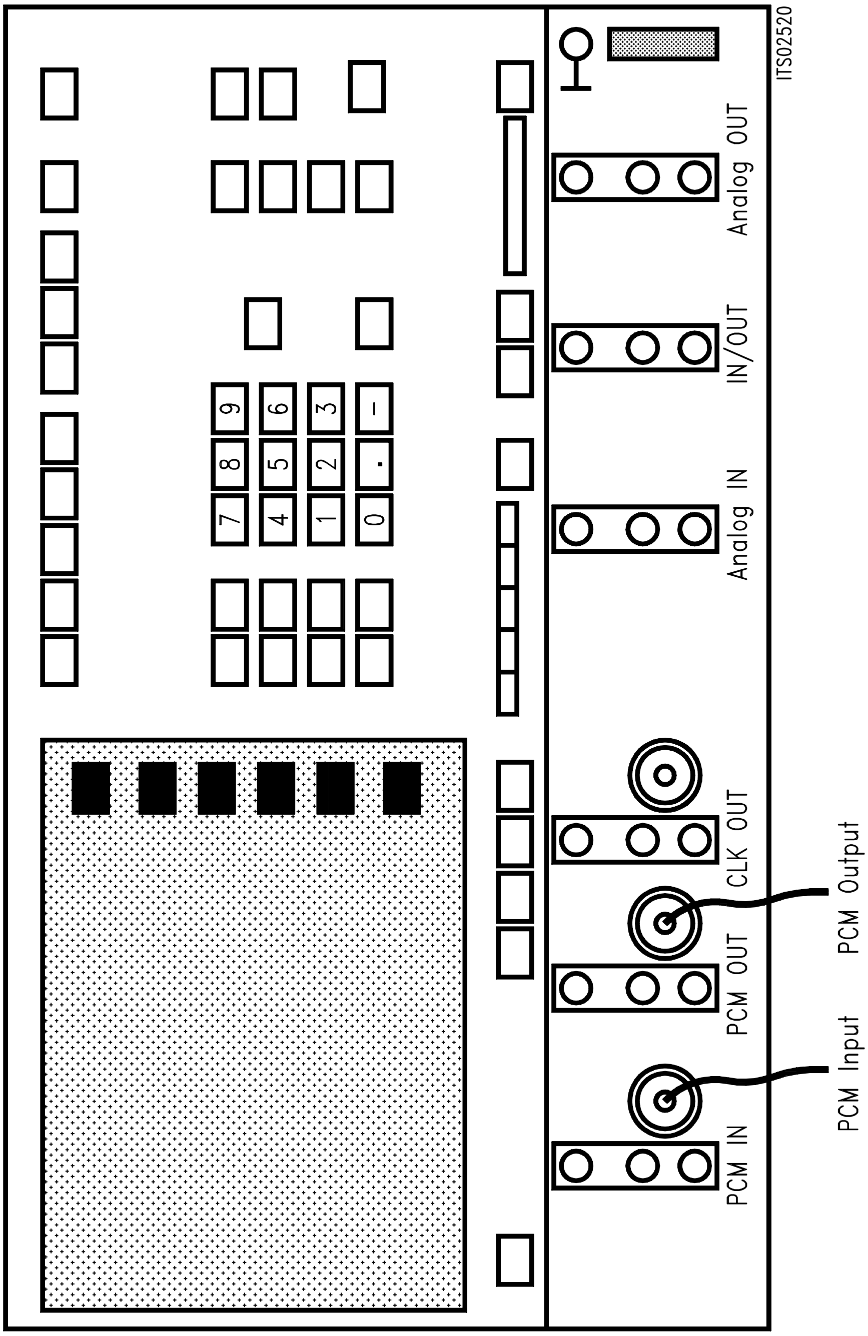


Figure 5
PCM4 Front View

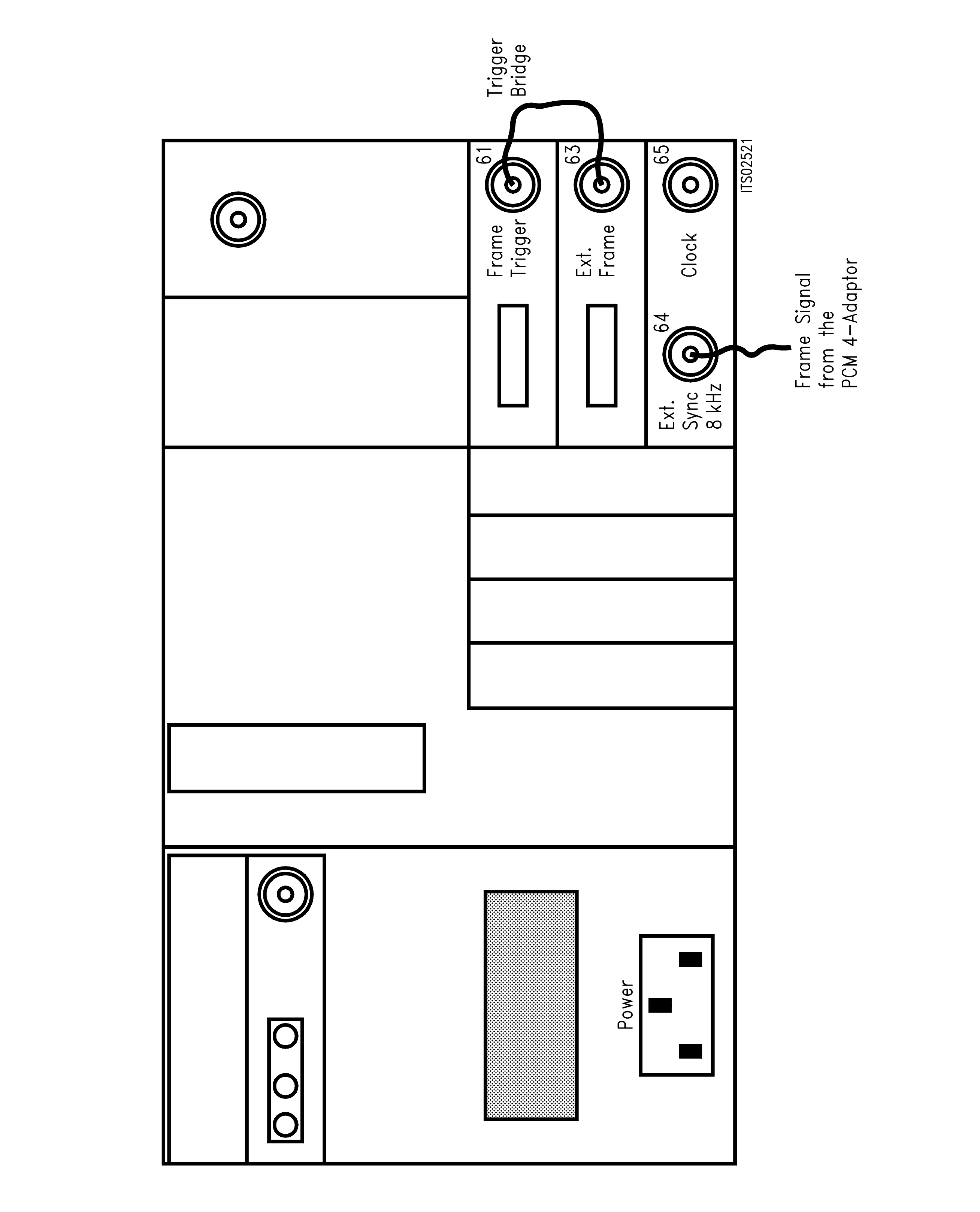


Figure 6
PCM4 Rear View

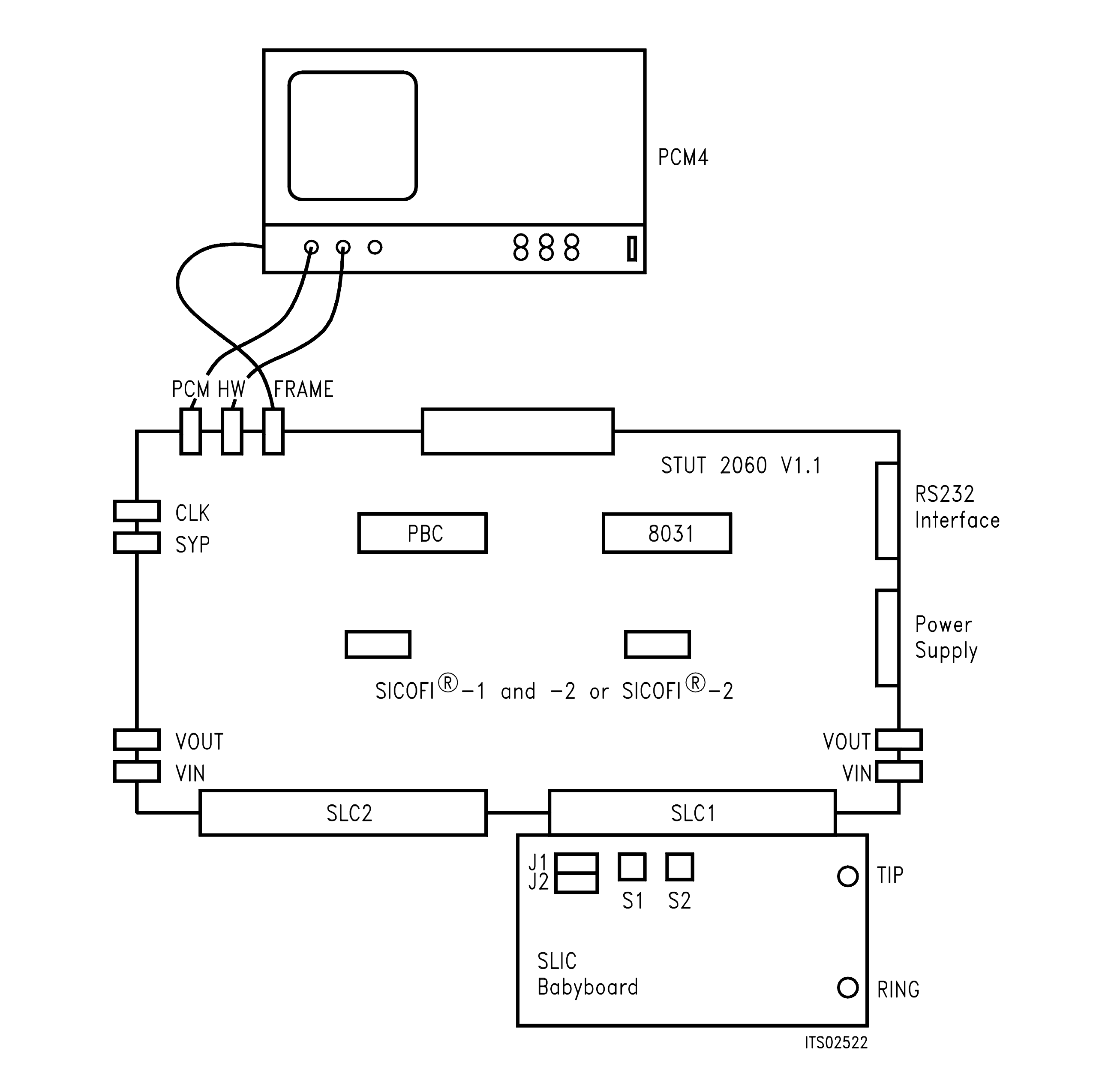


Figure 7
SICOFI® Measurement Set-Up

Required hardware for a measurement set-up:

1 PC IBM AT or compatible
1 PCM4 (Measuring set of Wandel & Goltermann)
1 SICOFI Testboard STUT 2060
1 SLIC Babyboard

2.8 The PCM4 Programming

The PCM4 has to be programmed as following:

PCM interface	2Mbit/s
Digital loop	open
Time-slot assignment	32 time slots
CRC 4 frame	out
Code	NRZ (receiver and transmitter)
Output impedance	75 Ω unsymmetrical
Clock	internal 2048 kHz, when PCM4 is master
	external 8 kHz, when PCM4 is slave
Input impedance	> 3 kΩ
Words	standard
Transmit signal	in the addressed channel
Input	no mistake
Law	A- or μ-law
NF-input and -output	1
Level	in dBm0
Two wire (D-D)	open
Digital channel no.	time channel
PCM highway output	channel 1
PCM highway input	channel 2

3 Starting the Board

The board is started in the following way:

– Set the DIL-switches in the right position (**see chapter 2.x**)
– Connect the transmit and receive highways to the PCM4
– Plug the external CLOCK and FRAME (SYP) (if used)
– Connect the RS232 interface to your computer
– Provide power supply via the power supply connector CON1
– Plug your SLIC to the connectors CON6 or CON7
– Use a terminal or a personal computer with a transfer program (9600 Baud, even parity)
– Switch ON the power supply
– Press the <BLANK> key at your computer (terminal) keyboard to start the autobaud
  After this your computer(terminal) shows the title screen:

```
                    SIEMENS

      MUENCHEN    BALANSTR. 73       BAUELEMENTE

      PPPPP       BBBBB       CCCC
      P    P      B    B      C    C
      P    P      B    B      C
      PPPPP       BBBBB       C
      P           B    B      C
      P           B    B      C    C
      P           BBBBB       CCCC

              THE KEY TO DIGITAL
            COMMUNICATIONS SYSTEMS

    SYNTAX OF AN INPUT-LINE
    WRITE: NAME = HEXDATA CR
    READ: NAME CR
    I-FRAME: RI PBC-COMMAND, DATA, DATA, ... CR
    RR-FR.: RR CR
    RQ-FR.: RQ CR
  *
```

– Program the PBC, SICOFI and SLIC
  The coefficients are stored in a file (XXX.byt) generated by the SICOFI coefficients program (see the succeeding section).

4 Programming the Board

You can program the PBC, SICOFI, and SLIC via the RS232-interface to a microprocessor. Following commands are possible:

PSR = 2D	phase 7 for PBC
CAM00 = 41	receive CHA, SIP 0, time slot 1, highway 0
CAM20 = 40	transmit CHA, SIP 0, time slot 1, highway 0
CAM01 = 41	receive CHA, SIP 1, time slot 1, highway 0
CAM21 = 40	transmit CHA, SIP 1, time slot 1, highway 0
CIW0 = 26, F4, 80	SICOFI SIP 0, Power up, all filters OFF
CIW0 = 26, F4, 78	SICOFI SIP 0, Power up, all filters ON
CIW1 = 26, F4, 80	SICOFI SIP 1, Power up, all filters OFF
SIG0 = C0	signaling byte to program SICOFI at SIP0

In the following the commands are treated in detail.

4.1 Command PSR (Phase Shift Register)

The PSR is used to shift the clock on the PCM-highways relative to the synchronization pulse (SYP). By this way different delays in a system are compensated for. The shifted clock can be used separately for transmit and receive direction and is the same on highway 0 and 1. PSR can only be written; after reset it is 00_H.

	7	6	5	4	3	2	1	0
PSR-byte	X	X	X-Shift			R-Shift		

X-shift: clock shift on transmit highway 0 and 1, value 0 ... 7
R-shift: clock shift on receive highway 0 and 1, value 0 ... 7
X: do not care

Correspondence between the programmable values of X-shift and R-shift and the clock shift on the highway is as follows:

X-Shift or R-Shift	Clock Shift
0 0 0	2
0 0 1	3
0 1 0	4
0 1 1	5

X-Shift or R-Shift	Clock Shift
1 0 0	6
1 0 1	7
1 1 0	0
1 1 1	1

For example:
If the first time slot of a frame in both directions (transmit and receive) should start at the same time as the SYP signal you have to write the value 36_H in the PSR (**see table**).

4.2 Command CAM (Contents Addressable Memory)

A connection between subscriber and PCM-Highway is set up by programming the proper CAM-register.

CAM00 =

MS1	MS0	Time Slots 0 ... 63

→ SIP-line 0 ... 7

→ 0 channel A, receive direction
1 channel B, receive direction
2 channel A, transmit direction
3 channel B, transmit direction

MS1	MS2	
1	1	no transfer
1	0	normal transfer, highway 1
0	1	normal transfer, highway 0
0	0	µP-transfer

You have to write the following value into the lower 6 bits of the CAM-register:

Desired	Input value in the				
PCM-Time-Slot	**Clock Shift**	**PSR (X-Shift or R-Shift)**	**Transmit CAM**	**Receive CAM**	**Common Channel Register**
N	0	6	N – 2	N	N – 1
N	1	7	N – 1, N – 2*	N	N – 1
N	2	0	N – 1	N	N
N	3	1	N – 1	N + 1, N*	N
N	4	2	N – 1	N + 1	N
N	5	3	N – 1	N + 1	N
N	6	4	N – 1	N + 1	N
N	7	5	N – 1	N + 1	N

* PCM-highway 0, 1

For example:
channel A, SIP-line 4, transmit highway 0, clock shift 5
CAM24 = $4E_H$

channel B, SIP-line 7, receive highway 1, clock shift 7
CAM17 = 89_H

4.3 Command SIGS (Signaling Strobe)

The Signaling Strobe is a programmable frame-synchronous signal, which you get at the SIGS-pin (A8) of connectors CON6 and CON7. With this signal you can drive an expansion logic for the SICOFI. As the PBC sends 16 signaling bits, and the SICOFI uses only 10, with an active SIGS the remaining 6 bits are switched to the expansion logic. The active SIGS-signal is programmed in the Signaling Configuration Register (SCR). You can write and read it; after Reset it is 00_H and not active.

	7							0
SCR	D/RS	C/XS	B/AS	A/BS	SS	FPC	X	X

The SS-bit (Strobe Select):

SS = 0: Strobe via channel A and/or B

	7							0
SCR	RS	XS	AS	BS	0	X	X	X

RS – Receive Strobe
XS – Transmit Strobe
AS – Channel A Strobe
BS – Channel B Strobe

The strobe is active (high), if RS and/or XS together with AS and/or BS are set.
The next table shows the strobe as a function of the bits RS, XS, AS and BS. '1' means high level (active).

				Transmit		Receive	
RS	**XS**	**AS**	**BS**	**ChA**	**ChB**	**ChA**	**ChB**
0	0	X	X	0	0	0	0
1	0	1	0	0	0	1	0
1	0	0	1	0	0	0	1
1	0	1	1	0	0	1	1
0	1	1	0	1	0	0	0
0	1	0	1	0	1	0	0
0	1	1	1	1	1	0	0
1	1	1	0	1	0	1	0
1	1	0	1	0	1	0	1
1	1	1	1	1	1	1	1
X	X	0	0	0	0	0	0

SS = 1: strobe via bits of the signaling byte

SCR (bit 7 … bit 0)

7							0
D	C	B	A	1	FPC	X	X

FPC = 1 The strobe covers 6 bits of the signaling byte. With bit 0 the strobe is always high in receive and transmit direction.

FPC = 0 The strobe covers 9 bits of the signaling byte. The strobe is always active in transmit direction with bits 2 ... 0 and in receive direction with bits 1 ... 0.

A, B, C, D set the other bit-positions, at which the strobe is active. The strobe is active in receive direction with the A-, B-, C-, D-bits being set to ’1’ in the SCR-register. The strobe is low in transmit direction with the A-, B-, C-, D-bits being set to ’1’ in the SCR-register.

Strobe

The strobe is used to drive an external Tri-State-Driver, which sends some bits to the SIP-line. You have to continue programming the strobe in transmit direction to avoid overlapping of both transmitters. This is valid for the following combination:

A	**B**	**C**	**D**
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1

4.4 Control Byte for CIW Command

The following description of the programming bytes is only valid for the SICOFI PEB 2060.

If the SICOFI-2 adaptor is used, you have to program the corresponding bytes for the SICOFI-2 (PEB 2260).

There are three classes of the CIW command for the SICOFI which are defined by bits 2 and 3 in each control byte:

– NOP NORMAL OPERATION
  no status modification or data exchange
  control byte: bit 3 = 1
  bit 2 = 1

– SOP STATUS OPERATION
  contains information about the SICOFI status and use of signaling expansion logic
  control byte: bit 3 = 0
  bit 2 = 1

– COP COEFFICIENT OPERATION
  contains information about data exchange
  control byte: bit 3 = X
  bit 2 = 0

SOP and COP contain additional address information which is valid if 2 SICOFIs are connected to one and the same PBC port.

4.4.1 SOP Command

If the SICOFI status has to be changed, a status operation byte is transferred containing the following information:

7						0
AD	R/W	PU	TR	0	1	LSEL

AD Address information which is relevant if 2 SICOFIs are connected to one and the same PBC port. Here: always AD = 0

R/W Read/write information
Enables reading from the SICOFI or writing information to the SICOFI (read = 1, write = 0)

PU Power-up/power-down
PU = 1 Power-up (operating)
PU = 0 Power-down (standby)

TR Three-party conferencing
If TR = 1, the received voice bytes of channel A and B are added

LSEL Length select
Defines the number of the subsequent data bytes

4.4.1.1 SOP Write

If the SICOFI status has to be defined initially or changed, the SOP command looks like

7						0
AD	0	PU	TR	0	1	LSEL

and the subsequent configuration bytes are written into one or both configuration registers CR1, CR2.
In this case, the meaning of LSEL is:

- 0 0 status setting is completed (no bytes following)
- 1 1 one byte will follow and is stored in CR1
- 1 0 two bytes will follow and are stored in CR2 and CR1
- 0 1 not used

Corresponding to the configuration bytes transmitted, the information contained in the configuration registers is

	7							0
CR1	DB	RZ	RX	RR	RG	TM	TM	TM

where

- DB disable B filter (DB = 1), restore B filter (DB = 0)
- RZ disable Z filter (RZ = 0), restore B filter (RZ = 1)
- RX disable X filter (RX = 0), restore B filter (RX = 1)
- RR disable R filter (RR = 0), restore B filter (RR = 1)
- RG disable G filter (RG = 0), restore B filter (RG = 1)

Test Modes	**DB**	**RZ**	**RX**	**RR**	**RG**	**TM**	**TM**	**TM**
No test mode	X	X	X	X	X	0	0	0
analog loop back via Z-filter	X	X	X	X	X	0	0	1
disable high pass	X	X	X	X	X	0	1	0
cut off receive path (HP active)	X	X	X	X	X	0	1	1
Not used						1	0	0
Not used						1	0	1
Digital loop back via B-filter	X	X	X	X	X	1	1	0
Digital loop back via PCM-reg.	X	X	X	X	X	1	1	1

and

	7							0
CR2	D	C	B	A	EL	AM	µ/A	PCS

where

- D signaling pin SD is input (D = 1) or output (D = 0)
- C signaling pin SC is input (C = 1) or output (C = 0)
- B signaling pin SB is input (B = 1) or output (B = 0)
- A signaling pin SA is input (A = 1) or output (A = 0)
- EL signaling expansion logic connected (EL = 1) or not connected (EL = 0)
- AM Address Mode
  one SICOFI: AM = 1
  two SICOFIs: AM = 0; SA is input automatically
- µ/A µ-law: µ/A = 1 A-law: µ/A = 0
- PCS Programmed B-filter coefficients (PCS = 0) or fixed coefficients for B-filter (PCS = 1)

Note: The power-on reset or a hardware reset via RS pin resets all CR1 bits to 0 and sets all CR2 bits to 1.

4.4.1.2 SOP Read

If the SICOFI status has to be evaluated, using the SOP command

7							0
AD	1	PU	TR	0	1	1	0

the contents OF CR2 and CR1 is read back to SIP. The meaning of the SOP bits is as described in the SOP write section.

4.4.2 COP Command

With a COP command, programmable filter coefficients can be written into or read from the coefficients RAM. With the following bytes you can write into the RAM:

	SICOFI A	SICOFI B
B-filter part 1	03	83
B-filter part 2	0B	8B
B-filter delay	18	98
Z-filter	13	93
X-filter	23	A3
R-filter	2B	AB
GR-/GX-filter	30	B0

4.4.3 CIW Command

The CIW command writes data in the SICOFI like filter coefficients, power-up, status of the four signaling pins, number of SICOFIs at the SIP-line.

CIW0 = 26, F4, 80

- 80 → CR1
- F4 → CR2
- 26 → SIP0

CIW1 = 13, 20, 1D, AA, 9B, CB, 2C, 13, B4

- 1D, AA, 9B, CB, 2C, 13, B4: filter coefficients
- 20 → Z-filter coefficients following
- 13 → SIP1

4.4.4 CIR Command

The CIR command reads data out of the SICOFI which have been written into the SICOFI with the CIW command.

CIR0 = 66

- 6 → COP command to read the SICOFI status
- 6 → SIP-line

You can read out the filter coefficients with the following byte:

	SICOFI A	SICOFI B
B-filter part 1	43	C3
B-filter part 2	4B	CB
B-filter delay	58	D8
Z-filter	53	D3
X-filter	63	E3
R-filter	6B	EB
GR-/GX-filter	70	F0

The coefficients are followed by the values of CR2 and CR1 register.

4.5 Command SIG

With the SIG command you can write the signaling byte. This byte is used by the signaling interface of SICOFI. It has:
3 transmit signaling inputs (SI1, SI2, SI3),
3 receive signaling outputs (SO1, SO2, SO3), and
4 signaling pins (SA, SB, SC, SD), which are individually programmable as either transmit input or receive output.
The signaling field format is generally

in transmit direction

7							0
SI1	SI2	SI3	SD	SC	SB	SA	SEL

in receive direction

7							0
SO1	SO2	SO3	SD	SC	SB	SA	SEL

where SEL is the signaling expansion bit if EL = 1 in CR2

For the 6 different cases possible, the signaling byte format at SIP is for

Receive Signaling Byte									**Transmit Signaling Byte**							
Case BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1	SO1	SO2	SO3	Y	Y	Y	Y	Y	SI1	SI2	SI3	SD	SC	SB	SA	0
2	SO1	SO2	SO3	Y	Y	Y	Y	Y	SI1	SI2	SI3	SD	SC	SB	SA	Z
3	SO1	SO2	SO3	SD	SC	SB	SA	Y	SI1	SI2	SI3	0	0	0	0	0
4	SO1	SO2	SO3	SD	SC	SB	SA	Y	SI1	SI2	SI3	Z	Z	Z	Z	Z
5 A SICOFI																
	SO1	SO2	SO3	Y	Y	Y	Y	Y	SI1	SI2	SI3	SD	Z	Z	Z	Z
B SICOFI																
	Y	Y	Y	Y	SO1	SO2	SO3	Y	Z	Z	Z	Z	SI1	SI2	SI3	SD
6 A SICOFI																
	SO1	SO2	SO3	SD	Y	Y	Y	Y	SI1	SI2	SI3	0	Z	Z	Z	Z
B SICOFI																
	Y	Y	Y	Y	SO1	SO2	SO3	SD	Z	Z	Z	Z	SI1	SI2	SI3	0

Z High-impedance state
Y Do not care

Cases:

1. A single SICOFI connected to a single PBC port; EL = 0 (no expansion logic): SA, SB, SC, SD programmed as transmit signaling inputs

2. A single SICOFI; EL = 1 (expansion logic provided; SA, SB, SC, SD programmed as in case 1).

3. A single SICOFI; EL = 0; SA, SB, SC, SD programmed as receive signaling outputs

4. A single SICOFI; EL = 1; SA, SB, SC, SD programmed as in case 3.

5. Two SICOFIs connected to one and the same PBC port; SD programmed as transmit signaling input.

6. Two SICOFIs, SD programmed as receive signaling output. If two SICOFIs are connected to one and the same PBC port, no expansion logic is provided. SA is programmed as input automatically and defines the addressed SICOFI:

SA = 0: A SICOFI
SA = 1: B SICOFI

Example:

SIG0 = C0
C0 → signaling byte
SIG0 → SIP-line

4.6 Microprocessor Ports

If you want to use the ports of the microprocessor, than you have to extend the microprocessor software and to change the EPROM.

4.7 Program Examples

a) If you want to do measurements with a PCM4 from 'Wandel & Goltermann' you may program the following example:

The PCM4 is the master. It sends the data in time slot 1 and receives from time slot 2. The SLIC is a HARRIS HC 5502A. Due to the clock shift of the PCM4 (– 1 bit) we program the clock shift with 7 to the preceding time slot. In this case:

PSR = 2D	phase 7 for PBC
CAM00 = 41	receive ChA, SIP0, time slot 1, hw0
CAM20 = 40	transmit ChA, SIP0, time slot 1, hw0
CIW0 = 26, F4, 80	SICOFI power up, all filters off
CIW0 = 13, 20, DA, CA, 2B, 23, 41, C2, 2B	Z-filter
CIW0 = 23, 50, C8, B5, 49, C2, 21, 04, 90	X-filter
CIW0 = 2B, C0, C8, 96, C2, CA, B4, 01, 1D	R-filter
CIW0 = 03, C4, 25, 13, 3D, 6B, A9, BC, BB	B-filter part 1
CIW0 = 0B, 00, 36, D2, C2, B6, 41, 74, 2C	B-filter part 2
CIW0 = 18, 19, 19, 11, 19	B-filter delay
CIW0 = 30, 41, B0, 20, 92	GR-/GX-filter
SIG0 = C0	SLIC Power up, conversation
CIW0 = 26, F4, 78	SICOFI power up, all filters on

b) The board is the master. The PCM4 sends the data in time slot 1 and receives the data from time slot 2. The SLIC is a HARRIS HC 5502A. You have to connect the BNC-plug No. 64 of the PCM4 (external clock) to the Frame-out plug (Clock section). The parameter 3 of the PCM4 (digital generator) is programmed with 33 (external clock (8 kHz)). The shifted clock is exactly 0. In this case we have to program:

PSR = 36	phase 0 for PBC
CAM00 = 41	receive ChA, SIP0, time slot 1, hw0
CAM20 = 40	transmit ChA, SIP0, time slot 2, hw0
CIW0 = 26, F4, 80	SICOFI power up, all filters OFF
CIW0 = 13, 20, DA, CA, 2B, 23, 41, C2, 2B	Z-filter
CIW0 = 23, 50, C8, B5, 49, C2, 21, 04, 90	X-filter
CIW0 = 2B, C0, C8, 96, C2, CA, B4, 01, 1D	R-filter
CIW0 = 03, C4, 25, 13, 3D, 6B, A9, BC, BB	B-filter part 1
CIW0 = 0B, 00, 36, D2, C2, B6, 41, 74, 2C	B-filter part 2
CIW0 = 18, 19, 19, 11, 19	B-filter delay
CIW0 = 30, 41, B0, 20, 92	GR-/GX-filter
SIG0 = C0	SLIC Power-up, conversation
CIW0 = 26, F4, 78	SICOFI power-up, all filters ON

c) Example for communication between SICOFI at SIP0 and electronic-SLIC (HARRIS HC 5502A) and between SICOFI at SIP1 and transformer-SLIC.

CAM01 = 82	receive ChA, SIP1, time slot 1, hw1
CAM21 = 81	transmit ChA, SIP1, time slot 2, hw1
CIW0 = 26, F4, 80	
CIW0 = 13, 20, 1D, AA, 9B, CB, 2C, 13, B4	
CIW0 = 23, 50, 2B, AE, B1, 24, B2, 02, 42	
CIW0 = 2B, 50, 9B, 26, 32, A8, 32, 1B, 22	(TRAFO-SLIC)
CIW0 = 03, 91, 22, 39, 02, 2B, C3, 22, C1	
CIW0 = 0B, 00, 2A, 02, BB, 38, 12, BA, 21	
CIW0 = 18, 19, 19, 11, 19	
CIW0 = 30, 31, 2A, 10, 33	
CIW0 = 26, F4, 78	
CAM00 = 83	receive ChA, SIP0, time slot 2, hw1
CAM20 = 80	transmit ChA, SIP0, time slot 1, hw1
CIW0 = 26, F4, 80	
CIW0 = 13, 20, DA, CA, 2B, 23, 41, C2, 2B	
CIW0 = 23, 50, C8, B5, 49, C2, 21, 04, 90	
CIW0 = 2B, C0, C8, 96, C2, CA, B4, 01, 1D	(HARRIS-SLIC HC 5502A)
CIW0 = 03, C4, 25, 13, 3D, 6B, A9, BC, BB	
CIW0 = 0B, 00, 36, D2, C2, B6, 41, 74, 2C	
CIW0 = 18, 19, 19, 11, 19	
CIW0 = 30, 41, B0, 20, 92	
SIG0 = C0	
CIW0 = 26, F4, 78	

4.8 Programming Differences of PEB 2060 and PEB 2260

If the SICOFI testboard is used with the SICOFI-2 adaptor the programming commands are different (refer to the SICOFI and SICOFI-2 datasheet).

The programming bytes for the different SICOFI filters remain the same with the exception of the gain programming GX and GR.

SICOFI PEB 2060:

CIW0 = 30, GR, GR, GX, GX	for GR and GX programming

SICOFI-2 PEB 2260:

CIW0 = 30, GX, GX, GX, 80, 80	for GX programming
CIW0 = 3A, GR, GR	for GR programming

If you want to use our SICOFI-SLIC programming examples please note that the programming of the signaling is only valid for the SICOFI PEB 2060. If you use the SICOFI-2 PEB 2260 the command for the signaling must be changed.

5 Appendix

5.1 List of Replaceable Parts

IC 1	TL 7702	IC 11	SAB 27128
IC 2	µP 8031	IC 12	PEB 2050
IC 3	74LS241	IC 13	74LS157
IC 4	74LS155	IC 14	74LS161
IC 5	MAX 232	IC 15	74LS04
IC 6	SAB 8282	IC 16	74LS112
IC 7	74LS157	IC 17	HM 6264
IC 8	74LS241	IC 18	PEB 2060
IC 9	74HC125	IC 19	PEB 2060
IC 10	74LS393	IC 20	74LS245

Resistors

R_1, R_3, R_4	10 kΩ
R_2	27 kΩ
R_5, R_6	3.3 kΩ

Dekade of resistors

R_{a1}, R_{a2}, R_{a3}, R_{a4}	4.7 kΩ

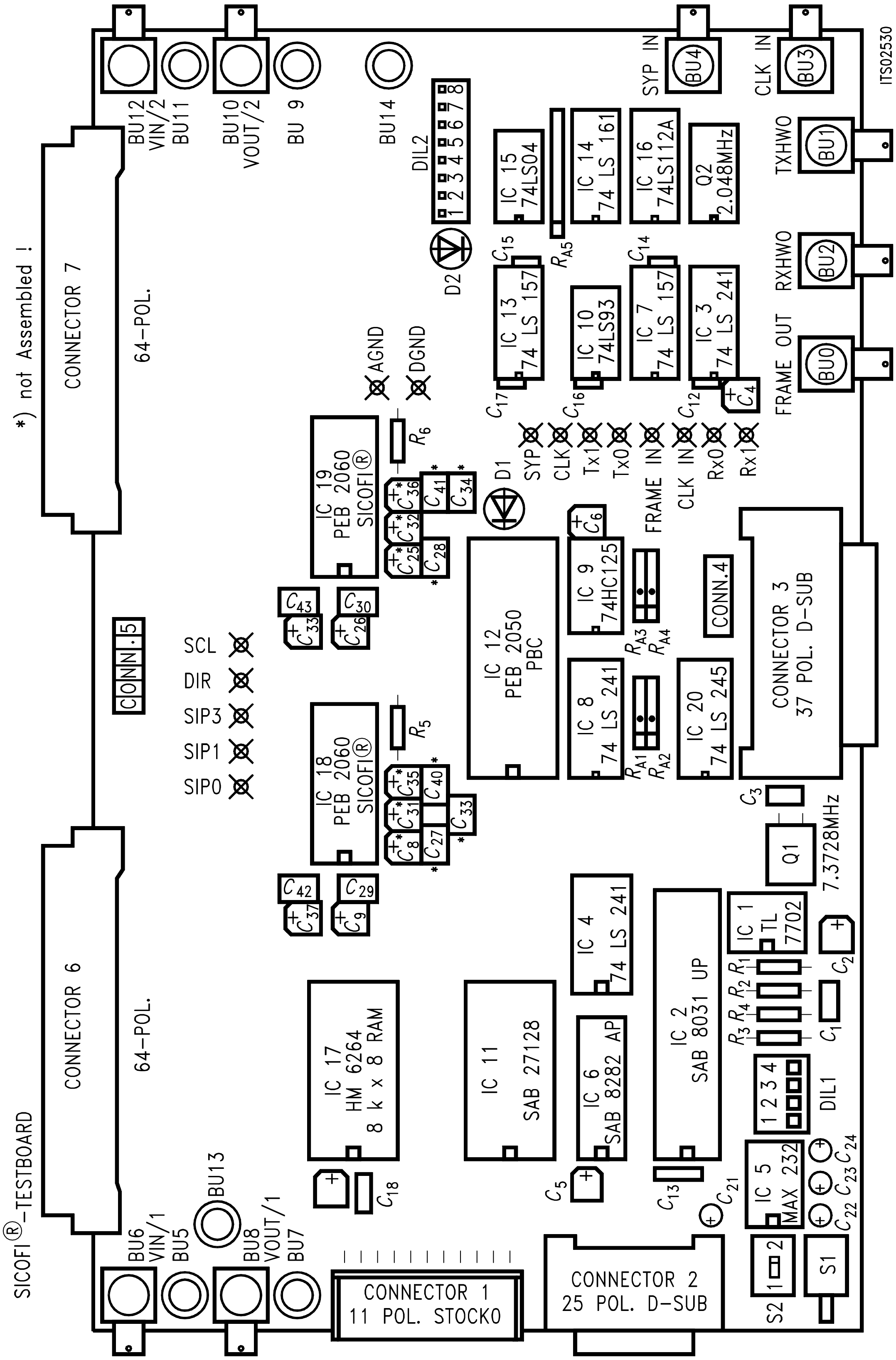
Capacitors

C_1, C_{12} ... C_{18}, C_{27}, C_{28}, C_{40}, C_{41}	100 nF
C_2, C_4, ... C_8, C_{25}, C_{35}, C_{36}	1 µF
C_3	27 pF
C_{21} ... C_{24}	22 µF

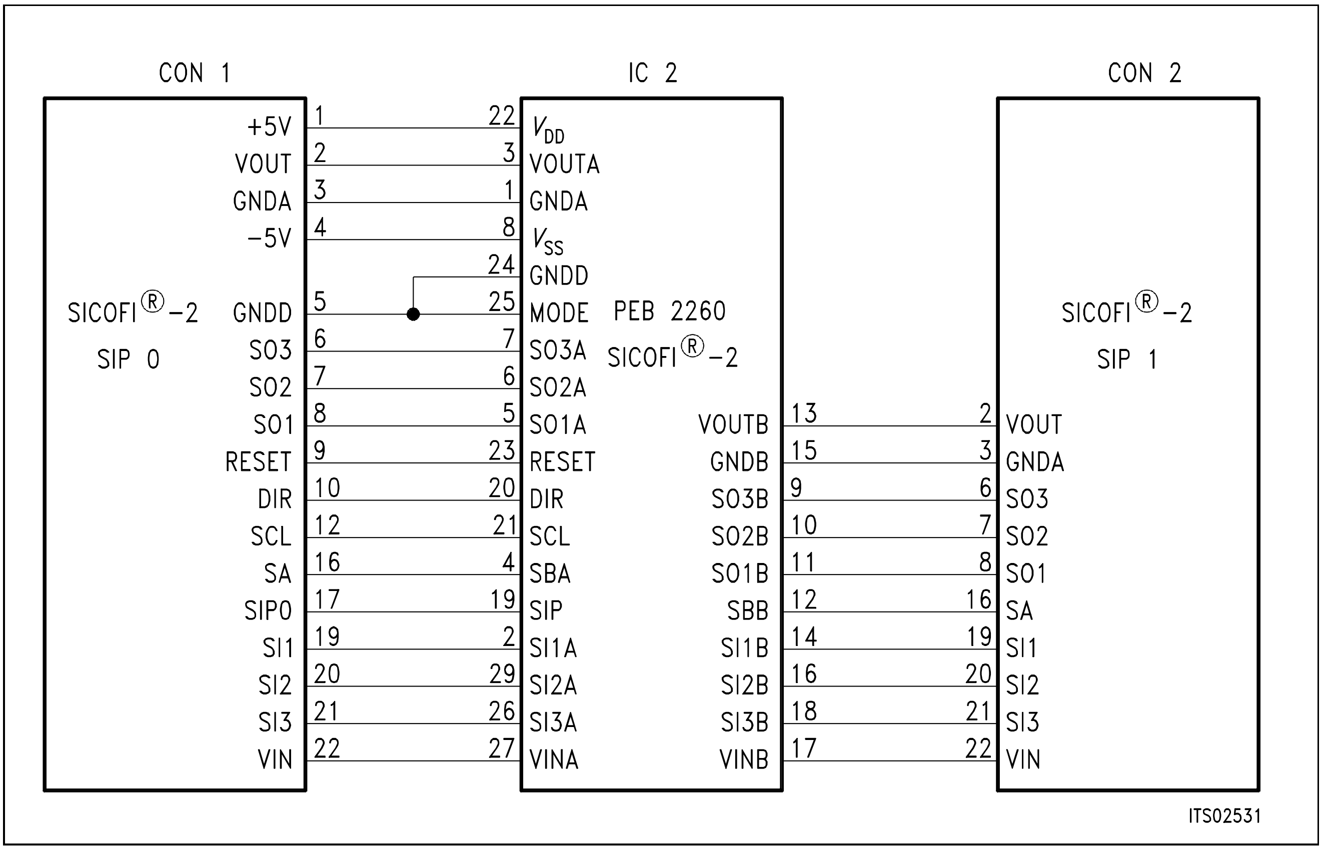
Others

S1	Reset switch
S2	dual DIL switch
DIL 1	8 pole DIL-switch
DIL 2	16 pole DIL-switch
Bu0, Bu1 ... Bu4, Bu6, Bu8, Bu10, Bu12	BNC-plugs
Bu5, Bu7, Bu9, Bu11, Bu13, Bu14	Banana plugs
CON1	power supply connector
CON2	D-SUB connector 25 pins
CON3	D-SUB connector 37 pins
CON6, CON7	64 pins connector male (or female)

5.2 Floor Plan of the SICOFI® Testboard



5.3 Circuit Diagram of the SICOFI® - 2 Adaptor



SICOFI® -2 Module for the Siemens ISDN PC Userboard (SIPB)

Contents **Page**

1 Introduction

The development of Analog Subscriber Line Cards for voice transmission in ISDN networks poses enormous efforts to the engineer in implementing the very strict requirements of the specifications to the system, thus problems that cannot be solved by experience must be settled by lengthy trial and error procedures.

The SICOFI-2 Module SIPB 5135 helps in developing the analog line card.

In an ISDN the analog line card consists of a codec filter circuit and an analog part comprising a hybrid and the line drivers and means for ringing and testing. With the SICOFI-2 integrated circuit the SICOFI-2 Module already provides a ready-to-use codec filter and interfaces to two subscriber line circuits (SLICs). Thus this board offers the outstanding advantage of enabling immediate starting with experiments on the analog line card, and to measure very comfortably various transmission functions using the PCM4 measuring device of Wandel & Goltermann.

The integration of the SICOFI-2 Module into the SIPB-system using the Menu Software renders the development and the adaptation of a voice transmission path to an ISDN to simply connecting a single board.

2 Features

- Compatible to SIPB 5000 userboard system
- Two interfaces for connecting customer specific SLIC boards
- Enables measurements of various transfer functions of the SLMA such as
  - return loss
  - gain
  - transhybrid loss
  - noise
  - gain tracking
- Same SLIC connector as on the SICOFI Testboard (STUT 2060)
- Operating in two different interfaces modes SLD or IOM-2

3 Use

The SICOFI-2 Module SIPB 5135 is developed to be used in connection with the Line Card Module SIPB 5121. If at the secondary side of the Line Card Module a PCM4 Adaptor SIPB 5311 is connected, a very useful development and testing tool for the analog line card results (**figure 1**).

Using a PCM4 of Wandel & Goltermann the following measurements are possible:

– return loss
– level in A/D- and D/A-direction
– gain tracking in A/D- and D/A-direction
– noise in A/D- and D/A-direction
– echo return loss

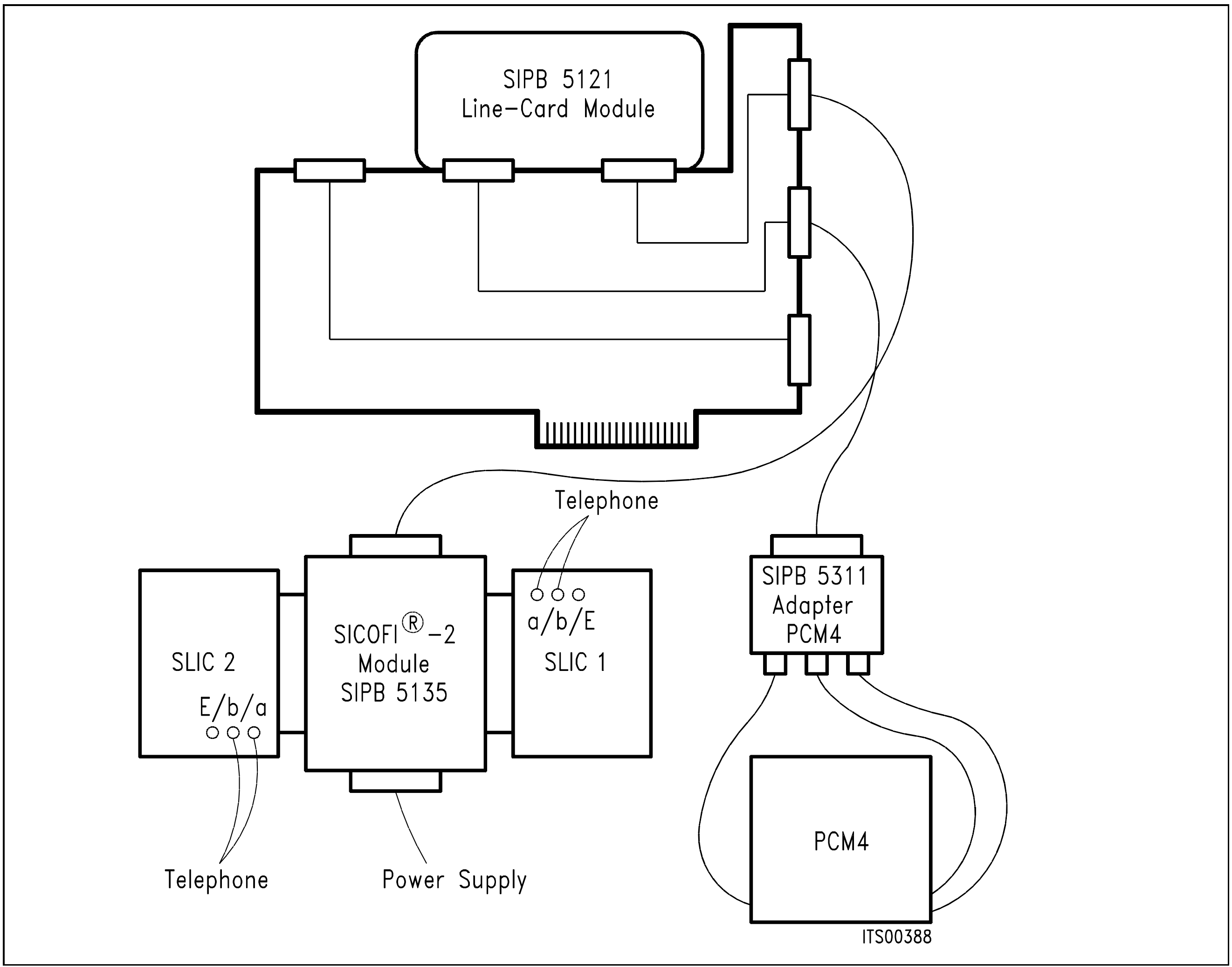


Figure 1
Measuring Set-Up

With very sensitive noise measurements power (5 V) may be supplied externally to the SICOFI-2 Board.

4 Circuitry

4.1 Block Diagram

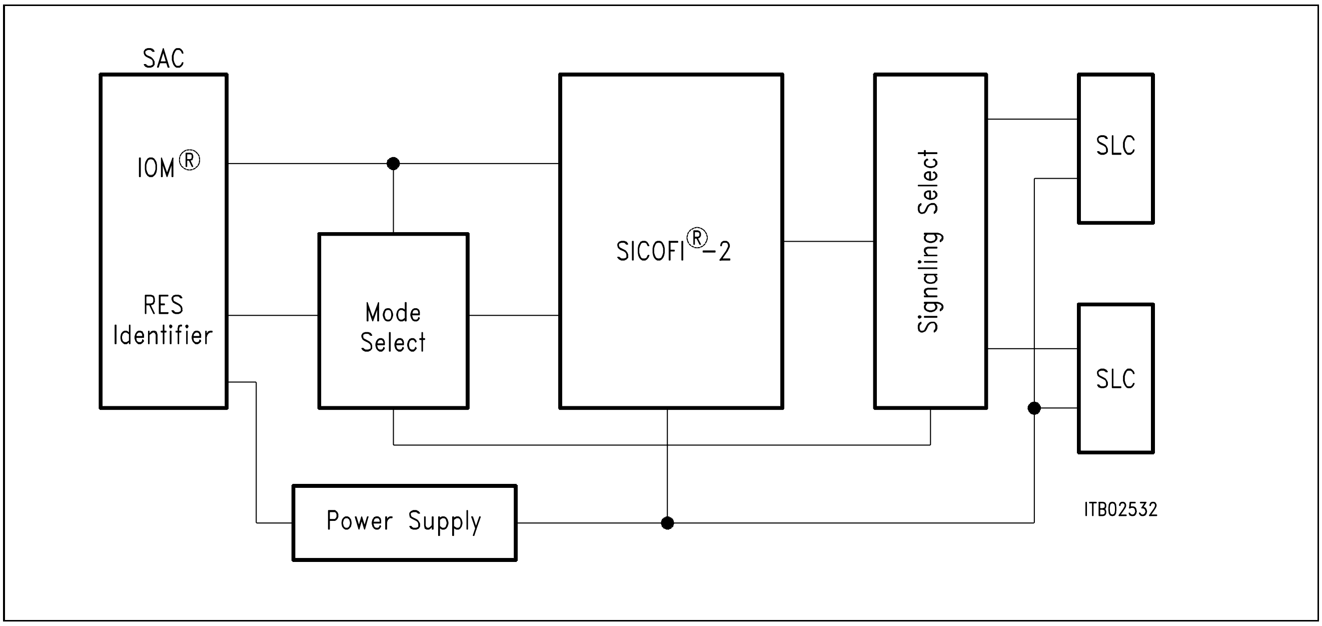


Figure 2
Block Diagram of the SICOFI® -2 Module

4.2 Connector Pin-Outs

4.2.1 Service Access Connector SAC (ST2)

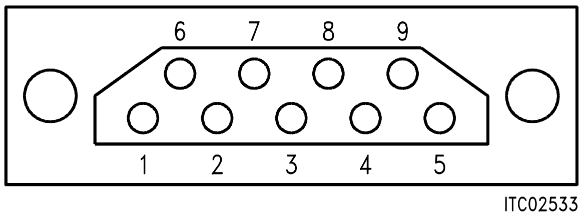


Figure 3
Service Access Connector SAC

Pin	Use	Signal
1	–	Not connected
2	O	Identifier (SLD = "0", IOM = "1")
3	I	RESET
4	O	DU (IOM mode)
	I/O	SIP4 (SLD mode)
5	I	DD (IOM mode)
	I/O	SIP0 (SLD mode)
6	I	FSC
7	I	DCL
8	I	+ 5 V
9	I	GND

4.2.2 SLIC Connector SLC (ST1, ST4)

To connect the SLICs, a 64-pin connector is used.

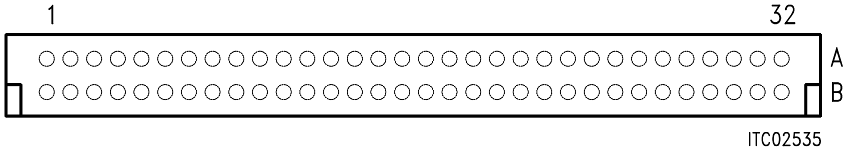


Figure 4
SLIC Connector SLC

Pin Definition and Function

Pin	Row	Use	Signal
1	A	I/O	Bridge to other SLIC connector
2	A	I/O	Bridge to other SLIC connector
3	A	I/O	Bridge to other SLIC connector
4	A	I/O	Bridge to other SLIC connector
5	A	I/O	Bridge to other SLIC connector
6	A	O	FSC
7	A	O	CLK 512 kHz
11	A	I/O	SIP4 (only in SLD – interface mode)
12	A	O	GND
13	A	O	+ 5 V
14	A	O	RING AC 65 V
15	A	O	– 5 V
16	A	O	RESET (high active)
17	A	O	– 70 V
19	A	O	– 48 V
20	A	O	SIP0 (only in SLD – interface mode)
21	A	O	SO1 (SLD) / C1 (IOM-2)
22	A	O	SO2 (SLD) / C2 (IOM-2)
23	A	O	SO3 (SLD) / C3A (IOM-2)
24	A	I	SI1 (SLD) / I1 (IOM-2)
25	A	I	SI2 (SLD) / CI1 (IOM-2)
26	A	I	SI3 (SLD) / CI2 (IOM-2)
28	A	O	GND analog
29	A	I	VIN (SICOFI analog input)
30	A	O	GND analog
31	A	O	VOUT (SICOFI analog output)
32	A	O	GND analog
2	C	O	– 12 V
4	C	O	+ 12 V
21	C	I/O	SB (SLD) / CI1 (IOM-2)
22	C	I/O	CI2 (IOM-2)

Bridges between both SLIC connectors are provided at the SICOFI-2 Module to allow for direct signaling between the SLICs. These connections are established by jumpers.

The signaling pins CI1 and CI2 are connected to pins C21 and C22 or to A25 and A26 respectively. Selection is done by DIL switch S. This selection is needed to provide additional input pins at row A when operating in the IOM-2 interface mode.

4.2.3 Power Supply Plug PSC (ST3)

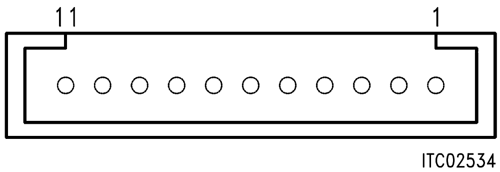


Figure 5
Power Supply Connector PSC

Pin	Function
1	+ 5 V
2	Digital Ground (DGND)
3	+ 12 V
4	Analog Ground (AGND)
5	– 48 V
6	Battery Ground (BGND)
7	– 5 V
8	Ring Ground (RGND; not used)
9	– 12 V
10	Ring signal (not used)
11	Not used

4.3 List of Replaceable Parts

Component	Type/Value
IC1	PEB 2260
IC2	74 HC 147
IC3	74 HC 4052
IC4	74 HC 4052
IC5	74 HC 4053
IC6	74 HC 4316
IC7	74 HC 4053
IC8	74 HC 93
IC9	74 HC 4053
IC10	74 HC 04
IC11	74 HC 125
IC12	74 HC 126
IC13	74 HC 00
T1, T2	BC 237A
D1, D2	1 N 4007
$R_1 \dots R_7$	10 kΩ
R_8	7 × 10 kΩ
C_1, C_2	10 µF
C_3, C_4	10 nF
C_5	100 nF
S1	10 × 1
S2 – S5	DIP 8 pol.
Relay K1	DS4E-SL2 5 V
Relay K2	DS2E-SL2 5 V

4.4 Floor Plan

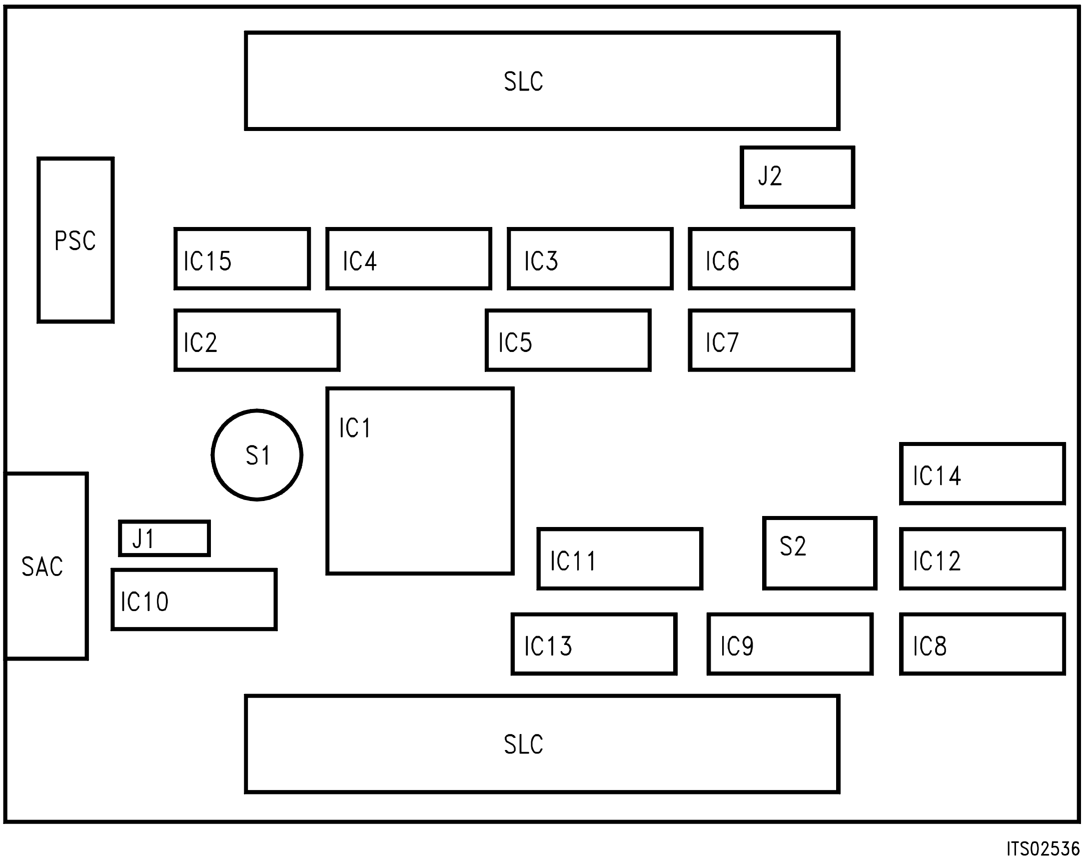


Figure 6
Floor Plan of the SICOFI®-2 Module

5 Operational Information

5.1 Configuring the SICOFI®-2 Module

Before power is applied to the SICOFI-2 Module, it has to be configured by means of switch and jumper settings for a given application.

Possible configurations of the SICOFI-2 Module are:

– selecting the interface mode (SLD- or IOM modes)
– selecting the signaling pins at the SLIC connectors SLC.

Selection of the interface mode is done by means of rotary switch S1, and of the signaling pins in using the DIP switch S2.

Switch S1

The 10-position rotary switch S1 selects the interface modes SLD or IOM. An identifier signal is transmitted to the configuration register of the Line Card Module for indicating the actual interface mode. This configuration register is readable by the Menu Software.

In the IOM mode, 9 different modes are possible. Only a single IOM mode works at a 512 kHz clock frequency (slow IOM). All other IOM modes (fast IOM) operate at 4096 MHz, and 8 different channels at the interface are selectable. All existing possibilities are summarized in the following table.

S1 Position	Interface Mode
0	SLD mode
1	IOM (DCL = 512 kHz)
2	IOM channel 0 (DCL = 4096 kHz)
3	IOM channel 1 (DCL = 4096 kHz)
4	IOM channel 2 (DCL = 4096 kHz)
5	IOM channel 3 (DCL = 4096 kHz)
6	IOM channel 4 (DCL = 4096 kHz)
7	IOM channel 5 (DCL = 4096 kHz)
8	IOM channel 6 (DCL = 4096 kHz)
9	IOM channel 7 (DCL = 4096 kHz)

5.1.1 SLD Interface Mode

In the SLD interface mode the pertining identifier signal is logical "0". The SIP-line 4 is connected to the SICOFI-2. The SIP-line 0 is connected to the SLIC connectors 1 and 2.

In the SLD interface mode the DIP- switches have no function (don’t care).

5.1.2 IOM® Interface Mode

There are two different timing modes, 512 kHz (slow IOM) and 4096 kHz (fast IOM). In both modes the identifier is logical "1".

Both bidirectional pins CI1 and CI2 of both SICOFI channels (A and B) are switchable between row A and C of the SLIC connector. This is necessary, because some SLICs have more signaling outputs at the connector row A than the SICOFI-2 board has inputs. Selection of the signaling paths is described in the following **table 1**.

DIP Switch S2

The module has four DIP-switches to select the pin assignment at the SLIC-connector. Selection is only possible in the IOM mode and affects the two bidirectional pins CI1A/B and CI2A/B of the SICOFI-2 Board.

Table 1
DIP Switch Settings for Pin Assignment of CI1A/B and CI2A/B

DIP – Switch				Pin – Assignment			
S1	S2	S3	S4	A25	A26	C21	C22
OFF	OFF	OFF	OFF	X	X	CI1	CI2
OFF	ON	OFF	ON	X	CI2	CI1	X
ON	OFF	ON	OFF	CI1	X	X	CI2
ON	ON	ON	ON	CI1	CI2	X	X

X = open, high impedance

5.2 Programming

Being in the **IOM interface mode**, the clock generator, the interface mode, and the EPIC configuration are programmed first. Then the SICOFI-2 is to follow. The corresponding track files for programming the EPIC and SICOFI-2 are found in **chapter 6**.

After this procedure the system is ready for measuring the transfer functions using the PCM4.

5.3 Power Supply

The PC does not provide all necessary voltages to supply the connected boards accordingly. That is why the SICOFI-2 Module is equipped with a connector for additional external power supply.

The voltage + 5 V is selectable internal or external by jumper J1. External 5 V power supply is choosen if sensitive noise measurements are done. With all other measurements the internal voltage source is used.

6 Glossary

ARCOFI®	Audio Ringing COdec FIlter
B	64 kbit/s voice and data channel not frame oriented
D	16 kbit/s packetized data and control transmission channel
DD	Data Downstream (at IOM interface)
DIR	Direction signal (same as FSC)
DTMF	Dual Tone Multi Frequency
DU	Data Upstream (at IOM interface)
EPIC®	Extended PCM Interface Controller
FSC	Frame Signal
ICC	ISDN Communication Controller
IEC-Q	ISDN Echo Cancellation circuit 2B1Q
IOM®	ISDN Oriented Modular
IOS	IOM Software
ISAC®-S	ISDN Subscriber Access Controller on S-bus
ISDN	Integrated Services Digital Network
LT/S	Line Termination Simulator
PC	Personal Computer
PCM	Pulse Code Modulation
S	Double wire pair (2 $\times$ B + D)
SAC	Service Access Connector
SICOFI®	SIgnal COdec FIlter
SIP	Serial Interface Port
SLC	SLIC connector
SLD	Subscriber Line Digital
SLIC	Subscriber line interface card
TE	Terminal Equipment
2B1Q	Transmission code requiring 120-kHz bandwidth

7 Menu Software Track Files

This section contains track files for connecting the Line-Card Module and the SICOFI-2.The Line-Card Module is configured just by software. The pertinent track file LISISLD.TRK contains the Line Card configuration, when the SICOFI-2 board is operated in the **SLD interface mode**.

When working in the **IOM mode** (4096 kHz), the correct track file is LISIIOM2.TRK.

7.1 Track Files for SLD Interface Mode

LISISLD.TRK

```
C ****************************************
C                 lc_sld2
C ****************************************
C
C application: initialization of the
C              line card module
C              for an sld architecture
C additional modules: sicofi2 board
C                     (sipb 5135)
C
C
C configuration:
C pcm interface:  4 hws with 32 ts each
C cfi interface:  8 bi.ports with 8 ts
C                 each (8 sld lines)
C
C configuration of the lc module:
C config register bits:
C id,cks/tc2/tc1/tc0/dch/dma/cts/res
C clock mode 7 (xtal 2048 khz)
C * reset of on board devices
C * cks=1  (3rd slot may be occupied by
C          an audio module v2.0)
W /LINECA/CONFIG/CONFIG/CONFIG F1
W /LINECA/CONFIG/CONFIG/CONFIG F0
C
C configuration of the pcm interface:
C * pcm mode 0, single clock rate
C * pfs evaluated with falling edge
C * no comparison function
W /LINECA/EPIC/PCMCFI/PMOD 00
C * pcm bit number is 256
W /LINECA/EPIC/PCMCFI/PBNR FF
C * pcm offset is 2 bits (pfs marks
C bit 5 of ts 0) in up and downstream
C direction
```

```
W /LINECA/EPIC/PCMCFI/POFD EF
W /LINECA/EPIC/PCMCFI/POFU 17
C * transmit with rising edge, receive
C with falling edge of pcl
W /LINECA/EPIC/PCMCFI/PCSR 01
C

C configuration of the cfi interface:
C * cfi mode 3, clock source: pcl/pfs
C * pfs evaluated with falling edge
C * prescaler = 1
W /LINECA/EPIC/PCMCFI/CMD1 2C
C * fsc output: fc mode 6
C * dc output: single rate
C * xmit rising, rec falling edge
W /LINECA/EPIC/PCMCFI/CMD2 C0
C * cfi bit number is 64
W /LINECA/EPIC/PCMCFI/CBNR 3F
C * pfs marks cfi ts0, bit7
C * no shift between xmit and rec
W /LINECA/EPIC/PCMCFI/CTAR 02
W /LINECA/EPIC/PCMCFI/CBSR 20
C * subchannel position: 64kbps=bits7.0
C                        32kbps=bits7.4
C                        16kbps=bits7.6
W /LINECA/EPIC/PCMCFI/CSCR 00
C
C initialization of cm ctrl field:
C * cm reset mode
W /LINECA/EPIC/MARSCR/OMDR 00
C * ff is copied to all positions of
C * the cm ctrl field
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MACR 70
C
C cfi configuration for sld:
C * cm init mode
W /LINECA/EPIC/MARSCR/OMDR 80
C cfi time slots 2 and 3 of port 4 are
C programmed as downstream feature
C control and signaling channels,
C time slots 6 and 7 as upstream
C feature ctrl and signaling channels
C cfi ts 0-7 of port 4 represent thus
C sld port 4 (amc pin 10c)
C * ts 2 downstream:
C sig value ff is transmitted
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 18
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 3 downstream:
W /LINECA/EPIC/MARSCR/MADR 00
W /LINECA/EPIC/MARSCR/MAAR 19
```

```
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts 6 upstream:
C ff is init value for sig receive
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR B8
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts 7 upstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR B9
W /LINECA/EPIC/MARSCR/MACR 7B
C
C * pcm status is
R /LINECA/EPIC/MARSCR/STAR 05
C * not synchronized (pss=0)
C
C setting epic to normal mode
W /LINECA/EPIC/MARSCR/OMDR C0
R /LINECA/EPIC/MARSCR/ISTA 08
R /LINECA/EPIC/MARSCR/STAR 25
C pcm status: synchronized (pss=1)
C
C initialization of the pcm tristate
C field, all ch. to high impedance
W /LINECA/EPIC/MARSCR/MADR 00
W /LINECA/EPIC/MARSCR/MACR 68
C
C activation epic:
C * normal mode, pcm and cfi active
C * cfi output drivers push-pull
C * mf ch. handshake protocol disabled
W /LINECA/EPIC/MARSCR/OMDR E2
C
C mask of idecl interrupts:
W /LINECA/IDEC/COMMON/VISM 0F
C
C programming of sicofi2:
C power down, 3bytes will follow:
W /LINECA/EPIC/MCHSTR/MFFIFO 05
C transmit signaling bits to tristate:
W /LINECA/EPIC/MCHSTR/MFFIFO 10
C tone generator off
W /LINECA/EPIC/MCHSTR/MFFIFO 00
C all filters off, a-law, sb input:
W /LINECA/EPIC/MCHSTR/MFFIFO 00
C address for sld port 4:
W /LINECA/EPIC/MCHSTR/MFSAR 0C
C transmit command:
W /LINECA/EPIC/MCHSTR/CMDR 04
R /LINECA/EPIC/MCHSTR/ISTA 20
C mffi interrupt: fc transfer complete
C
```

```
C read back from sicofi:
R /LINECA/EPIC/MCHSTR/STAR 25
C mffifo: empty and may be written
C read back command for sicofi:
C power up, read back cr2, cr1:
W /LINECA/EPIC/MCHSTR/MFFIFO 66
C address of sld port 4, 8 bytes are
C expected
W /LINECA/EPIC/MCHSTR/MFSAR 8C
C transmit+receive same line command:
W /LINECA/EPIC/MCHSTR/CMDR 0C
R /LINECA/EPIC/MCHSTR/ISTA 20
C mffi interrupt: fc transfer complete
R /LINECA/EPIC/MCHSTR/STAR 26
C mffifo is not empty and may be read
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 26
C mffifo is not empty and may be read
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 26
R /LINECA/EPIC/MCHSTR/MFFIFO DF
C nop command received i.e. no further
C bytes will follow!
C reset mffifo:
W /LINECA/EPIC/MCHSTR/CMDR 01
R /LINECA/EPIC/MCHSTR/STAR 25
C mffifo empty and may be written
C
C digital loop back via pcm-register
C in sicofi2 b1 channel:
W /LINECA/EPIC/MCHSTR/MFFIFO 25
W /LINECA/EPIC/MCHSTR/MFFIFO 11
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFSAR 0C
W /LINECA/EPIC/MCHSTR/CMDR 04
R /LINECA/EPIC/MCHSTR/ISTA 20
C
C transmission of idle code "aa" in b1
W /LINECA/EPIC/MARSCR/MADR AA
W /LINECA/EPIC/MARSCR/MAAR 08
W /LINECA/EPIC/MARSCR/MACR 79
C up ch. setup for b1 receive:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR A8
W /LINECA/EPIC/MARSCR/MACR 79
C reading received b1 value:
W /LINECA/EPIC/MARSCR/MAAR A8
W /LINECA/EPIC/MARSCR/MACR C8
R /LINECA/EPIC/MARSCR/MADR AA
C change value to "12":
```

```
W /LINECA/EPIC/MARSCR/MADR 12
W /LINECA/EPIC/MARSCR/MAAR 08
W /LINECA/EPIC/MARSCR/MACR 48
C reading received value:
W /LINECA/EPIC/MARSCR/MAAR A8
W /LINECA/EPIC/MARSCR/MACR C8
R /LINECA/EPIC/MARSCR/MADR 12
C
C removing digital pcm loop:
W /LINECA/EPIC/MCHSTR/MFFIFO 25
W /LINECA/EPIC/MCHSTR/MFFIFO 10
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFSAR 0C
W /LINECA/EPIC/MCHSTR/CMDR 04
R /LINECA/EPIC/MCHSTR/ISTA 20
C
C transmission of idle codes in pcm
C time slots 0 and 31 of port0:
C * "99" in ts 0:
W /LINECA/EPIC/MARSCR/MADR 99
W /LINECA/EPIC/MARSCR/MAAR 80
W /LINECA/EPIC/MARSCR/MACR 08
C * ts 0 to low impedance:
W /LINECA/EPIC/MARSCR/MADR 0F
W /LINECA/EPIC/MARSCR/MAAR 80
W /LINECA/EPIC/MARSCR/MACR 60
C * "88" in ts 31:
W /LINECA/EPIC/MARSCR/MADR 88
W /LINECA/EPIC/MARSCR/MAAR F9
W /LINECA/EPIC/MARSCR/MACR 08
C * ts 31 to low impedance:
W /LINECA/EPIC/MARSCR/MADR 0F
W /LINECA/EPIC/MARSCR/MAAR F9
W /LINECA/EPIC/MARSCR/MACR 60
C
C switching of b channels between sld
C and pcm interface:
C (u=upstream, d=downstream)
C
C * u: sip4, b1 to pcm port0, ts1:
W /LINECA/EPIC/MARSCR/MADR 81
W /LINECA/EPIC/MARSCR/MAAR A8
W /LINECA/EPIC/MARSCR/MACR 71
C * pcm port0, ts1 to low impedance:
W /LINECA/EPIC/MARSCR/MADR 0F
W /LINECA/EPIC/MARSCR/MAAR 81
W /LINECA/EPIC/MARSCR/MACR 60
C * d: pcm port0, ts1 to sip4, b1:
W /LINECA/EPIC/MARSCR/MADR 01
```

```
W /LINECA/EPIC/MARSCR/MAAR 08
W /LINECA/EPIC/MARSCR/MACR 71
C
C the connection sld b1 <-> pcm ts 1
C is established, a loop back can be
C realized by a short circuit at sac
C (pins 6 and 7) or by using the pcm
C test loop bit (ptl) in omdr:
W /LINECA/EPIC/MARSCR/OMDR F2
C removing the test loop:
W /LINECA/EPIC/MARSCR/OMDR E2
C
C transmission of signaling byte to
C subscriber:
C write value in madr (e.g. 34h)
W /LINECA/EPIC/MARSCR/MADR 34
C write subscr. address into maar
C (e.g. 18h for sip4)
W /LINECA/EPIC/MARSCR/MAAR 18
C write moc=1001 in macr:
W /LINECA/EPIC/MARSCR/MACR 48
C change value to "00":
W /LINECA/EPIC/MARSCR/MADR 00
W /LINECA/EPIC/MARSCR/MAAR 18
W /LINECA/EPIC/MARSCR/MACR 48
```

7.2 Track File for Fast IOM® Interface Mode

LISIIOM2.TRK

```
C ********************************************
C                      lc_iom2
C ********************************************
C
C application: initialization of the
C              line card module
C              for an iom2 line card
C
C setup: line card module sipb 5121
C        optional: s-access or layer-1
C        modules in 3rd amc slot and/
C        or external layer-1 modules
C        connected to sac
C        for the configuration of the
C        additional modules please
C        refer to the pertaining
C        module descriptions
C        the layer-1 modules should be
C        set to lt mode, iom2 mode
C        with an appropriate iom chan.
```

```
C        assignment as indicated
C        below
C
C note: this track file exists also in
C       a non commented version:
C       nc_iom2
C
C iom2 channel assignment:
C * ch0: dig. subsc. decentral d
C * ch1: dig. subsc. central d
C * ch2: dig. subsc. mixed d
C * ch3: analog subscriber (sicofi2)
C
C interface characteristics:
C pcm interface: 2 hws with 64 ts each
C cfi interface: 4 hws with 32 ts each
C                (4 iom2 interfaces)
C
C configuration of the lc module:
C config register bits:
C id,cks/tc2/tc1/tc0/dch/dma/cts/res
C * clock mode 6 (xtal 4096khz)
C * reset of on board devices
C * cks=0: 3rd slot may be s-access
C   or p-access module
W /LINECA/CONFIG/CONFIG/CONFIG 61
W /LINECA/CONFIG/CONFIG/CONFIG 60
C * note: if 3rd slot should be layer-1
C         module please program:
C         config e1
C         config e0
C
C configuration of the pcm interface:
C * pcm mode 1, single clock rate
C * pfs evaluated with falling edge
C * port assignment: port0=txd0,rxd0
C                    port1=txd2,rxd3
C * no comparison function
W /LINECA/EPIC/PCMCFI/PMOD 44
C * pcm bit number is 512
W /LINECA/EPIC/PCMCFI/PBNR FF
C * no pcm offset, output with rising,
C * input with falling edge
W /LINECA/EPIC/PCMCFI/POFD F0
W /LINECA/EPIC/PCMCFI/POFU 18
W /LINECA/EPIC/PCMCFI/PCSR 45
C
C configuration of the cfi interface:
C * cfi mode 0, clock source: pcl/pfs
C * pfs evaluated with falling edge
C * prescaler = 1
```

```
W /LINECA/EPIC/PCMCFI/CMD1 20
C * fsc output: fc mode 6
C * dcl output: double rate
C * xmit rising, rec falling edge
W /LINECA/EPIC/PCMCFI/CMD2 D0
C * cfi bit number is 256
W /LINECA/EPIC/PCMCFI/CBNR FF
C * pfs marks cfi ts31,bit1
W /LINECA/EPIC/PCMCFI/CTAR 02
C * no shift between xmit and rec
W /LINECA/EPIC/PCMCFI/CBSR 00
C * subchannel position: 64kbps=bits7.0
C                        32kbps=bits7.4
C                        16kbps=bits7.6
W /LINECA/EPIC/PCMCFI/CSCR 00
C
C initialization of cm ctrl field:
C * cm reset mode
W /LINECA/EPIC/MARSCR/OMDR 00
C * ff is copied to all positions of
C * the cm ctrl field
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MACR 70
C
C cfi configuration for iom2:
C * cm init mode
W /LINECA/EPIC/MARSCR/OMDR 80
C

C cfi time slots 2 and 3 of port 0
C are programmed as monitor and c/i
C channels, decentral d ch. handling
C (d ch. not switched to pcm)
C cfi ts 0-3 represent thus iom2 ch.0
C with b1, b2, monitor and d/ci/mr,mx
C * ff is copied to all addressed
C * positions of the cm data field
W /LINECA/EPIC/MARSCR/MADR FF
C * ts 2 downstream:
W /LINECA/EPIC/MARSCR/MAAR 08
W /LINECA/EPIC/MARSCR/MACR 78
C * ts 3 downstream:
W /LINECA/EPIC/MARSCR/MAAR 09
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts 2 upstream:
W /LINECA/EPIC/MARSCR/MAAR 88
W /LINECA/EPIC/MARSCR/MACR 78
C * ts 3 upstream:
W /LINECA/EPIC/MARSCR/MAAR 89
W /LINECA/EPIC/MARSCR/MACR 70
C
C cfi time slots 6 and 7 of port 0 are
```

```
C programmed as monitor and c/i
C channels, central d ch. handling
C (d ch. is switched to pcm port 0,
C ts 5, bits 1..0 in up and downstream
C direction
C cfi-ts 4-7 represent thus iom2 ch. 1
C * ts 6 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 18
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 7 downstream:
W /LINECA/EPIC/MARSCR/MADR 09
W /LINECA/EPIC/MARSCR/MAAR 19
W /LINECA/EPIC/MARSCR/MACR 74
C * ts 6 upstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 98
W /LINECA/EPIC/MARSCR/MACR 78
C * ts 7 upstream:
W /LINECA/EPIC/MARSCR/MADR 89
W /LINECA/EPIC/MARSCR/MAAR 99
W /LINECA/EPIC/MARSCR/MACR 74
C

C cfi time slots 10 and 11 of port 0
C are programmed as monitor and c/i
C channels, mixed d ch. handling
C upstream the d ch. is switched to
C pcm port 0, ts 5, bits 3..2
C downstream the d ch. is not switched
C directly to cfi port 0, ts 11 but
C is switched to cfi port 3, ts 1,
C bits 7..6 which is connected to cdr
C of the decentralized idec
C cfi ts 8-11 represent thus iom2 ch.2
C * ts 10 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 28
W /LINECA/EPIC/MARSCR/MACR 78
C * ts 11 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 29
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts 10 upstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR A8
W /LINECA/EPIC/MARSCR/MACR 78
C * ts 11 upstream:
W /LINECA/EPIC/MARSCR/MADR 89
W /LINECA/EPIC/MARSCR/MAAR A9
W /LINECA/EPIC/MARSCR/MACR 75
C * downstream connection d ch.:
```

```
W /LINECA/EPIC/MARSCR/MADR 09
W /LINECA/EPIC/MARSCR/MAAR 07
W /LINECA/EPIC/MARSCR/MACR 75
C
C cfi time slots 14 and 15 of port 0
C are programmed as monitor and
C signaling channels (analog iom)
C cfi ts 12-15 represent thus iom2 ch3
C * ts 14 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 38
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 15 downstream:
W /LINECA/EPIC/MARSCR/MAAR 39
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts 14 upstream:
W /LINECA/EPIC/MARSCR/MAAR B8
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 15 upstream:
W /LINECA/EPIC/MARSCR/MAAR B9
W /LINECA/EPIC/MARSCR/MACR 7A
C * pem status is
R /LINECA/EPIC/MARSCR/STAR 05
C * not synchronized (pss=0)
C
C setting epic to normal mode
W /LINECA/EPIC/MARSCR/OMDR C0
R /LINECA/EPIC/MARSCR/ISTA 08
R /LINECA/EPIC/MARSCR/STAR 25
C pcm status: synchronized (pss=1)
C
C initialization of the pcm tristate
C field, all ch. to high impedance
W /LINECA/EPIC/MARSCR/MADR 00
W /LINECA/EPIC/MARSCR/MACR 68
C
C activation epic:
C * normal mode, pcm and cfi active
C * cfi output drivers push-pull
C * mf ch. handshake protocol enabled
W /LINECA/EPIC/MARSCR/OMDR E6
C
C reset cififo:
W /LINECA/EPIC/MARSCR/CMDR 10
C
C setting pcm port0, ts 5 to low
C impedance:
W /LINECA/EPIC/MARSCR/MADR 0F
W /LINECA/EPIC/MARSCR/MAAR 89
W /LINECA/EPIC/MARSCR/MACR 60
C
```

```
C mask of idec1 interrupts:
W /LINECA/IDEC/COMMON/VISM 0F
C
C initialization of idec1
C * single connection iom mode
C * cha assigned to iom ch0, uncond.
C   transmission, no address compare
C   (completely decentral d channel
C   handling)
C * chb not used (central d handling)
C * chc assigned to iom ch2, master
C   mode, sapi s compare (mixed d ch.
C   handling)
C * chd not used (analog iom)
C
C common registers:
W /LINECA/IDEC/COMMON/CCR 82
W /LINECA/IDEC/COMMON/ACR 4A
C
C cha registers:
W /LINECA/IDEC/CHA_A/MODE 0C
C
C chc registers:
W /LINECA/IDEC/CHA_C/TSR 04
W /LINECA/IDEC/CHA_C/MODE 6C
C
C * enabling interrupts, reset cha,c
W /LINECA/IDEC/COMMON/VISM 0A
W /LINECA/IDEC/CHA_A/CMDR C1
R /LINECA/IDEC/CHA_A/ISTA 10
R /LINECA/IDEC/CHA_A/STAR 11
W /LINECA/IDEC/CHA_C/CMDR C1
R /LINECA/IDEC/CHA_C/ISTA 50
R /LINECA/IDEC/CHA_C/STAR 51
C
C initialization of idec2
C * single connection ts mode
C * ch b is assigned to pcm port0, ts5
C   bits 1..0, uncond. transmission
C   no address compare (the d ch. of
C   iom ch1 is handled centralized)
C * chc is assigned to pcm port0, ts5
C   bits 3..2, uncond., tr., sapi p
C   address compare (the p data of iom
C   ch2 is handled centralized)
C
C * common registers:
W /LINECA/IDEC_2/COMMON/CCR 04
W /LINECA/IDEC_2/COMMON/ACR 49
C
C * chb registers
```

```
W /LINECA/IDEC_2/CHA_B/TSR 17
W /LINECA/IDEC_2/CHA_B/MODE 0C
C
C * chc registers:
W /LINECA/IDEC_2/CHA_C/TSR 16
W /LINECA/IDEC_2/CHA_C/MODE 0C
C
C * enabling interrupts, reset chb,c
W /LINECA/IDEC_2/COMMON/VISM 09
W /LINECA/IDEC_2/CHA_B/CMDR C1
R /LINECA/IDEC_2/CHA_B/ISTA 30
R /LINECA/IDEC_2/CHA_B/STAR 31
W /LINECA/IDEC_2/CHA_C/CMDR C1
R /LINECA/IDEC_2/CHA_C/ISTA 50
R /LINECA/IDEC_2/CHA_C/STAR 51
C
C the line card is now ready for use
C in order to test the setup you can
C execute the track file lc_isac
C
C ****************************************
C
C ***************************************
C *               SICOFI2               *
C ***************************************
C
C Hardware: Line Card SIPB 5121
C           SICOFI2 Board SIPB 5135
C           PCM4 Adaptor SIPB 5311
C
C configuration:
C         Line Card: via software
C
C         SICOFI 2: S1 in position 5
C
C         PCM4 Adaptor: J1 is open
C ***************************************
C
C SICOFI2 set up in channel 3 of IOM2
C
C          S1 in position 5
C
C ***************************************
C please run the track file
C            LC_IOM2.TRK
C first to configure the Line Card
C ***************************************
C ***************************************
C
C selecting EPIC to monitor handshake
C in channel 3
```

```
W /LINECA/EPIC/MCHSTR/MFSAR 1C
C ***************************************
C in case of channel 0  MFSAR = 04       *
C                       S1 position 2    *
C in case of channel 1  MFSAR = 0C       *
C                       S1 position 3    *
C in case of channel 2  MFSAR = 14       *
C                       S1 position 4    *
C in case of channel 4  MFSAR = 24       *
C                       S1 position 6    *
C in case of channel 5  MFSAR = 2C       *
C                       S1 position 7    *
C in case of channel 6  MFSAR = 34       *
C                       S1 position 8    *
C in case of channel 7  MFSAR = 3C       *
C                       S1 position 9    *
C ***************************************
C
C channel 3 B1 to PCM time slot 1
W /LINECA/EPIC/MARSCR/MADR 81
W /LINECA/EPIC/MARSCR/MAAR B0
W /LINECA/EPIC/MARSCR/MACR 71
W /LINECA/EPIC/MARSCR/MADR 0F
W /LINECA/EPIC/MARSCR/MAAR 81
W /LINECA/EPIC/MARSCR/MACR 60
C

C PCM time slot 1 to channel 3 B1
W /LINECA/EPIC/MARSCR/MADR 01
W /LINECA/EPIC/MARSCR/MAAR 31
W /LINECA/EPIC/MARSCR/MACR 71
C
C channel 3 B2 to PCM time slot 2
W /LINECA/EPIC/MARSCR/MADR 82
W /LINECA/EPIC/MARSCR/MAAR B1
W /LINECA/EPIC/MARSCR/MACR 71
W /LINECA/EPIC/MARSCR/MADR 0F
W /LINECA/EPIC/MARSCR/MAAR 82
W /LINECA/EPIC/MARSCR/MACR 60
C
C PCM time slot 2 to channel 3 B2
W /LINECA/EPIC/MARSCR/MADR 02
W /LINECA/EPIC/MARSCR/MAAR 30
W /LINECA/EPIC/MARSCR/MACR 71
C
C
C sicofi identification:
C write to SICOFI2 80h, 00h
W /LINECA/EPIC/MCHSTR/MFFIFO 80
W /LINECA/EPIC/MCHSTR/MFFIFO 00
C EPIC enable receive + transmit
W /LINECA/EPIC/MCHSTR/CMDR 08
```

```
R /LINECA/EPIC/MCHSTR/ISTA 20
C EPIC received data
R /LINECA/EPIC/MCHSTR/STAR 26
C first byte from SICOFI2
R /LINECA/EPIC/MCHSTR/MFFIFO 80
R /LINECA/EPIC/MCHSTR/STAR 26
C second byte from SICOFI2
R /LINECA/EPIC/MCHSTR/MFFIFO 80
R /LINECA/EPIC/MCHSTR/STAR 27
C reset FIFO
W /LINECA/EPIC/MCHSTR/CMDR 01
R /LINECA/EPIC/MCHSTR/STAR 25
C
C initialization of sicofi:
C CR4, CR3, CR2, CR1
C 00h, 00h, 00h, 00h
C for both channels of SICOFI2
C
C SICOFI2 address = 81h
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C channel A:
W /LINECA/EPIC/MCHSTR/MFFIFO 05
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 00
C channel B:
W /LINECA/EPIC/MCHSTR/MFFIFO 85
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 47
C send the initialisation bytes
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C
C
C power up both channels
W /LINECA/EPIC/MCHSTR/MFFIFO 24
```

```
W /LINECA/EPIC/MCHSTR/MFFIFO E4
C send the bytes
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
W /LINECA/EPIC/MCHSTR/CMDR 01
R /LINECA/EPIC/MCHSTR/STAR 25
C end of power up
C
C
C end of track file
C
```

SLIC Babyboard STUS 5502 for HARRIS SLIC HC 5502

Contents **Page**

1 Features

- Interface to SICOFI Testboard STUT 2060
- Interface to SICOFI 2 SIPB 5135
- Analog telephone directly connectable
- Ring relay on board
- Secondary protection circuit on board

2 Use

For one of our SLIC-applications a HARRIS SLIC Babyboard has been designed in order to connect it with the SICOFI Testboard STUT 2060.

With both boards it is possible to measure the transfer functions of the HARRIS SLIC HC 5502A together with the SICOFI and to check the calculations done with SICOFI coefficients program.

The signaling pins of SICOFI are connected with the control interface of the HARRIS SLIC to control the SLIC functions. Therefore it is possible to select the modes

power down
power up
ringing

and to read out the status of

hook switch (OFF or ON),
ring/tip, and
ground-key.

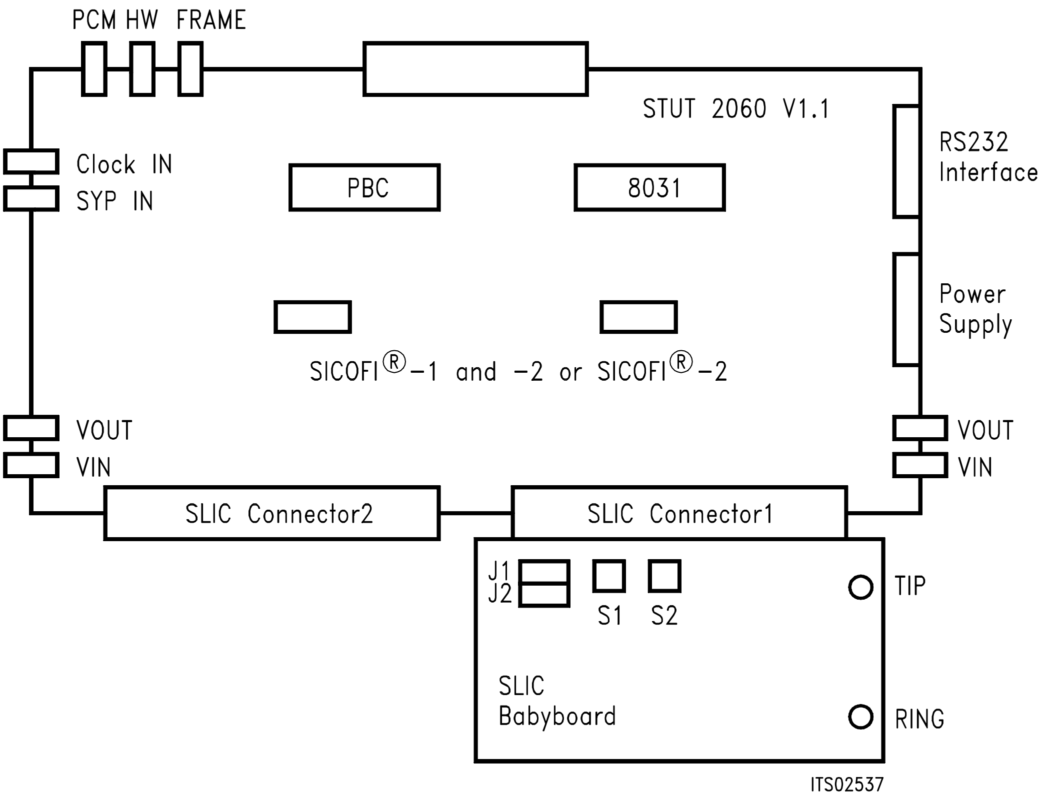


Figure 1
Connecting the SLIC Babyboard to the SICOFI® Testboard

For practical use the SLIC Babyboard STUS 5502 is inserted into one of the SLIC connectors SLC of the SICOFI Testboard STUT 2060. Using a set-up like that shown in **figure 1**, the transfer functions of an analog line card can be established. For programming, the Byte File is used which is to be found in the HARRIS SLIC HC 5502 Application Note.

3 Circuitry

3.1 Block Diagram

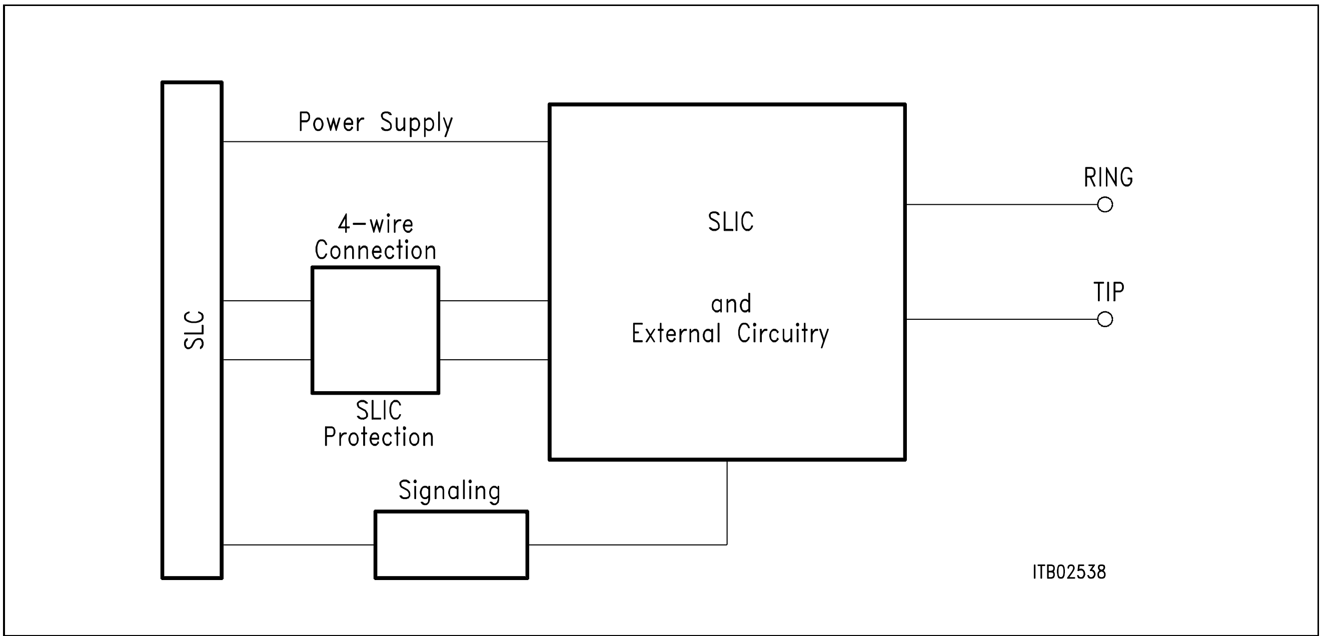


Figure 2
Block Diagram of the SLIC Babyboard STUS 5502

In **figure 2** the three functional blocks of the SLIC Babyboard are shown:

– SLIC
– Protection circuit
– Signaling

3.1.1 SLIC

The SLIC requires a few external components for output impedance, echo cancellation, filter capacitors, and power supply. Some of these functions are realized by the SICOFI and hence it was possible to reduce the number of extra components.

The description of the SLIC is to be found in the pertinent Application Note. The SLIC switches the ringer relay and provides a digital parallel interface to control the SLIC modes. These modes are

– power down

– conversation (active)

– ringing.

–

3.1.2 Protection Circuit

The protection circuit screens the SLIC against high voltages (secondary protection). This is realized by 2 diodes D1, D2 and the fuse resistors $R_{B1} \dots R_{B4}$. No primary protection, however, e.g. surge arristors, is provided.

3.1.3 Signaling

The signaling lines connect the SICOFI signaling interface to the digital SLIC interface. The SICOFI switches the SLIC into one of the three possible modes and the SLIC provides the corresponding information on the loop status (ground key or on/off-hook) for the SICOFI or SICOFI-2. Actual ringing, however, is not possible because there is no ringer relais installed.

3.1.4 Power Supply

Power is supplied to the SLIC via the SLIC connector SLC.

3.2 Connector Pin-Outs

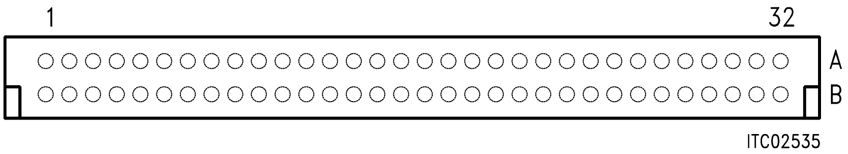


Figure 3
SLIC Connector SLC

Note: Pins not mentioned are not connected

Pin	Row	Function	Signal	Meaning
12	A	I	GND	Power supply
13	A	I	+ 5 V	Power supply
19	A	I	– 48 V	Power supply
21	A	I	SO1	/RC
22	A	I	SO2	/PD
24	A	O	SI1	/SHD
25	A	O	SI2	/GKD
26	A	I	SI3	/GKD
28	A	I	AGND	Analog ground
29	A	O	VIN	4-wire analog output
31	A	I	VOUT	4-wire analog input
32	A	I	AGND	Analog ground
4	C	I	+ 12 V	Power supply

3.3 Wiring Diagram

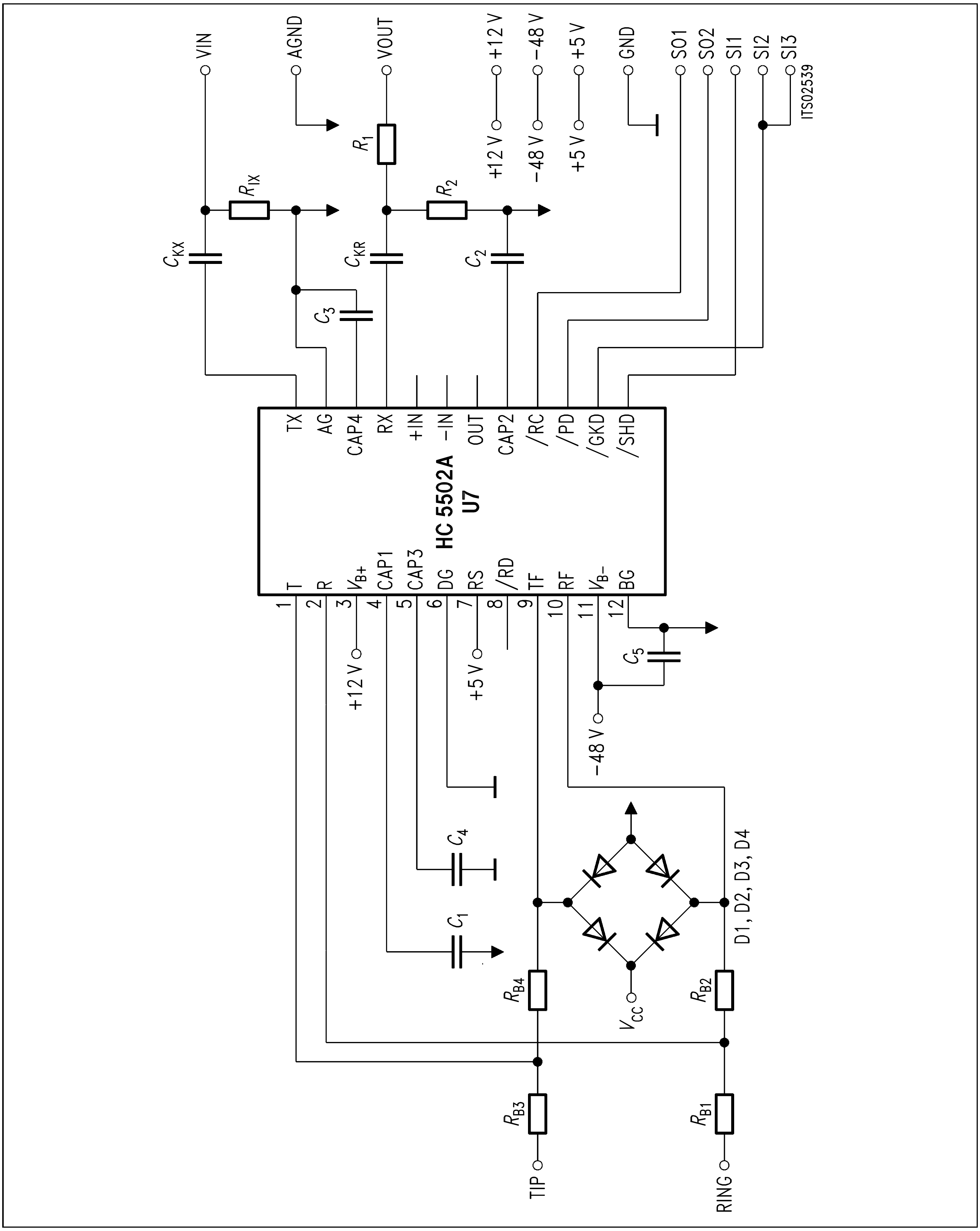


Figure 4
Wiring Diagram

3.4 List of Replaceable Parts

Component	Type/Value
IC1	HC 5502
D1 … D4	BAY 45
D5, D6	ZPO3V9
C_1	470 nF/100 V
C_2	150 nF/100 V
C_3	1 µF/100 V
C_4	330 nF/100 V
C_{kx}, C_{kr}	470 nF/100 V
R_1, R_2	1 k Ω
R_{B1} … R_{B4}	150 Ω
R_{ix}	10 k Ω

3.5 Floor Plan

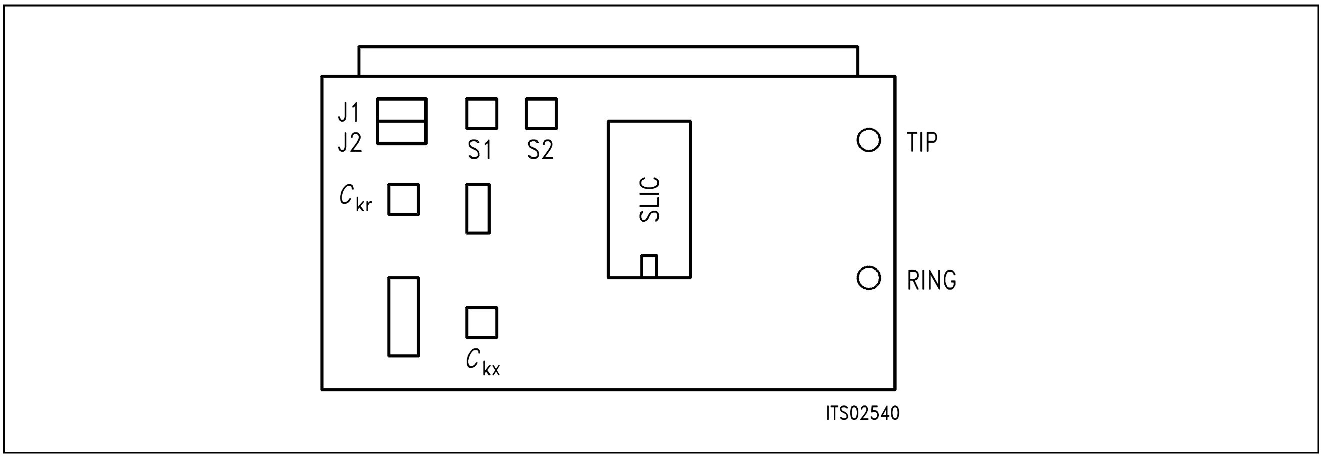


Figure 5
Floor Plan of the STUS 5502 Babyboard

4 Operational Information

4.1 Configuration

Before power is applied, the SLIC Babyboard has to be configured by means of setting the jumpers J1 and J2 and switches S1 and S2.
Possible configurations are:

– with or without voltage divider in receive direction

– connection to 4-wire SLIC side

The Babyboard contains two jumpers J1 and J2 to select the voltage divider, and two switches S1 and S2 to establish the connection to the 4-wire SLIC side (**see figure 5**).

Voltage divider not used	J1 set
Voltage divider used	J2 set
Connection to SICOFI VIN	S2 in position ON
Connection to SICOFI VOUT	S1 in position ON

4.2 Mode Select

The actual modes of the HARRIS SLIC HC 5502 are selected by the digital interface. This interface is connected to the signaling pins of the SICOFI. The signaling commands are different for the SICOFI Testboard STUT 2060 and for the SICOFI-2 Board SIPB 5135.

4.2.1 Mode Select for STUT 2060

Mode selection differs for the Testboard STUT 2060 being equipped with the SICOFI PEB 2060 or with the SICOFI-2 PEB 2260.
Following byte sequences apply to the STUT 2060 using the **PEB 2060**:

SIG0 = 80	power down
SIG0 = C0	active, conversation
SIG0 = 30	ringing (no on-board ring relais)

The line status (off-hook/ground-key), which is selected by the above signaling, can be read out via the SICOFI SIP-line:

SIG0: 7F	ON-hook
SIG0: 6F	OFF-hook and ground-key
SIG0: 0F	OFF-hook (no ground-key)

Following byte sequences apply to the STUT 2060 using the **PEB 2260** for both channels:

SIG0 = 11	power down
SIG0 = 33	active, conversation
SIG0 = 00	ringing (no on-board ring relais)

The line status can be read out via the SICOFI SIP-line:

SIG0: 77	ON-hook
SIG0: 00	OFF-hook and ground-key
SIG0: 66	OFF-hook (no ground-key)

4.2.2 Mode Select for SIPB 5135

Following byte sequences apply to the SIPB 5135 using the **PEB 2260** channel A (channel B = + 80_H):

C/I = 07	power down
C/I = 0F	active, conversation
C/I = 03	ringing (no on-board ring relais)

The loop and ground key information are available from the SICOFI-2 Board for both SLICs at the same time):

C/I = DB	loop detection: OFF-hook, ground key not pushed
C/I = 03	loop detection: OFF-hook, ground key pushed
C/I = FF	loop detection: ON-hook

5 Glossary

DIR	Direction signal (same as FSC)
FSC	Frame Synchronization Clock
PC	Personal Computer
PCM	Pulse Code Modulation
SICOFI	SIgnal processing COdec FIlter
SIG	SIGnaling byte at the SIP-line
SIP	Serial Interface Port
SIPB	Siemens ISDN PC User Board (system)
SLD	Subscriber Line Data
STUS	Siemens Telecom User Board SLIC
STUT	Siemens Telecom User Board Testboard
SYP	Synchronous Port

6 Application and Example

The Babyboard STUS 5502 is used in connection with the SICOFI Testboard STUT 2060 when an analog line card application is tested using HARRIS SLICs HC 5502A. To demonstrate its functionality a set-up is given below: The Babyboard is connected to the Testboard via the SLIC connector SLC and configured as described in **chapter 4**. The PCM4 is connected to the Testboard for to measure the transfer functions of the SICOFI and the SLIC. For the connection and programming procedures of the PCM4 refer to the SICOFI Testboard description.

The programming of SICOFI is listed in the SICOFI Application Note "SICOFI PEB 2060 + HARRIS SLIC HC 5502". The byte file (HC5502.BYT) is shown in the following **table 1** for the SICOFI Testboard STUT 2060 using the PEB 2060:

Table 1
Byte File to Program the SICOFI®

PSR = 36
CAM00 = 41
CAM20 = 40
CIW0 = 06, F4, 80
CIW0 = 13, 30, BA, EA, 25, 23, 41, C1, BB
CIW0 = 23, 50, C8, B5, 4A, C2, 21, 04, 90
CIW0 = 2B, D0, C8, 84, DC, B1, 93, 02, 1D
CIW0 = 30, A0, 11, 20, 92
CIW0 = 03, C4, 12, 23, 32, 72, B9, B2, BA
CIW0 = 0B, 00, 97, FD, C8, DD, 4C, C2, BC
CIW0 = 18, 19, 19, 11, 19
CIW0 = 26, F4, 78
SIG0 = C0

Switch and Jumpers Settings

Before connecting the Testboard to the PCM4 and SLIC Babyboard respectively, make sure that all jumpers and switches are set correctly.

Testboard:	DIL switch 1.1 – 1.4 ON	
	DIL switch 2.1 – 2.4 ON	
Babyboard:	Voltage divider not used	J1 set
	Voltage divider used	J2 set
	Connection to SICOFI VIN	S2 in position ON
	Connection to SICOFI VOUT	S1 in position ON

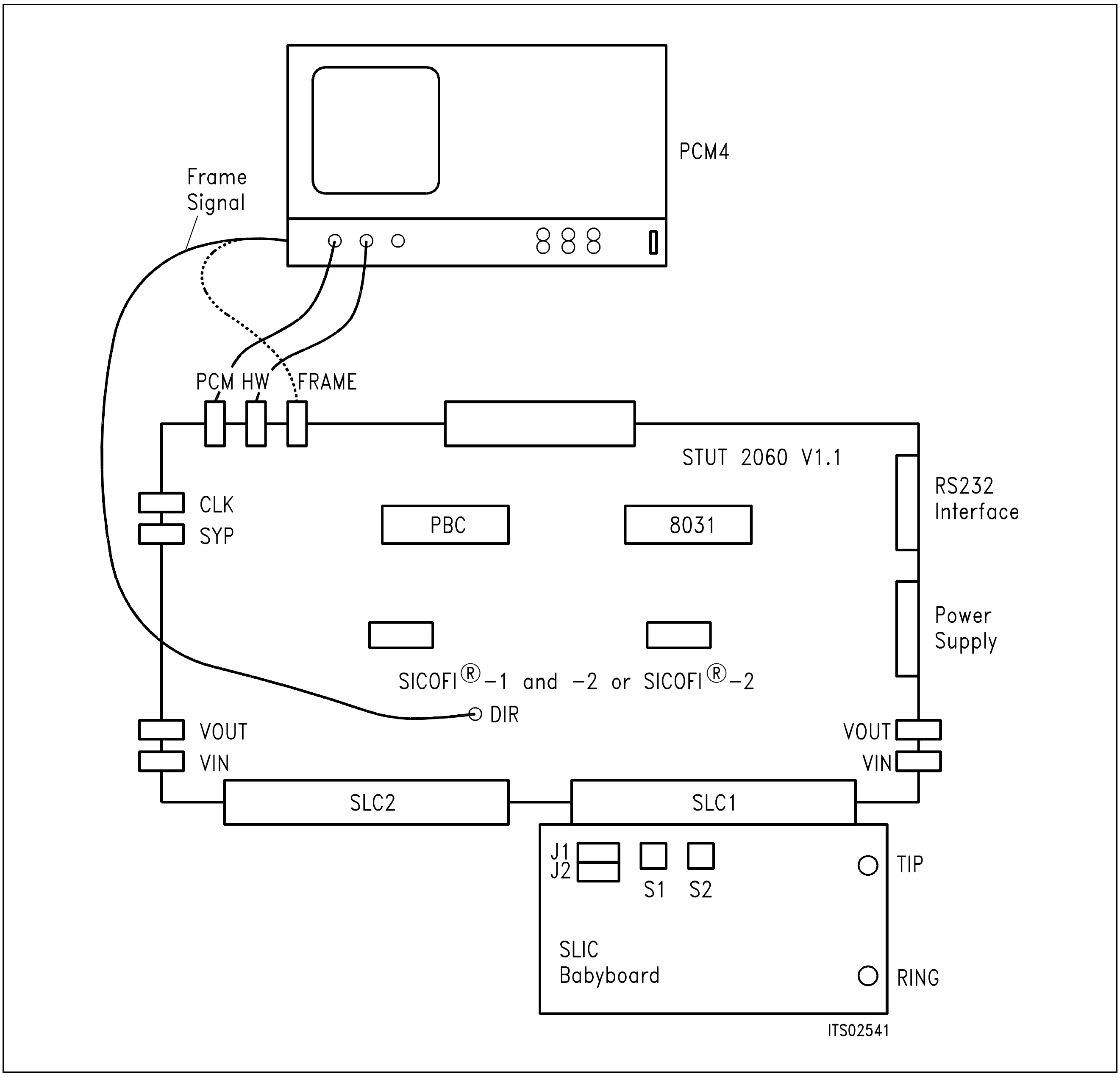


Figure 6
SICOFI® Measurement Set-Up

Required hardware for a measurement set-up:

1	PC IBM AT or compatible
1	PCM4 (Measuring set of Wandel & Goltermann)
1	SICOFI Testboard STUT 2060
1	SLIC Babyboard

SLIC Babyboard STUS 5509 for HARRIS SLIC HC 5509

Contents **Page**

1 Features

- Interface to SICOFI Testboard STUT 2060
- Interface to SICOFI-2 Board SIPB 5135
- Analog telephone directly connectable
- Ring relay on board
- Secondary protection circuit on board

2 Use

For one of our SLIC-applications a HARRIS SLIC Babyboard has been designed in order to connect it with the SICOFI Testboard STUT 2060.

With both boards it is possible to measure the transfer functions of the HARRIS SLIC HC 5509 together with the SICOFI and to check the calculations done with SICOFI coefficients program.

The signaling pins of SICOFI are connected with the control interface of the HARRIS SLIC to control the SLIC functions. Therefore it is possible to select the modes
power down
power up
ringing
and to read out the status of
hook switch (OFF or ON),
ring/tip, and
ground-key.

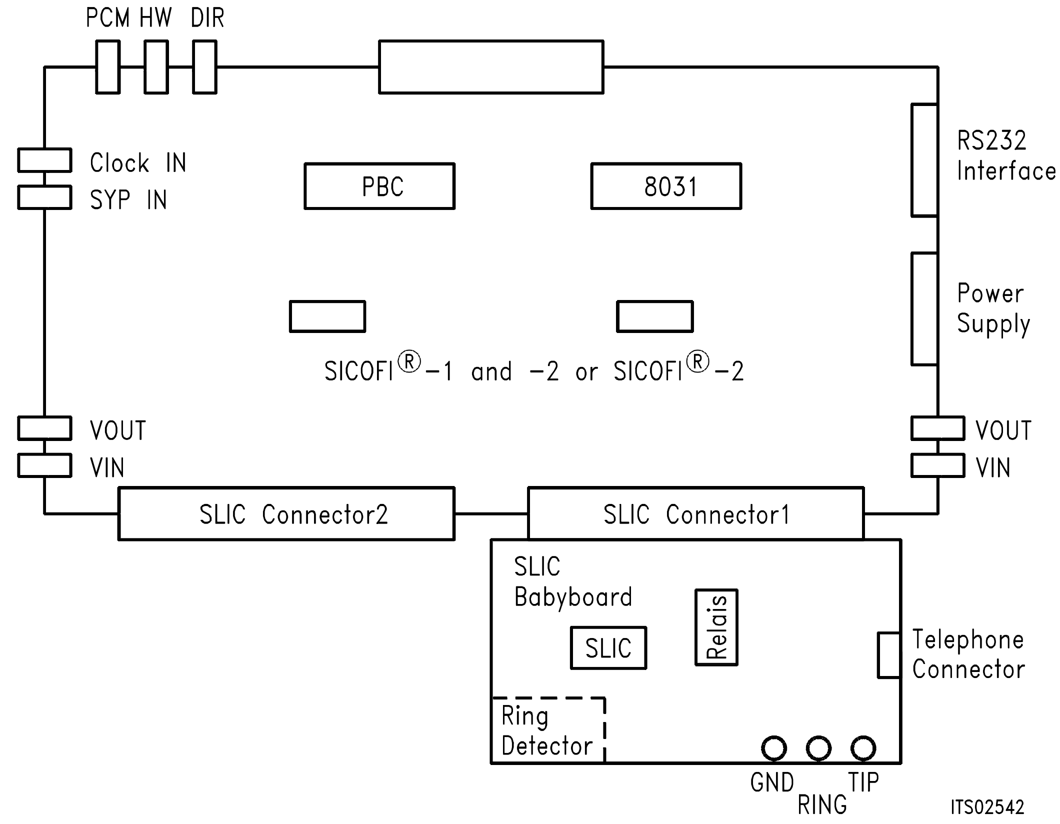


Figure 1
Connecting the SLIC Babyboard to the SICOFI® Testboard

For practical use the SLIC Babyboard STUS 5509 is inserted into one of the SLIC connectors SLC of the SICOFI Testboard STUT 2060. Using a set-up like that shown in **figure 1**, the transfer functions of an analog line card can be established. For programming, the Byte File is used which is to be found in the HARRIS SLIC HC 5502 Application Note, the SICOFI however has to be switched to the ’AGR’ with 6 dB attenuation. The reason is that in contrast to the STUS 5502 the STUS 5509 has no voltage devider on board.

3 Circuitry

3.1 Block Diagram

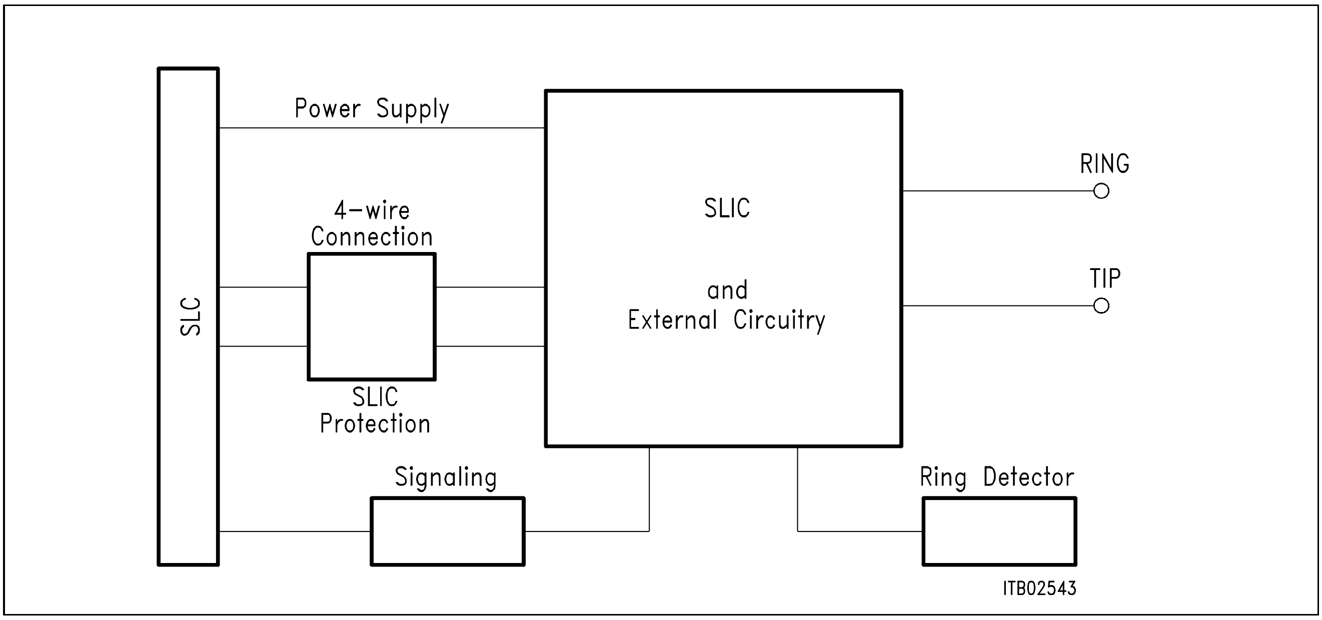


Figure 2
Block Diagram of the SLIC Babyboard STUS 5509

In **figure 2** the four functional blocks of the SLIC Babyboard are shown:

- SLIC
- Protection circuit
- Signaling
- Ring detector

3.1.1 SLIC

The SLIC requires a few external components for output impedance, echo cancellation, filter capacitors, and power supply. Some of these functions are realized by the SICOFI and hence it was possible to reduce the number of extra components.

The description of the SLIC is to be found in the HC 5502A Application Note. The SLIC switches the ringer relay and provides a digital parallel interface to control the SLIC modes. These modes are

– power down

– conversation (active)

– ringing.

3.1.2 Protection Circuit

The protection circuit screens the SLIC against high voltages (secondary protection). This is realized by 2 diodes D1, D2 and the fuse resistors R_{B1} … R_{B4}. No primary protection, however, e.g. surge arristors, is provided.

3.1.3 Signaling

The signaling lines connect the SICOFI signaling interface to the digital SLIC interface. The SICOFI switches the SLIC into one of the three possible modes and the SLIC provides the corresponding information on the loop status (ground key or on/OFF-hook) for the SICOFI or SICOFI-2.

3.1.4 Ring Detector

The ring detector provides a signal when the ringing signal crosses 0 V. Only in this moment the SLIC can activate the ring relais, because there is no noise on the line.

3.1.5 Power Supply

Power is supplied to the SLIC via the SLIC connector SLC.

3.2 Connector Pin-Outs

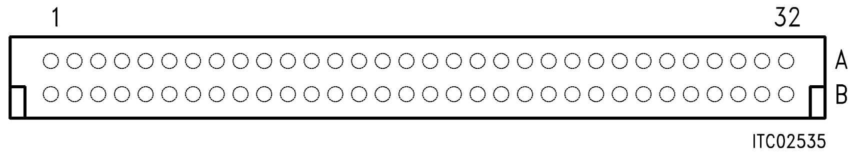


Figure 3
SLIC Connector SLC

Note: Pins not mentioned are not connected.

Pin	Row	Function	Signal	Meaning
12	A	I	GND	Power supply
13	A	I	+ 5 V	Power supply
19	A	I	– 48 V	Power supply
21	A	I	SO1	/F0
22	A	I	SO2	/F1
23	A	I	SO3	/TEST
24	A	O	SI1	/SHD
25	A	O	SI2	/GKD
26	A	I	SI3	/ALARM
28	A	I	AGND	Analog ground
29	A	O	VIN	4-wire analog output
31	A	I	VOUT	4-wire analog input
32	A	I	AGND	Analog ground
4	C	I	+ 12 V	Power supply

3.3 Wiring Diagram

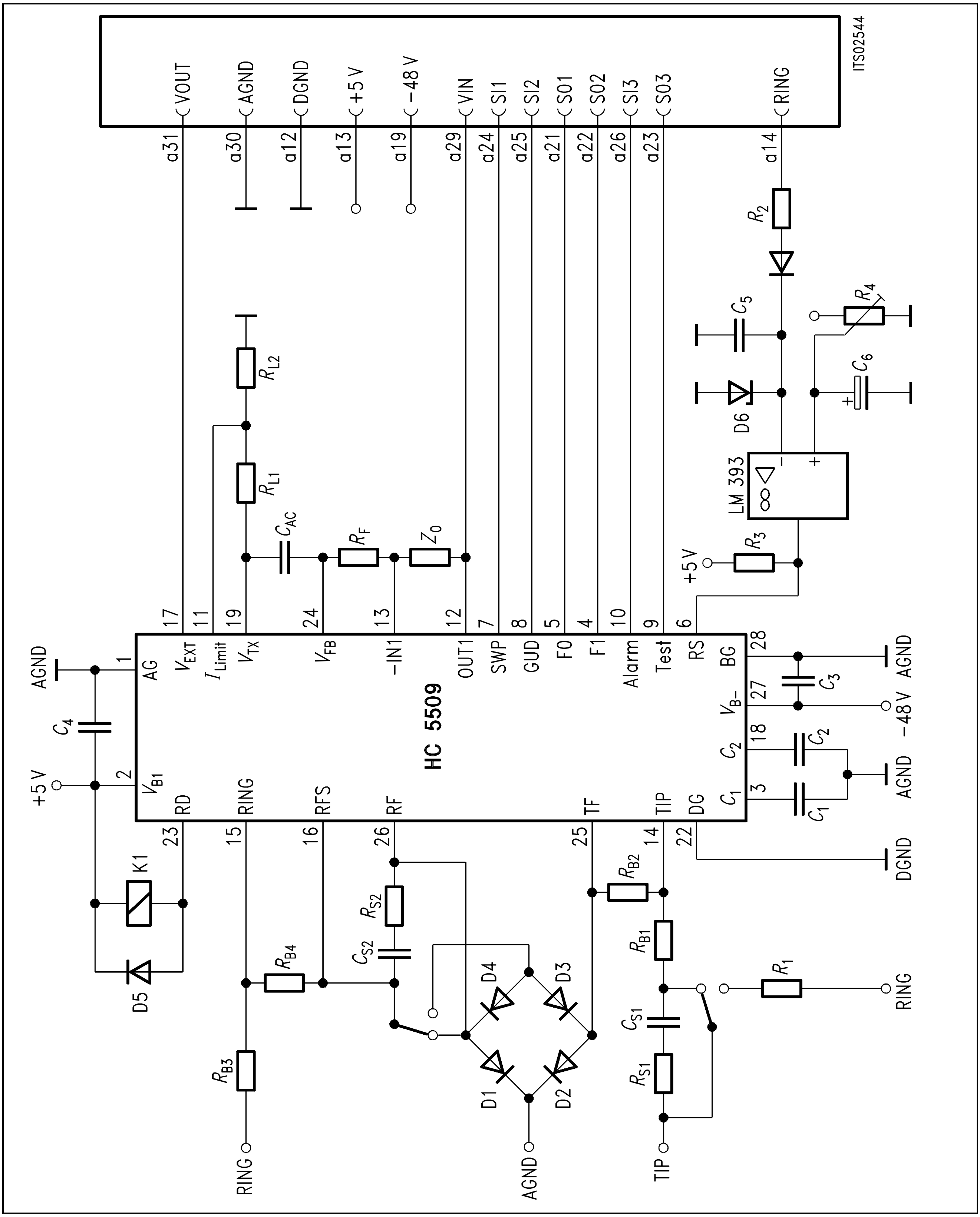


Figure 4
Wiring Diagram of the SLIC Babyboard STUS 5509

3.4 List of Replaceable Parts

Component	Type/Value
D1 … D5	1N4007
D6	BZX55C3V3
D7	1N4148
C_1	300 nF/30 V
C_2	680 nF/20 V
C_3, C_4	1 µF/100 V
C_5	47 nF
C_6	2.2 µF/40 V
C_7	100 nF
C_8	1 µF
C_{s1}, C_{s2}	100 nF
C_{AC}	470 nF/100 V
R_1	3.3 kΩ
R_2, R_3	10 kΩ
R_4	20 kΩ
R_{B1} … R_{B4}	50 Ω 1 %
R_{s1}, R_{s2}	1 kΩ
R_{L1}, R_{L2}	100 kΩ
R_F	20 kΩ
Z_0	60 kΩ

3.5 Floor Plan

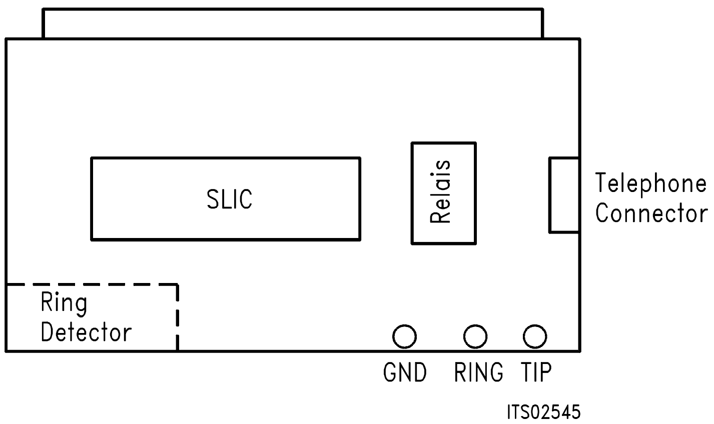


Figure 5
Floor Plan of the STUS 5509 Babyboard

4 Operational Information

4.1 Configuration

Before power is applied, the SLIC Babyboard has to be connected to the a/b-lines or a telephone and to be plugged to the Testboard.

4.2 Mode Select

The actual modes of the HARRIS SLIC HC 5509 are selected by the digital interface. This interface is connected to the signaling pins of the SICOFI. The signaling commands are different for the SICOFI Testboard STUT 2060 and for the SICOFI-2 Board SIPB 5135. In addition a software reset is required to switch it to the conversation mode.

4.2.1 Mode Select for STUT 2060

Mode selection differs for the Testboard STUT 2060 being equipped with the SICOFI PEB 2060 or with the SICOFI-2 PEB 2260.
Following byte sequences apply to the STUT 2060 using the **PEB 2060**:

SIG0 = 60	power down
SIG0 = 20	active, conversation
SIG0 = 10	ringing
SIG0 = E0	loop power denial active

The line status (OFF-hook/ground-key), which is selected by the above signaling, can be read out via the SICOFI SIP-line:

SIG0: 111x xxxx	ON-hook
SIG0: 001x xxxx	OFF-hook and ground-key
SIG0: 011x xxxx	OFF-hook (no ground-key)
SIG0: xx0x xxxx	thermal protection active

Conversation is programmed as follows:

SIG0 = 20
SIG0 = 60
SIG0 = 20

Following byte sequences apply to the STUT 2060 using the **PEB 2260** for both channels:

SIG0 = 66	power down
SIG0 = 44	active, conversation
SIG0 = 33	ringing (no ON-board ring relais)

The line status can be read out via the SICOFI SIP-line (both SLICs have the same status):

SIG0: x111 x111	ON-hook
SIG0: x010 x010	OFF-hook and ground-key
SIG0: x110 x110	OFF-hook (no ground-key)

4.2.2 Mode Select for SIPB 5135

Following byte sequences apply to the SIPB 5135 using the **PEB 2260** channel A (channel B = + 80h):

C/I = 7B	power down
C/I = 73	active, conversation
C/I = 0F	ringing (no ON-board ring relais)

The loop and ground key information are available from the SICOFI-2 Board for both SLICs at the same time):

C/I = DB	loop detection: OFF-hook, ground key not pushed
C/I = 93	loop detection: OFF-hook, ground key pushed
C/I = FF	loop detection: ON-hook

5 Glossary

DIR	Direction signal (same as FSC)
FSC	Frame Synchronization Clock
PCM	Pulse Code Modulation
SICOFI	SIgnal processing COdec FIlter
SIG	SIGnaling byte at the SIP-line
SIP	Serial Interface Port
SIPB	Siemens ISDN PC User Board (system)
SLC	SLIC Interface Connector
SLD	Subscriber Line Data
SLIC	Subscriber Line Interface Circuit
STUS	Siemens Telecom User Board SLIC
STUT	Siemens Telecom User Board Testboard
SYP	Synchronous Port

6 Application and Example

The Babyboard STUS 5509 is used in connection with the SICOFI Testboard STUT 2060 when an analog line card application is tested using HARRIS SLICs HC 5509. To demonstrate its functionality a set-up is given below: The Babyboard is connected to the Testboard via the SLIC connector SLC and configured as described in **chapter 4**. The PCM4 is connected to the Testboard for to measure the transfer functions of the SICOFI and the SLIC. For the connection and programming procedures of the PCM4 refer to the SICOFI Testboard description.

The programming of SICOFI is listed in the SICOFI Application Note "SICOFI PEB 2060 + HARRIS SLIC HC 5509". The byte file (HC5509.byt) is shown in the following **table 1** for the SICOFI Testboard STUT 2060 using the PEB 2060:

Table 1
Byte File to Program the SICOFI®

PSR = 36
CAM00 = 41
CAM20 = 40
CIW0 = 06, 04, 80
CIW0 = 13, 30, BA, EA, 25, 23, 41, C1, BB
CIW0 = 23, 50, C8, B5, 4A, C2, 21, 04, 90
CIW0 = 2B, D0, C8, 84, DC, B1, 93, 02, 1D
CIW0 = 30, A0, 11, 20, 92
CIW0 = 03, C4, 12, 23, 32, 72, B9, B2, BA
CIW0 = 0B, 00, 97, FD, C8, DD, 4C, C2, BC
CIW0 = 18, 19, 19, 11, 19
SIG0 = 20
SIG0 = 60
SIG0 = 20
CIW0 = 25, 00, 18, 04, 78

Switch and Jumpers Settings

Before connecting the Testboard to the PCM4 and SLIC Babyboard respectively, make sure that all jumpers and switches are set correctly.

Testboard: DIL switch 1.1 – 1.4 ON
DIL switch 2.1 – 2.4 ON

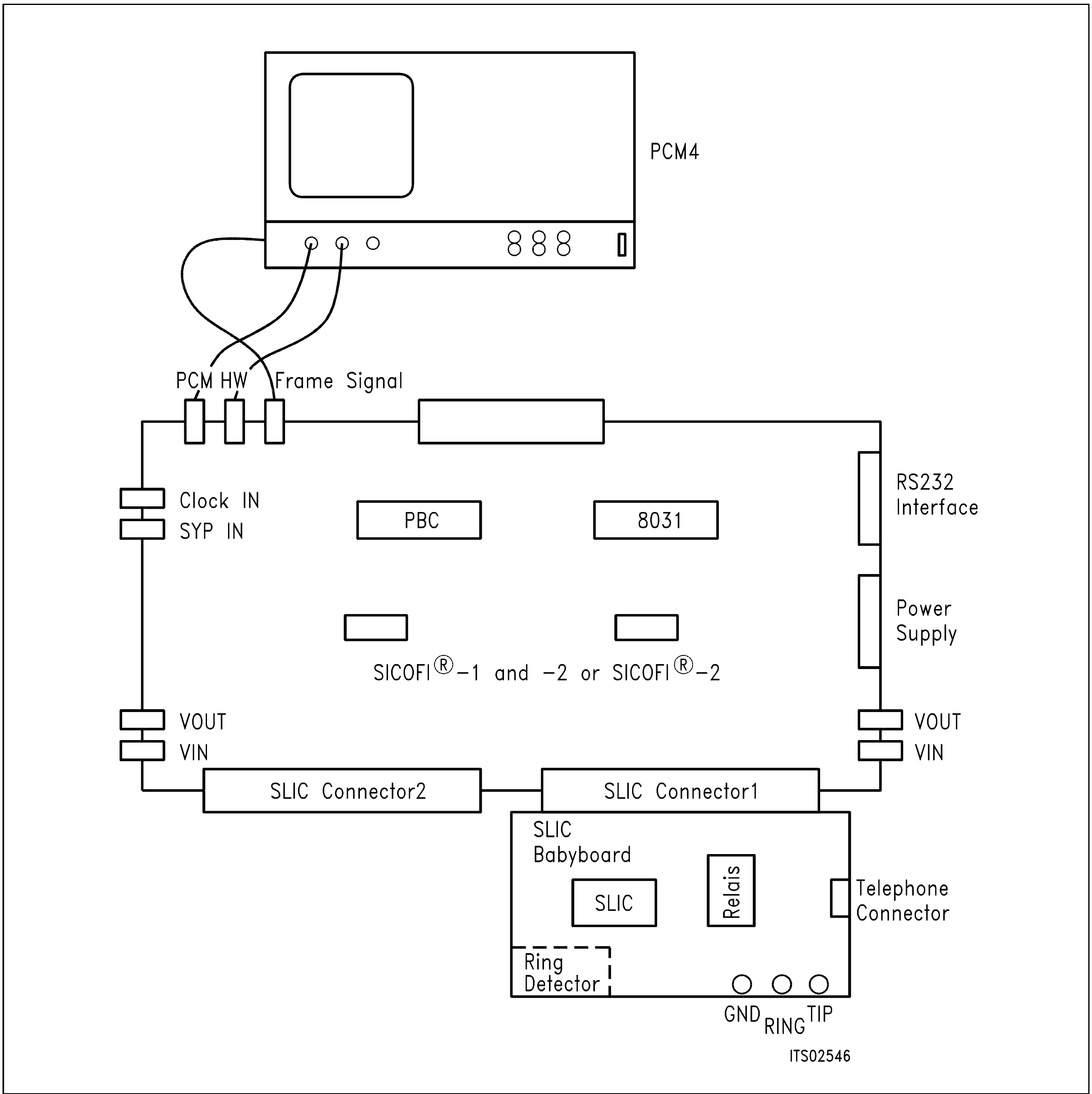


Figure 6
SICOFI® Measurement Set-Up

Required hardware for a measurement set-up:

1	PC IBM AT or compatible
1	PCM4 (Measuring set by Wandel & Goltermann)
1	SICOFI Testboard STUT 2060
1	SLIC Babyboard

Contents **Page**

1 Features

- Performs telephone line interface functions
- Interface to SICOFI Testboard STUT 2060
- Interface to SICOFI-2 Board SIPB 5135
- Analog telephone directly connectable to the SLIC Babyboard
- Ring relay driver provided on board
- Secondary protection circuit on board
- Loop monitoring functions

2 Use

For applications of the ERICSSON SLIC PBL 3736 an ERICSSON SLIC Babyboard has been designed. This Babyboard fits to the SICOFI Testboard STUT 2060.
By means of these two boards, namely the SLIC Babyboard and the SICOFI Testboard, the transfer functions, levels, return loss, transhybrid loss, and other properties of the SLIC linked to the SICOFI can be evaluated. This way test results obtained with the PCM4 Measuring Set and calculations performed by the SICOFI Coefficients Program can be compared. By doing so, the validity of the calculations is checked and errors that might have occurred can be eliminated.

To program the SLIC functions the signaling pins of the SICOFI are connected to the control interface of the ERICSSON SLIC. It is possible to select the modes

power down
power up
ringing

and also to read out the status of the loop current detector and the ring/trip comparator.

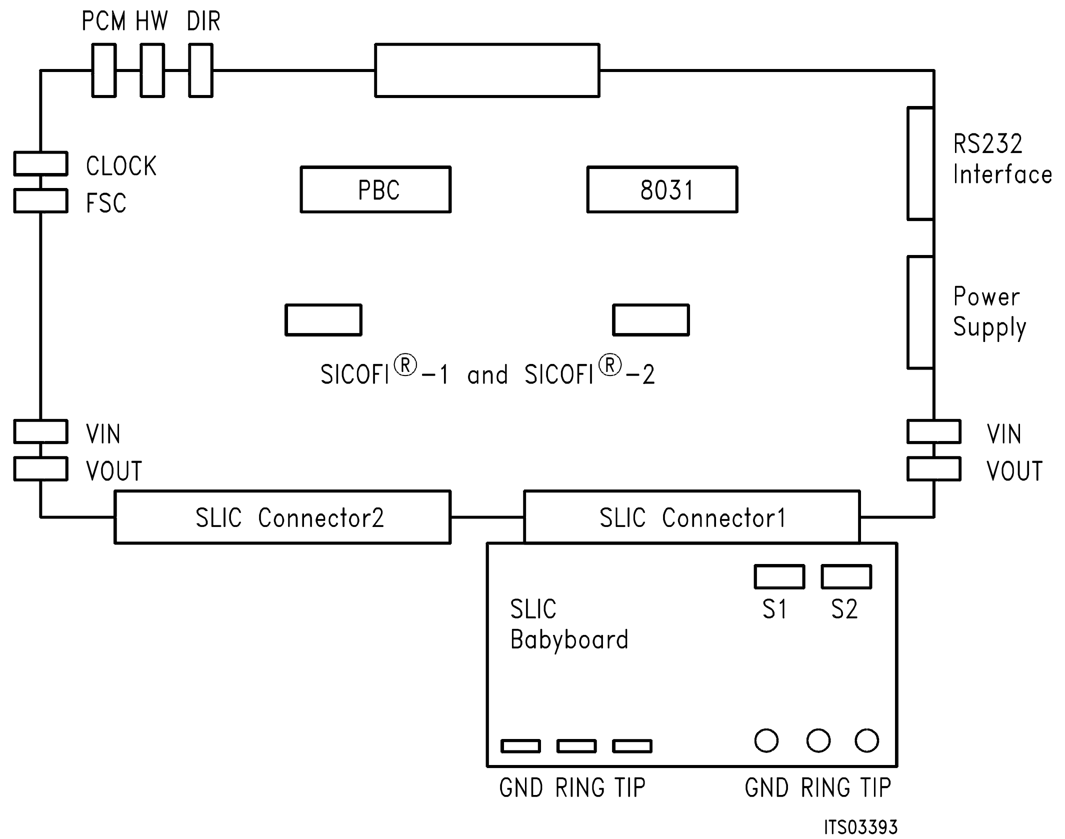


Figure 1
Connecting the SLIC Babyboard to the SICOFI® Testboard

The SLIC Babyboard STUS 3736 must be inserted into one of the SLIC connectors SLC of the SICOFI Testboard STUT 2060. Using a set-up as shown in **figure 1**, the transfer functions of an analog line card can be measured. The programming bytes which have been calculated with the SICOFI Coefficients Program are sent via the RS232 interface to the SICOFI on the testboard.

3 Circuitry

3.1 Block Diagram

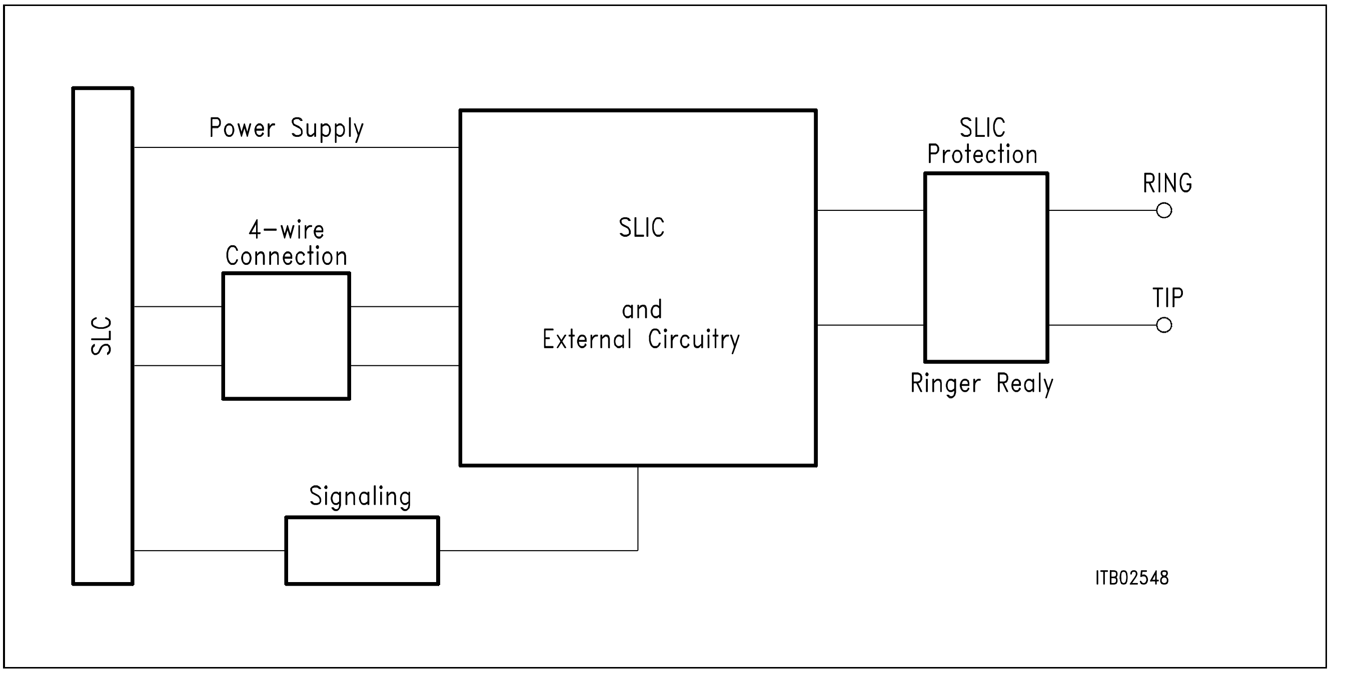


Figure 2
Block diagram of the SLIC Babyboard STUS 3736

In figure 2 the four functional blocks of the SLIC Babyboard are shown:

- SLIC
- Protection circuit
- Signaling
- Ringing

3.1.1 SLIC

The SLIC requires some external components for output impedance matching, echo cancellation, filter completion, and power supply. Some of these functions are already provided by the SICOFI and hence it was possible

a) to reduce the number of extra components and
b) to use one SLIC hardware for two different country specifications.

The SLIC is described in the Application Note "Calculating SLIC Transfer Functions of the ERICSSON SLIC PBL 3736 Using K-Parameters and SPICE".

The SLIC switches the ring relay and provides a digital parallel interface to control the SLIC modes. These different modes are

power-down (stand-by state: the loop current is reduced to 1.5 times the loop current detector threshold)

conversation (normal state: signal transmission is normal)
ringing (the ring relay driver is activated).

3.1.2 Protection Circuit

The protection circuit screens the SLIC against high voltages (secondary protection). This is realized by 4 diodes D2 ... D5 and the fuse resistors RF1 and RF2 for energy dissipation. No primary protection, however, e.g. by surge arrestors, is provided.

3.1.3 Signaling

The signaling lines connect the SICOFI signaling interface to the digital SLIC interface (Pins E_0, C_1, C_2, C_3, DET). Via these pins the SICOFI switches the SLIC into one of the three possible modes (power-up, power-down, and ringing). The SLIC performs two different loop monitoring functions, namely loop current detection and ring/trip status detection. The respective detectors report their status through the SLIC output pin DET (pin 13) and thus provide the corresponding information about the loop current or ring/trip status to the SICOFI. The DET output is enabled by the "read enable pin" E_0. A logic HIGH enables the DET pin, a logic LOW disables the DET output. If you want to get information about the loop functions of the SLIC, you have to program the SICOFI with the signaling byte so that the E_0 pin is set to a logic HIGH. Examples are given in chapters 4.2.1 "Mode Select for STUT 2060" and 4.2.2 "Mode Select for SIPB 5135" respectively.

The actual state of operation of the SLIC determines which monitoring function is provided by the DET output, e.g. in the normal state the DET pin provides the loop current status.

For programming the SLIC the configuration registers 1 and 2 of the SICOFI have to be defined correctly in order to match the controlling pins of the SLIC to the signaling pins of the SICOFI. The pins C_3, C_2, C_1, DET, and E_0 of the SLIC are connected to the SICOFI pins SO1, SO2, SA, SI1 and SO3. When the SICOFI is in the SLD mode the signaling byte puts the SLIC to the desired status; being in the IOM mode, the Command/Indicate byte sets the operating state.

3.1.4 Power Supply

Power is supplied to the SLIC via the SLIC connector SLC. A relay switches the ringing voltage from the SLC to the a/b-line.

3.2 Connector Pin-Outs

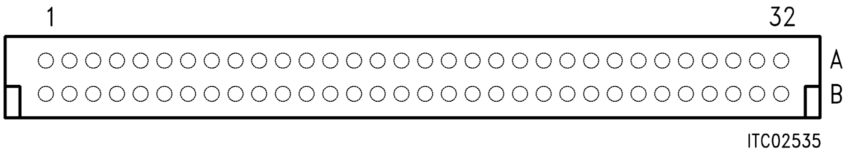


Figure 3
SLIC Connector SLC

Note 1: Pins not mentioned are not connected
Note 2: The pin numbering in the list below refers to the numbering on the SICOFI Testboard

Pin	Row	Function	Signal	Meaning
7	A	I	SCLK	Clock
12	A	I	GND	Power supply
13	A	I	+ 5 V	Power supply
14	A	I	65 V AC	Ringer power supply 65 V AC
15	A	I	– 5 V	Power supply
16	A	I	Reset	Reset
19	A	I	– 48 V	Power supply
21	A	I	SO1	C3
22	A	I	SO2	C2
23	A	I	SO3	E0
24	A	O	SI1	/DET
25	A	O	+ 5 V	SI2
26	A	O	+ 5 V	SI3
28	A	I	AGND	Analog ground
29	A	O	VIN	4 wire analog output
30	A	I	AGND	Analog ground
31	A	I	VOUT	4 wire analog input
32	A	I	AGND	Analog ground
21	C	O	SA	C1

3.3 Wiring Diagram

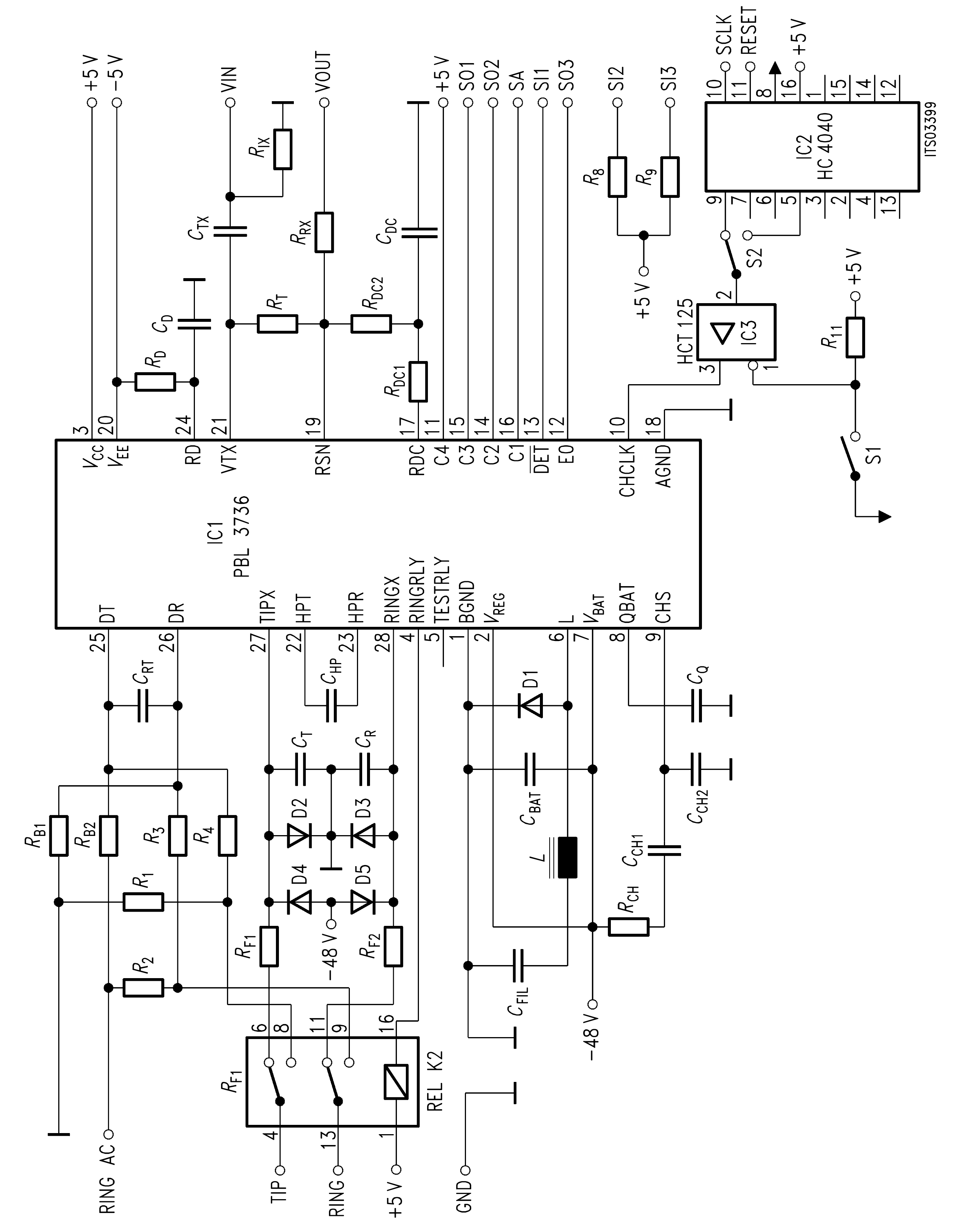


Figure 4
Wiring Diagram

3.4 List of Replaceable Parts

Component	Type/Value
IC1	PBL 3736
IC2	HC4040
IC3	HCT125
D1	1N4448
D2, D3, D4, D5	BAV 19
C_D	10 nF
C_{DC}	150 nF
C_{HP}, C_{RT}	220 nF
C_{CH1}	47 nF
C_{CH2}	560 pF
C_T, C_R	2.2 nF
C_{BAT}, C_Q	330 nF
C_{FIL}	470 nF
C_{TX}	1 µF
R_1, R_2	390 R
R_3, R_4	205 kΩ
R_8, R_9, R_{11}	10 kΩ
R_D	51.1 kΩ
R_{DC1}, R_{DC2}	20 kΩ
R_T	560 kΩ
R_{IX}	22 kΩ
R_{F1}, R_{F2}	20 R
R_{CH}	680 R
R_{B1}, R_{B2}	249 kΩ
R_{RX}	300 kΩ
K1	Relay 5 V

3.5 Floor Plan

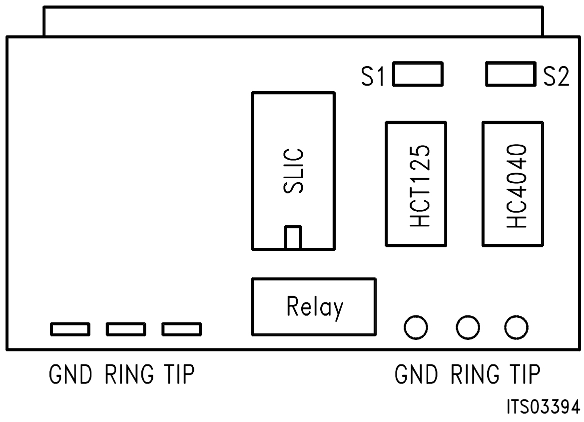


Figure 5
Floor plan of the STUS 3736 Babyboard

4 Operational Information

4.1 Configuration

Before power is applied, the SLIC Babyboard has to be configured by means of DIP switches S1 and S2.

Possible configurations are:

– Switch S1 for the HCT125
  Switched to the left side (away from switch S2) the HCT 125 puts through the signal from the frequency divider HC4040 to the clock input of the SLIC.
  Switched to the right side, the driver is switched OFF.

– Switch S2 for the HC4040
  Switched to the left side (towards switch S1) the 512 kHz clock frequency coming from the SICOFI is divided by two. Thus the SLIC is provided with the nominal frequency of 256 kHz. In case the SICOFI is in the IOM-2 mode and provides a frequency of 4096 kHz, the switch has to be in the right position (away from switch S1). The 4096 kHz frequency from the SICOFI then is divided down to 256 kHz.

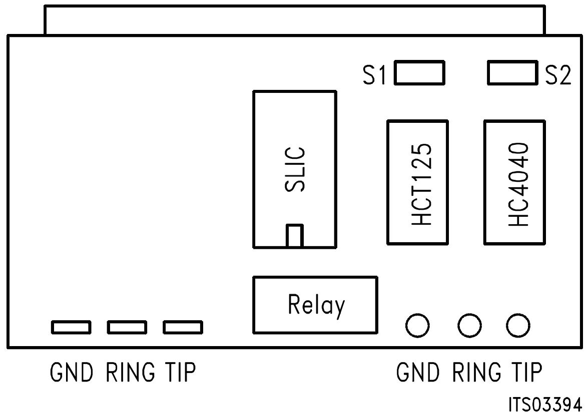


Figure 6
SLIC Babyboard with the switches S1 and S2

SIG0 = 20	Open-circuit state: The TIPX and the RINGX power amplifier present a high impedance to the line; loop current detector not active.
SIG0 = 22	Ringing state: Ring relay driver activated, ring trip detector is connected to the detector output (/DET), TIPX and RINGX are in the high-impedance state, and signal transmission is inhibited.
SIG0 = 60	Normal state: TIPX is the terminal closest to GND and sources loop current; signal transmission is normal, loop current detector is ON.
SIG0 = 62	Stand-by state: The loop current is limited to 1.5 times the loop current detector threshold current, loop current detector is ON.
SIG0 = A0	TIPX open-circuit state: The TIPX power amplifier presents a high impedance to the line, loop current detector is ON.
SIG0 = E0	Polarity reversal state: TIPX and RINGX polarity is reversed compared to normal state: RINGX is closest to GND and sources current, TIPX sinks current, loop current detector is ON, signal transmission is normal.
SIG0 = C2	Polarity reversal and stand-by state: See above.

Following byte sequences apply to the STUT 2060 using the **PEB 2260** for both channels:

SIG0 = 44	Open-circuit state
SIG0 = CC	Ringing state
SIG0 = 66	Normal state
SIG0 = EE	Stand-by state
SIG0 = 55	TIPX open-circuit state
SIG0 = 77	Polarity reversal state
SIG0 = FF	Polarity reversal and stand-by state.

4.2 Mode Select for SIPB 5135

The following byte sequences apply to the SIPB 5135 using the **PEB 2260** for programming channel A. For programming channel B one has to add 80hex to the C/I commands listed below. E.g. for putting the SLIC to channel B in the normal state, the command would be:

C/I = CB ($4B_H$ + 80_H).

C/I = 43 Open-circuit state
C/I = 53 Ringing state
C/I = 4B Normal state
C/I = 5B Stand-by state
C/I = 47 TIPX open-circuit state
C/I = 4F Polarity reversal state
C/I = 5F Polarity reversal and stand-by state

When the SICOFI-2 Board output C3A is a detection select output, then the loop and ground key information are available from the SICOFI-2 Board.

5 Application and Example

The Babyboard STUS 3736 is used in connection with the SICOFI Testboard STUT 2060 when an analog line card application is tested using the ERICSSON SLIC PBL 3736. To demonstrate its functionality, a set-up is given below: The Babyboard is connected to the Testboard via the SLIC connector SLC and configured as described in section 4. The PCM4 is connected to the Testboard to measure the transfer functions of the SICOFI and the SLIC. For the connection and programming procedures of the PCM4 refer to the SICOFI Testboard description.

The programming of SICOFI is listed in the SICOFI Application Note "Calculating SLIC Transfer Functions of the ERICSSON SLIC PBL 3736 Using K-Parameters and SPICE". The byte file for the SICOFI Testboard STUT 2060 using the PEB 2060 is shown below in table 1:

Table 1
Byte File to Program the SICOFI® PEB 2060

PSR = 36
CAM00 = 41
CAM20 = 40
CIW0 = 26, 04, 80
CIW0 = 13, 30, FA, BA, 52, 14, C2, B1, 2C
CIW0 = 23, F0, 19, 87, FB, 19, E5, 0A, B5
CIW0 = 2B, F0, 19, 87, FC, 29, 16, 00, BD
CIW0 = 03, 4B, 2B, 23, AB, B6, 19, BB, 23
CIW0 = 0B, 00, 35, C1, 32, 24, 65, 2B, AB
CIW0 = 18, 19, 19, 11, 19
CIW0 = 30, 41, B2, 00, 23
CIW0 = 25, 00, 08, 04, 78
SIG0 = 60

Switch Settings

Before connecting the testboard to the PCM4 measuring set and SLIC Babyboard respectively, make sure that all switches are set correctly.

Testboard: DIL switch 1.1 – 1.4 ON
DIL switch 2.1 – 2.4 ON

Babyboard: S1 in left position (away from switch S2, **see figure 6**)
S2 in left position (towards switch S1, **see figure 6**)

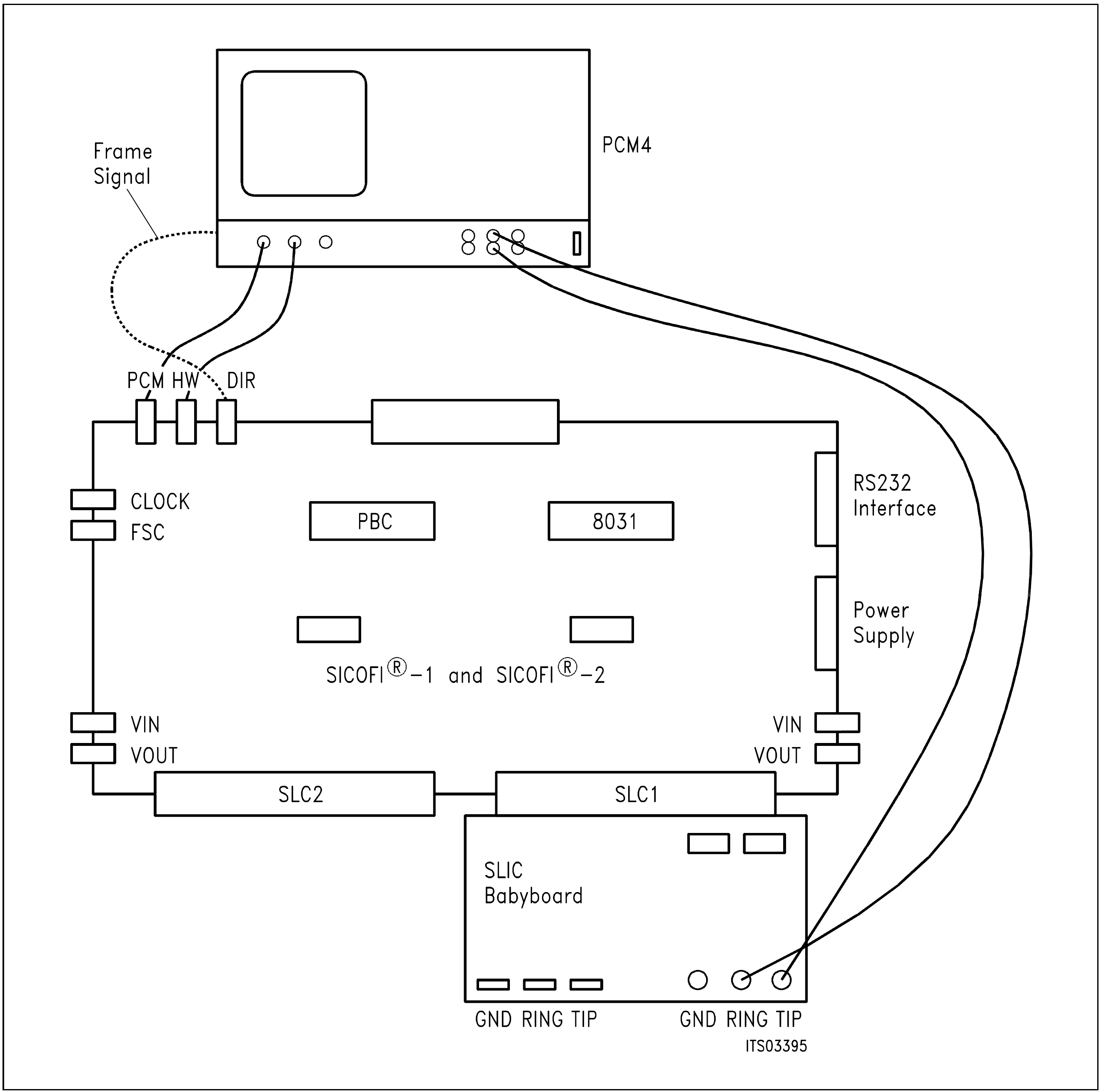


Figure 7
SICOFI® Measurement Set-Up

Required hardware for a measurement set-up:

1	PC IBM AT or equivalent
1	PCM4 (Measuring set by Wandel & Goltermann)
1	SICOFI Testboard STUT 2060
1	SLIC Babyboard

SLIC Babyboard STUS 3762 for ERICSSON SLIC PBL 3762/64

Contents **Page**

1 Features

- Interface to SICOFI Testboard STUT 2060
- Interface to SICOFI-2 Module SIPB 5135
- ERICSSON SLIC PBL 3762 or PBL 3764 to be used on board
- Analog telephone directly connectable
- Ring relay on board
- Secondary protection circuit on board

2 Use

For one of our SLIC-applications a ERICSSON SLIC Babyboard has been designed in order to connect it with the SICOFI Testboard STUT 2060.

With both boards it is possible to measure the transfer functions of the ERICSSON SLICs PBL 3762 or PBL 3764 together with the SICOFI and to check the calculations done with SICOFI coefficients program.

The signaling pins of SICOFI are connected with the control interface of the ERICSSON SLIC to control the SLIC functions. Therefore it is possible to select the modes

power down
power up
ringing

and to read out the status of

hook switch (OFF or ON),
ring/tip, and
ground-key.

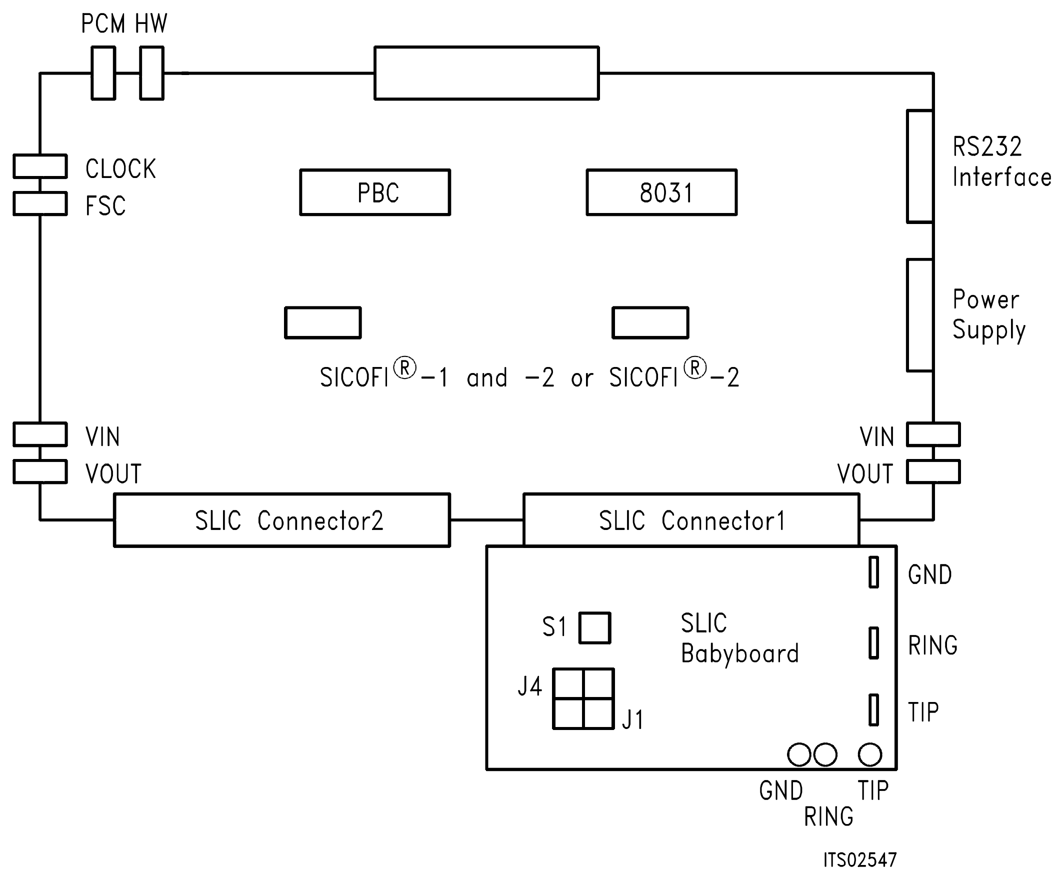


Figure 1
Connecting the SLIC Babyboard to the SICOFI® Testboard

For practical use the SLIC Babyboard STUS 3762 is inserted into one of the SLIC connectors SLC of the SICOFI Testboard STUT 2060. Using a set-up like that shown in **figure 1**, the transfer functions of an analog line card can be established. For programming, the Byte File is used which is to be found in the ERICSSON SLIC PBL 3762/64 Application Note.

3 Circuitry

3.1 Block Diagram

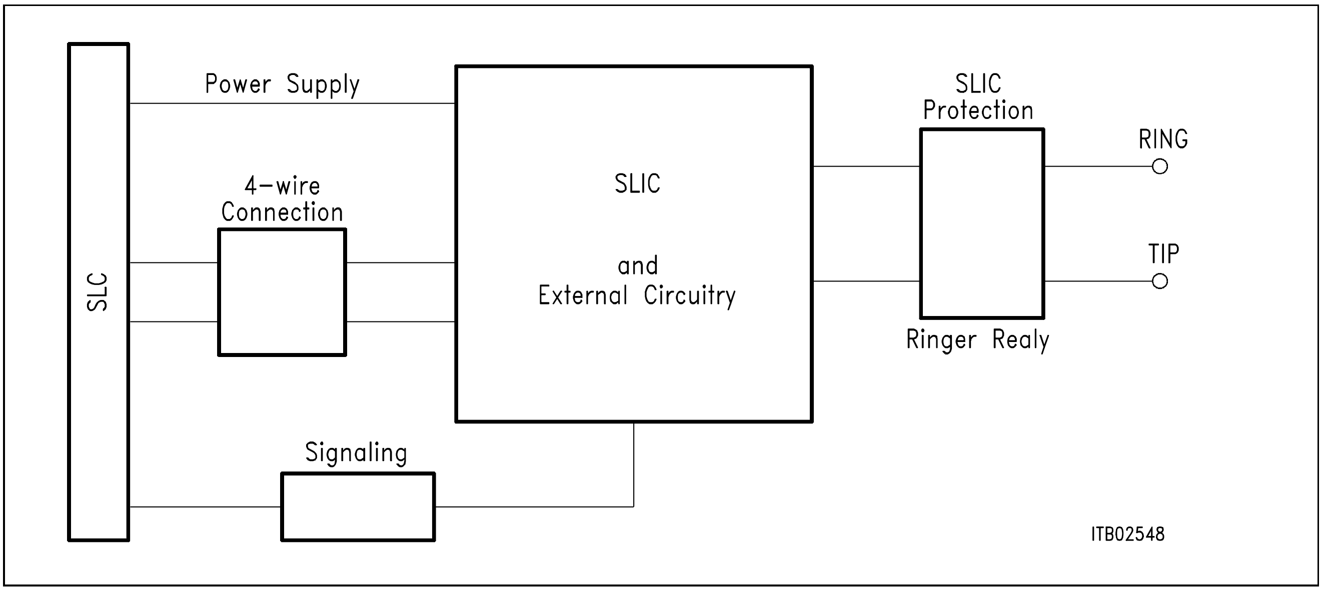


Figure 2
Block Diagram of the SLIC Babyboard STUS 3762

In **figure 2** the five functional blocks of the SLIC Babyboard are shown:

- SLIC
- Protection circuit
- Signaling
- Ringing

3.1.1 SLIC

The PBL 3762 and PBL 3764 SLICs are pin and software compatible the only difference being, that the PBL 3762 has resistive feeding and the PBL 3764 has constant current feeding. Thus both may be used with the SLIC Babyboard STUS 3762.

The SLIC requires some external components for output impedance, echo cancellation, filter capacitors, and power supply. Some of these functions are realized by the SICOFI and hence it was possible to reduce the number of extra components.

The description of the SLIC is to be found in the pertinent Application Note. The SLIC switches the ringer relay and provides a digital parallel interface to control the SLIC modes. These modes are

– power down

– conversation (active)

– ringing.

3.1.2 Protection Circuit

The protection circuit screens the SLIC against high voltages (secondary protection). This is realized by 4 diodes D3 ... D6 and the fuse resistors R_{F1} and R_{F2}. No primary protection, however, e.g. surge arristors, is provided.

3.1.3 Signaling

The signaling lines connect the SICOFI signaling interface to the digital SLIC interface. The SICOFI switches the SLIC into one of the three possible modes and the SLIC provides the corresponding information of the loop status (ground key or on/OFF-hook) for the SICOFI. When the SICOFI-2 is used in the IOM-2 mode, the SLIC sends both information (ground-key and loop status) with the detection select output enabled. In this case the SICOFI-2 changes the logic level at the output C3A every 250 µsec. Depending on the logic level at the C3A output of the SICOFI-2, the SLIC transmits the ground-key or loop status to a SICOFI-2 input (I1A). The detector output switches the loop information to the signaling bit I1x, and the ground-key information to bit CI1x of the C/I-channel.

3.1.4 Power Supply

Power is supplied to the SLIC via the SLIC connector SLC. A relay switches the ringing voltage from the SLC to the a/b-line.

3.2 Connector Pin-Outs

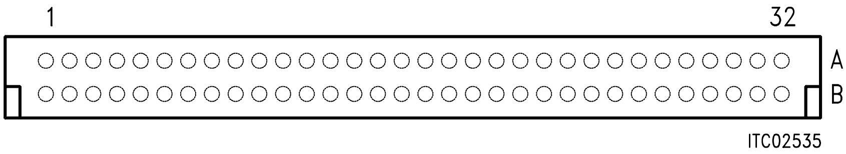


Figure 3
SLIC Connector SLC

Note: Pins not mentioned are not connected

Pin	Row	Function	Signal	Meaning
12	A	I	GND	Power supply
13	A	I	+ 5 V	Power supply
14	A	I	65 V AC	Ringer power supply 65 V AC
15	A	I	– 5 V	Power supply
19	A	I	– 48 V	Power supply
21	A	I	SO1	C2
22	A	I	SO2	C1
23	A	I	SO3	E1
24	A	O	SI1	/DET
26	A	I	DGND	Digital ground
28	A	I	AGND	Analog ground
29	A	O	VIN	4-wire analog output
30	A	I	AGND	Analog ground
31	A	I	VOUT	4-wire analog input
32	A	I	AGND	Analog ground
21	C	O	SA	E0

3.3 Wiring Diagram

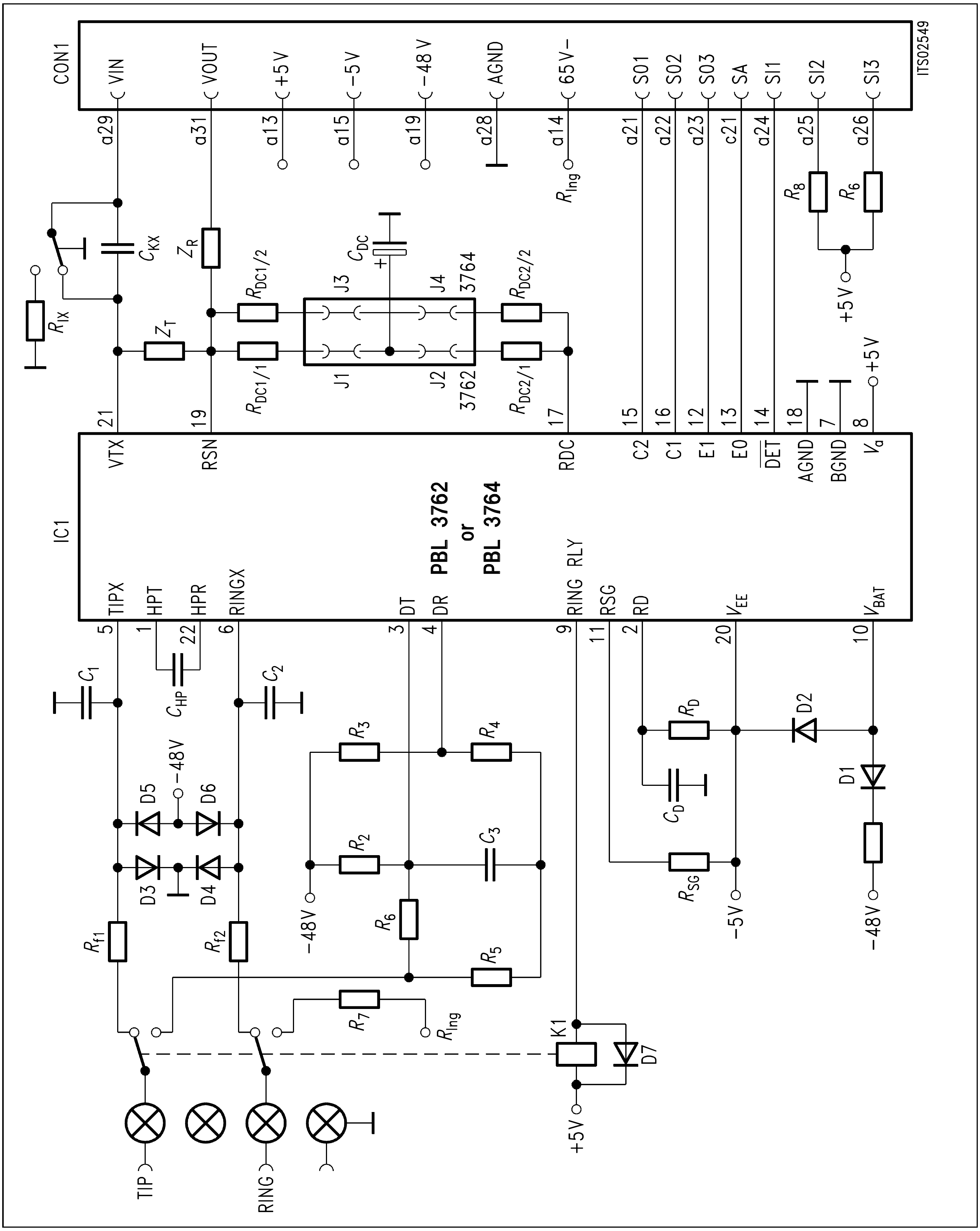


Figure 4
Wiring Diagram

3.4 List of Replaceable Parts

Component	Type/Value
IC1	PBL 3762 or PBL 3764
D1, D7	1N4007
D2	1N4148
D3, D4, D5, D6	BAY 45
C_1, C_2	2.2 nF/100 V
C_3	330 nF/100 V
C_{kx}	1 µF
C_D	15 nF/100 V
C_{DC}	3.3 nF/10 V
C_{HP}	33 nF/100 V
R_1	5.6 Ω
R_2	1.2 MΩ
R_3	910 kΩ
R_4	200 kΩ
R_5	150 Ω/2 W
R_6	200 kΩ
R_7	0 Ω
R_8, R_9	4.7 kΩ
R_D	39 kΩ
$R_{DC1/1}$	20 kΩ
$R_{DC2/1}$	20 kΩ
$R_{DC1/2}$	41.2 kΩ
$R_{DC2/2}$	41.2 kΩ
Z_T	598 kΩ
Z_R	300 kΩ
R_{ix}	24 kΩ
R_{SG}	20 kΩ
R_{F1}, R_{F2}	20 Ω
K1	Relay 5 V

3.5 Floor Plan

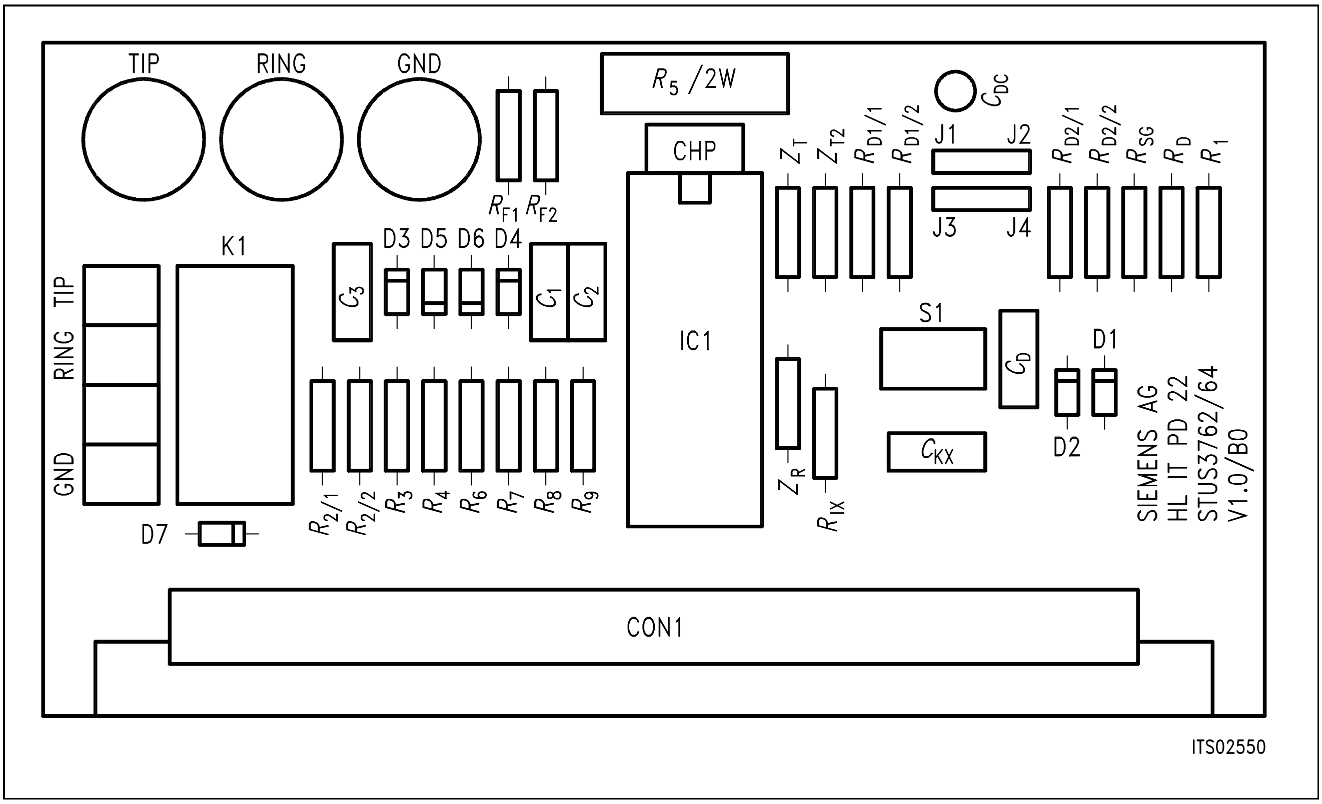


Figure 5
Floor Plan of the STUS 3762 Babyboard

4 Operational Information

4.1 Configuration

Before power is applied, the SLIC Babyboard has to be configured by means of DIP switch S1 and setting the jumpers J1 ... J4.
Possible configurations are:

– with or without blocking capacitor in transmit direction

– selecting the R_{DC} resistors for PBL 3762 or PBL 3764

The Babyboard contains four jumpers J1 ... J4 to select the R_{DC} resistors for the PBL 3762 (20 kΩ: J1, J2 set) or for the PBL 3764 (41.2 kΩ: J3, J4 set) respectively.

DIP Switch S1 selects the blocking capacitor in transmit direction at the SLIC 4-wire side. When switch S1 points towards the SLIC, then the capacitor is inserted. The capacitor is shunted out, when S1 is at the distant side (**see figure 6**).

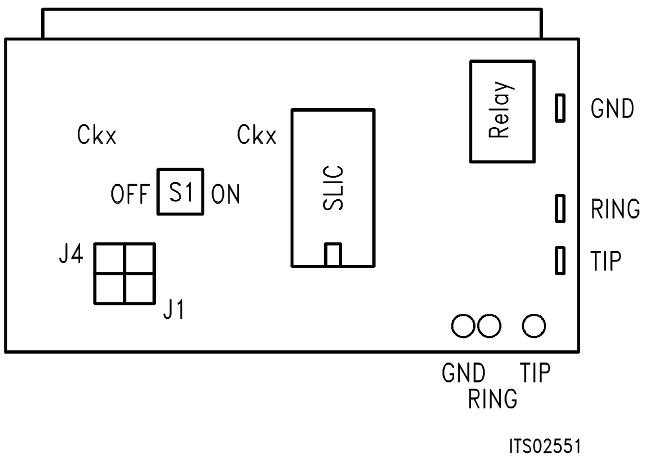


Figure 6
SLIC Babyboard and Switch S1

4.2 Mode Select

The actual modes of the ERICSSON SLICs PBL 3762 or PBL 3764 are selected by the digital interface. This interface is connected to the signaling pins of the SICOFI. The signaling commands are different for the SICOFI Testboard STUT 2060 and for the SICOFI-2 Board SIPB 5135.

4.2.1 Mode Select for STUT 2060

Mode selection differs for the Testboard STUT 2060 being equipped with the SICOFI PEB 2060 or with the SICOFI-2 PEB 2260.

Following byte sequences apply to the STUT 2060 using the **PEB 2060**:

SIG0 = E0	stand-by, loop current detector ON
SIG0 = C0	stand-by, ground key detector ON
SIG0 = A0	active, loop current detector ON
SIG0 = 80	active, ground key detector ON
SIG0 = 60	ringing, ring/tip detector ON

The line status (OFF-hook/ground-key), which is selected by the above signaling, can be read out via the SICOFI SIP-line:

SIG0: 80	ON-hook or ground key detection

Following byte sequences apply to the STUT 2060 using the **PEB 2260** for both channels:

SIG0 = 77	stand-by, loop current detector ON
SIG0 = 33	stand-by, ground key detector ON
SIG0 = 55	active, loop current detector ON
SIG0 = 11	active, ground key detector ON
SIG0 = 66	ringing, ring/tip detector ON

The line status (OFF-hook/ground-key), which is selected in the above signaling, can be read out via the SICOFI SIP-line.

SIG0: 11	ON-hook or ground-key detection

4.2.2 Mode Select for SIPB 5135

Following byte sequences apply to the SIPB 5135 using the **PEB 2260** channel A (channel B = + 80$_H$):

C/I = 4F	stand-by, loop current detector ON
C/I = 0F	stand-by, ground key detector ON
C/I = 47	active, loop current detector ON
C/I = 07	active, ground key detector ON
C/I = 4B	ringing, ring/tip detector ON

When the SICOFI-2 Board output C3A is a detection select output, then the loop and ground key information are available from the SICOFI-2 Board:

C/I = DB	loop detection OFF-hook, ground key is pushed
C/I = 93	loop detection ON-hook, ground key is pushed
C/I = FF	loop detection OFF-hook, ground key not found
C/I = B7	loop detection ON-hook, ground key not found

5 Glossary

DIR	Direction signal (same as FSC)
FSC	Frame Synchronization Clock
PC	Personal Computer
PCM	Pulse Code Modulation
SICOFI	SIgnal processing COdec FIlter
SIG	SIGnaling byte at the SIP-line
SIP	Serial Interface Port
SIPB	Siemens ISDN PC User Board (system)
SLD	Subscriber Line Data
STUS	Siemens Telecom User Board SLIC
STUT	Siemens Telecom User Board Testboard

6 Application and Example

The Babyboard STUS 3762 is used in connection with the SICOFI Testboard STUT 2060 when an analog line card application is tested using ERICSSON SLICs PBL 3762/64. To demonstrate its functionality a set-up is given below: The Babyboard is connected to the Testboard via the SLIC connector SLC and configured as described in **chapter 4**. The PCM4 is connected to the Testboard to measure the transfer functions of the SICOFI and the SLIC. For the connection and programming procedures of the PCM4 refer to the SICOFI Testboard description.

The programming of SICOFI is listed in the SICOFI Application Note "SICOFI PEB 2060 + ERICSSON SLIC PBL 3762". The byte file (PBL3762.BYT) is shown in the following **table 1** for the SICOFI Testboard STUT 2060 using the PEB 2060:

Table 1
Byte File to Program the SICOFI®

PSR = 36
CAM00 = 41
CAM20 = 40
CIW0 = 06, F4, 80
CIW0 = 13, 30, 22, 2A, 6B, 2B, 22, B3, 22
CIW0 = 23, F0, BC, 37, 72, 49, 36, 0F, A6
CIW0 = 2B, F0, 2B, 97, 74, 2A, 27, 02, CE
CIW0 = 30, 61, B1, 00, B4
CIW0 = 03, 35, 12, 52, 91, BE, F9, A9, F4
CIW0 = 0B, 00, 33, AB, 23, 32, 73, 39, FA
CIW0 = 18, 19, 19, 11, 19
CIW0 = 26, F4, 78
SIG0 = A0

Switch and Jumpers Settings

Before connecting the Testboard to the PCM4 and SLIC Babyboard respectively, make sure that all jumpers and switches are set correctly.

Testboard:	DIL switch 1.1–1.4 ON	
	DIL switch 2.1–2.4 ON	
Babyboard:	PBL 3762 being used	J1, J2 is CLOSED, J3, J4 is OPEN
	PBL 3764 being used	J1, J2 is OPEN, J3, J4 is CLOSED
	Capacitor C_{Kx} is enabled	S1 in position right (**figure 6**)
	Capacitor C_{Kx} is shorted	S1 in position left (**figure 6**)

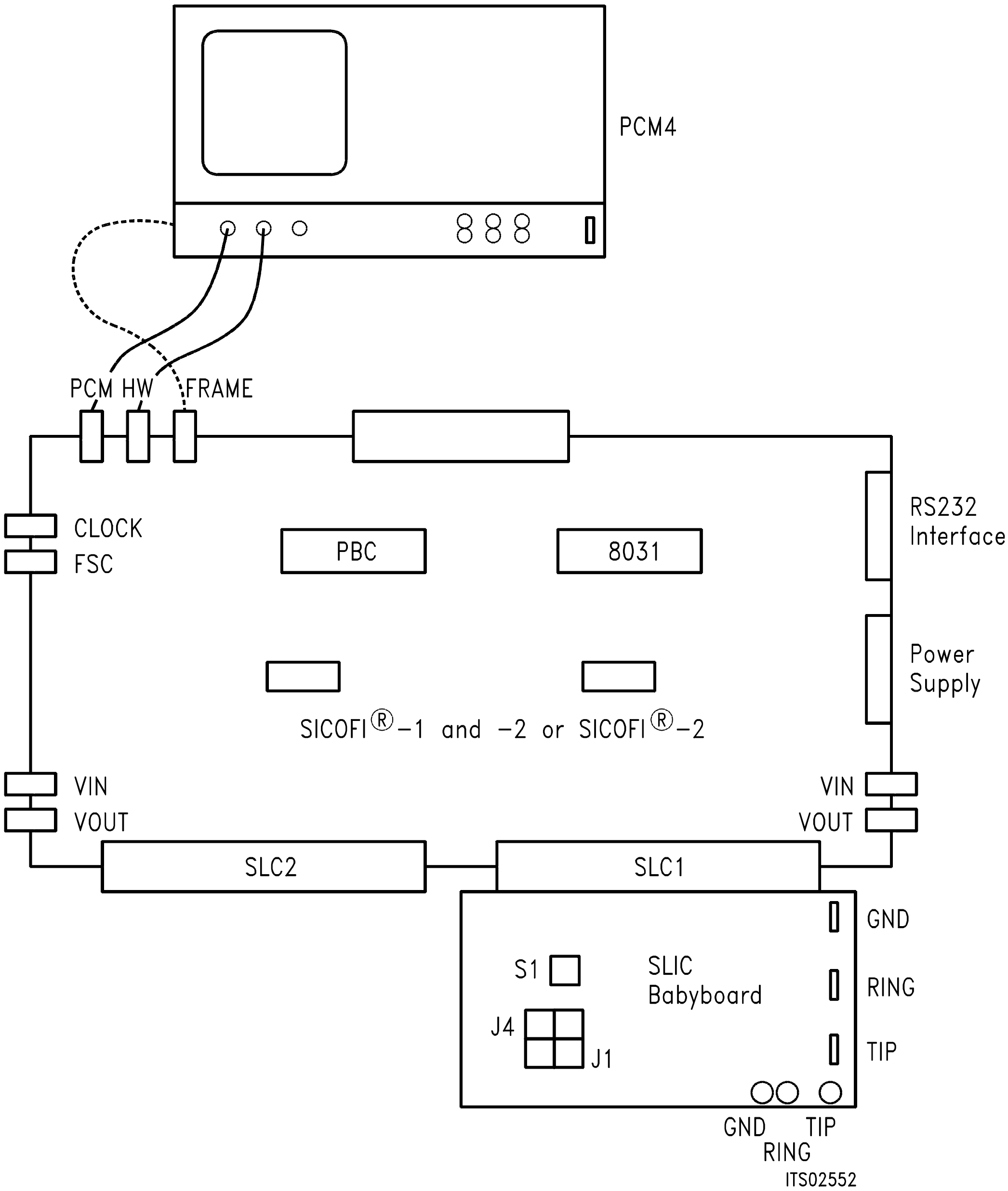


Figure 7
SICOFI® Measurement Set-Up

Required hardware for a measurement set-up:

1	PC IBM AT or compatible
1	PCM4 (Measuring set of Wandel & Goltermann)
1	SICOFI Testboard STUT 2060
1	SLIC Babyboard

SLIC Babyboard STUS 3030 for STM SLIC L3000/L3030

Contents **Page**

1 Features

- Interface to SICOFI Testboard STUT 2060
- Interface to SICOFI-2 Board SIPB 5135
- Serial or parallel interface selectable
- 4-wire side of the SLIC selectable for internal or external measurements
- Analog telephone directly connectable
- External battery supply of + 72 V can be connected via banana plugs

2 Use

For one of our SLIC-applications a SGS-THOMSON SLIC Babyboard has been designed in order to connect it with the SICOFI Testboard STUT 2060. With both boards it is possible to measure the transfer functions of the SGS-THOMSON SLIC L3000/L3030 together with the SICOFI and to check the calculations done with SICOFI coefficients program.
The switches S1 and S2 select the 4-wire side of the SLIC. The control interface of the L3030 is connected to the SLD line via external hardware to control the SLIC functions (serial interface). Therefore it is possible to select the modes

power down
power up
ringing
current on the a/b-line

and to read out the status of

hook switch (OFF or ON),
ground-key.

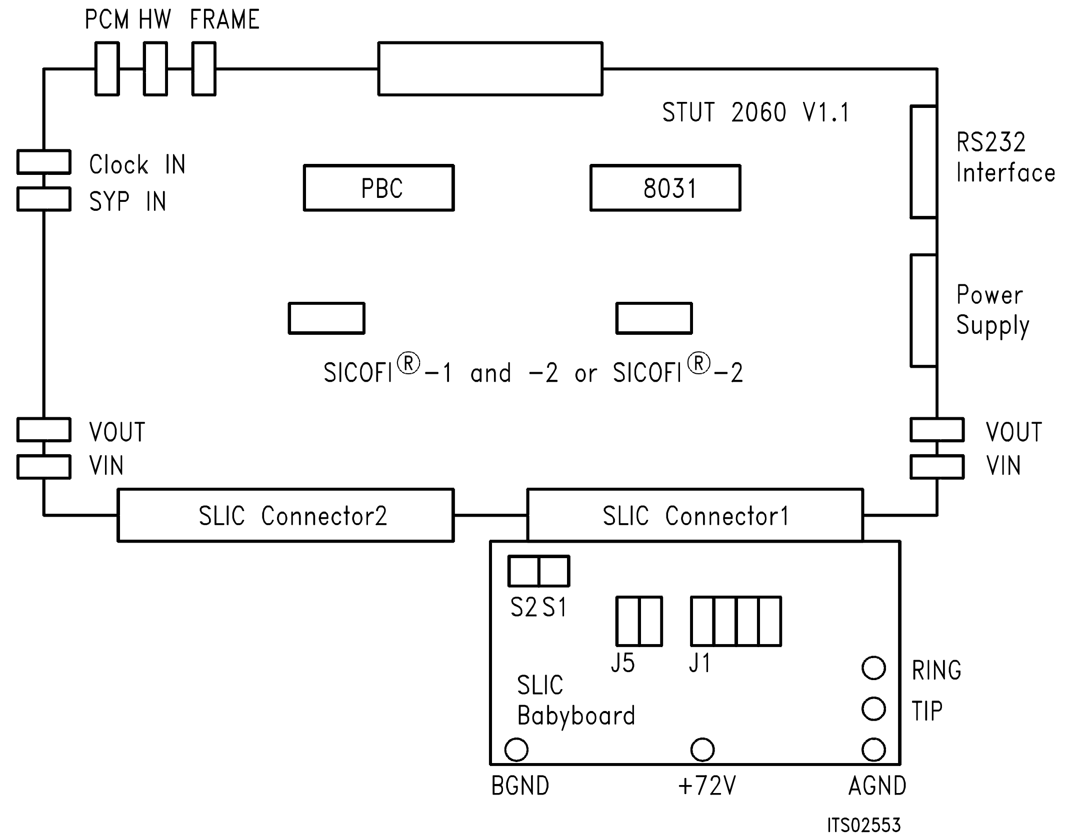


Figure 1
Connecting the SLIC Babyboard to the SICOFI® Testboard

For practical use the SLIC Babyboard STUS 3030 is inserted into one of the SLIC connectors SLC of the SICOFI Testboard STUT 2060. Using a set-up like that shown in **figure 1**, the transfer functions of an analog line card can be established. For programming, the Byte File is used which is to be found in the SGS-THOMSON L3030 Application Note.

3 Circuitry

3.1 Block Diagram

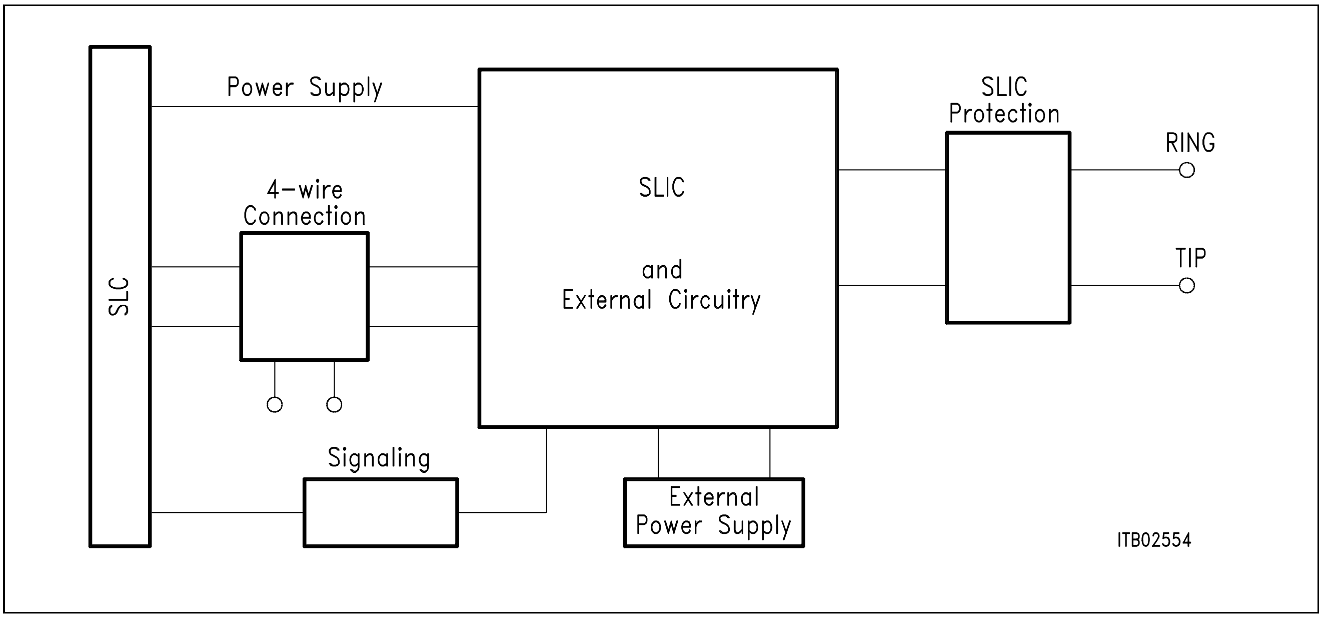


Figure 2
Block Diagram of the SLIC Babyboard STUS 3030

In **figure 2** the five functional blocks of the SLIC Babyboard are shown:

– SLIC
– Protection circuit
– Signaling
– External power supply
– 4-wire connection

3.1.1 SLIC

The SLIC is divided into two parts, a low voltage part (L3030) and a high voltage part (L3000). The high voltage part is connected to the line. It realizes the battery feeding and switches the ringing and the speech signals in both directions through the SLIC. The line current is programmable to 4 threshold values (25 mA, 30 mA, 45 mA, and 70 mA). An internal temperature sensing part shuts the line current off, when the temperature threshold is exceeded. The ringing signal is supplied by the battery on a small AC control-voltage (0.285 Vrms). The ringing signal starts and stops when the control signal crosses zero. The maximum time to switch-on the ringing signal is 1 s. The control signal is amplified and fed in balanced mode to the line with a superimposed DC voltage of 22 V.

The low voltage part synthesizes the DC characteristics. Echo cancellation is performed by controlling the output impedance. As several of these functions are already realized by the SICOFI it was possible to reduce the number of external components.

The L3030 contains a digital interface to control the SLIC modes. These modes are

– power down
– conversation (active)
– ringing.

The L3030 contains also a capacitor multiplier. It is selected via a resistor. If used the multiplier simulated a big capacitance from two little ones. These do not require as much space and are less expensive.

3.1.2 Protection Circuit

The protection circuit screens the SLIC against high voltages (e.g. lightnings). This is realized by 2 protection circuits L3121 from SGS-THOMSON and several diodes. These circuits apply to the a/b-lines.

3.1.3 Signaling

Being in the serial interface mode the control interface of the SLIC is connected to the SLD-line via external hardware. Information from and to the SLIC are sent in the signaling byte of the SIP-line. The external hardware is synchronized by a PBC.
Working in the parallel interface mode the SLIC gets signaling from the SICOFI signaling pins.

3.1.4 Power Supply

Power is supplied to the SLIC via the SLIC connector SLC. Only for battery voltage supply of + 72 V in some special applications an external power source is required.

3.1.5 4-Wire Selection

Two switches S1 and S2 select the 4-wire connection for to measure the SLIC functions exclusively or in combination with the SICOFI.

3.2 Connector Pin-Outs

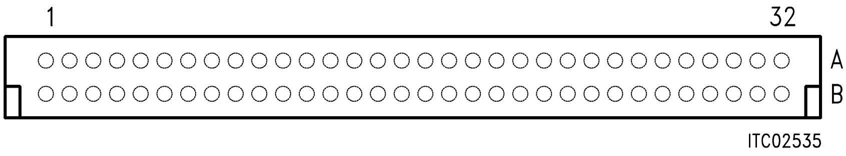


Figure 3
SLIC Connector SLC

Note: Pins not mentioned are not connected

Pin	Row	Function	Signal	Meaning
12	A	I	GND	Digital ground
13	A	I	+ 5 V	Power supply
15	A	I	– 5 V	Power supply
19	A	I	– 48 V	Power supply
21	A	I	SO1	Power down
22	A	I	SO2	Timing
23	A	I	SO3	Ring
24	A	O	SI1	Ground key
25	A	O	SI2	/GKD
28	A	I	AGND	Analog ground
29	A	O	VIN	4-wire analog output
30	A	I	AGND	Analog ground
31	A	I	VOUT	4-wire analog input
32	A	I	AGND	Analog ground

3.3 Wiring Diagram

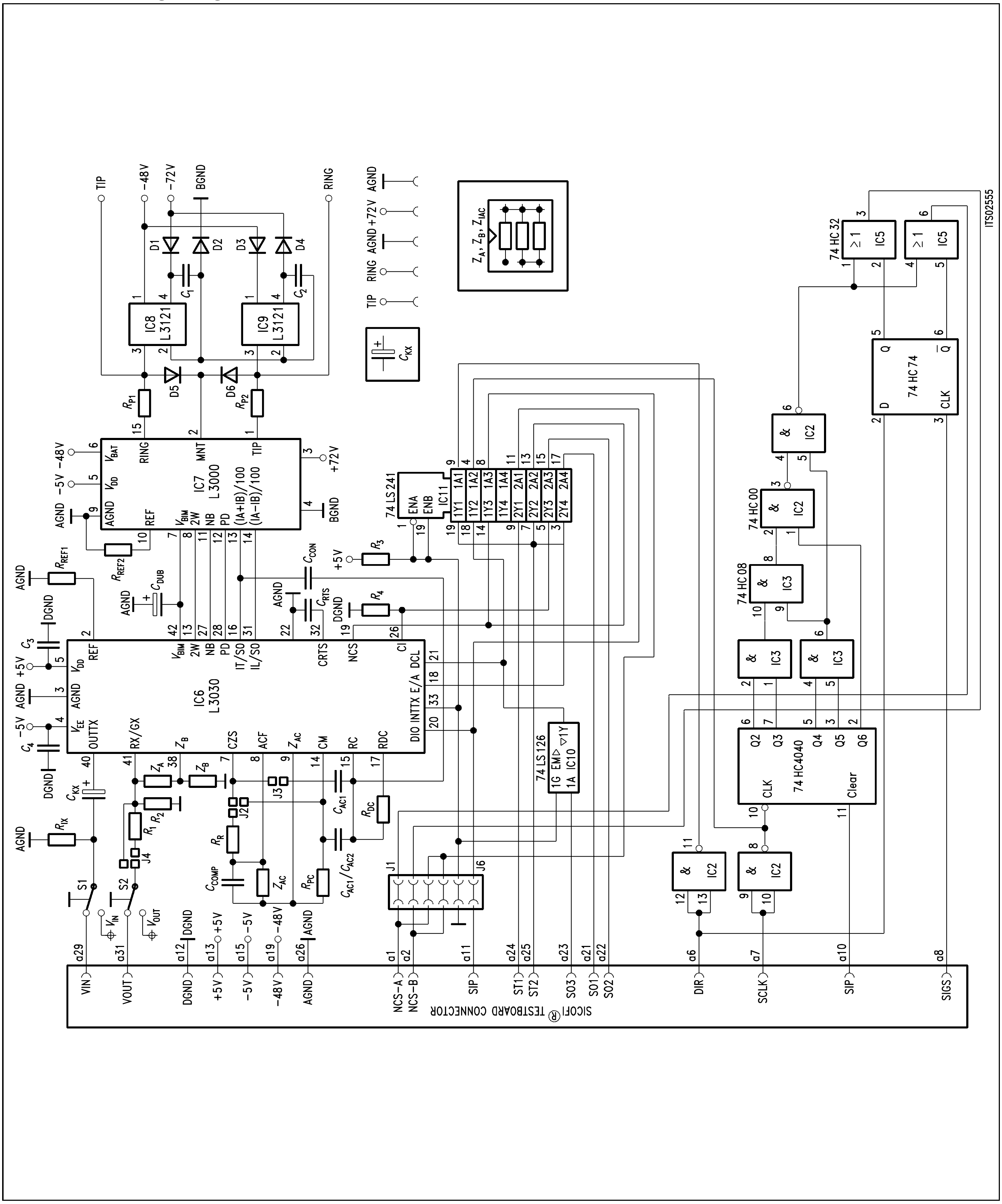


Figure 4
Wiring Diagram of the SLIC Babyboard STUS 3030

3.4 List of Replaceable Parts

Component	Type/Value
IC1	74HC 4040
IC2	74HC 00
IC3	74HC 08
IC4	74HC 74
IC5	74HC 32
IC6	L3030
IC7	L3000
IC8, IC9	L3121
IC10	74LS126
IC11	74LS241
D1 ... D6	1N4004
C_1, C_2	22 nF
C_3, C_4	47 µF
C_{kx}	1 µF
C_{AC1}, C_{AC2}	1 µF
C_{comp}	22 nF
C_{con}	150 nF
C_{rts}	330 nF
R_1, R_2	1 kΩ
R_3	4.7 kΩ
R_{REF1}, RB_{REF2}	25.5 kΩ
R_{ix}	10 kΩ
Z_A	6.2 kΩ (not installed)
Z_B	10 kΩ
Z_{AC}	499 Ω
R_R	49.9 kΩ
R_{pc}	100 Ω
R_{DC}	300 Ω
R_{p1}, R_{p2}	50 Ω

3.5 Floor Plan

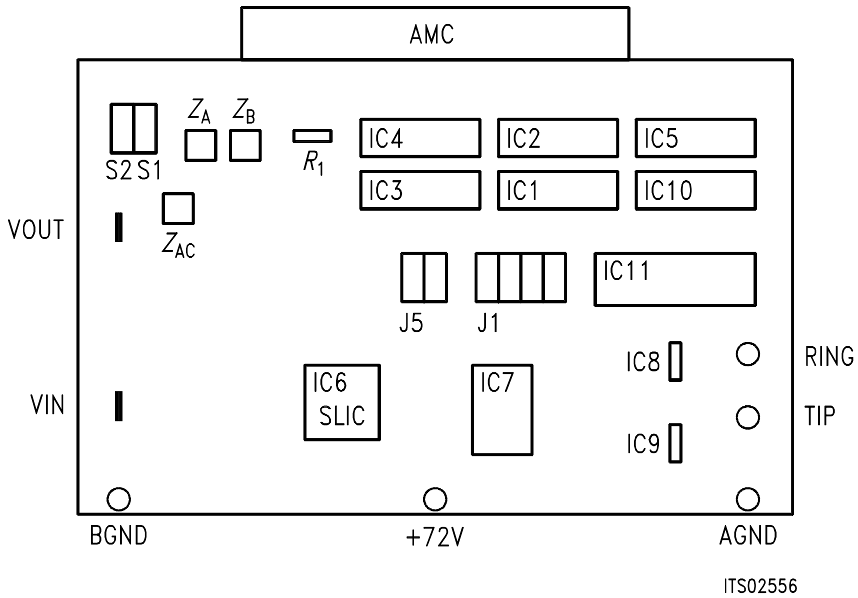


Figure 5
Floor Plan of the STUS 3030 Babyboard

4 Operational Information

4.1 Configuration

Before power is applied, the SLIC Babyboard has to be configured by means of setting switches S1, S2, jumpers J1 ... J6 and connecting the solder bridge for a particular application.

Possible configurations are:
– selecting the 4-wire analog side of the SLIC
– selecting serial or parallel mode at the digital interface
– using the balancing networks Z_A and Z_B and the voltage divider in receive direction

4.1.1 Setting Switches S1 and S2

The Babyboard contains two switches S1 and S2 to connect the 4-wire side of the SLIC to particular pins of the SLIC connector SLC or to the tags VIN/VOUT at the board.

Switch	Position	Pin	Connection
S1	int.	VIN at SLC	SICOFI and SLIC
S1	ext.	VIN	SLIC to tag VIN
S2	int.	VOUT at SLC	SICOFI and SLIC
S2	ext.	VOUT	SLIC to tag VOUT

4.1.2 Solder Bridges

The voltage divider and the capacitor multiplier are selected by establishing peculiar connections at solder bridges 1 ... 3:

Solder bridge 1 (below R1 – **see floor plan**) is to enable the voltage divider:

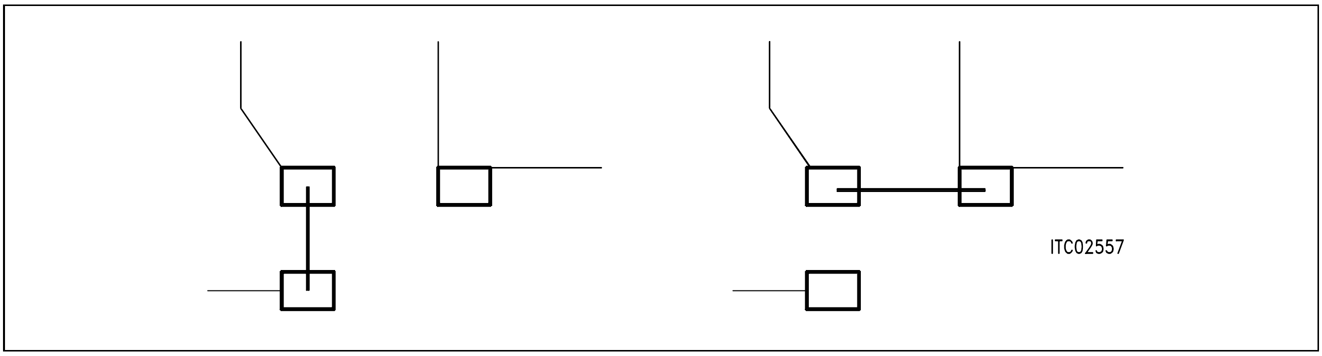


Figure 6
Solder Bridge 1. Left: Divider is Active. Right: Divider is Inactive.

Solder bridge 2 (close to C_{AC1} at the soldering side of the board) is to connect C_{AC1} to pin 7. If bridged, capacitor C_{AC1} is connected to pin 7.

Solder bridge 3 (near solder bridge 2) is to enable the capacitor multiplier.

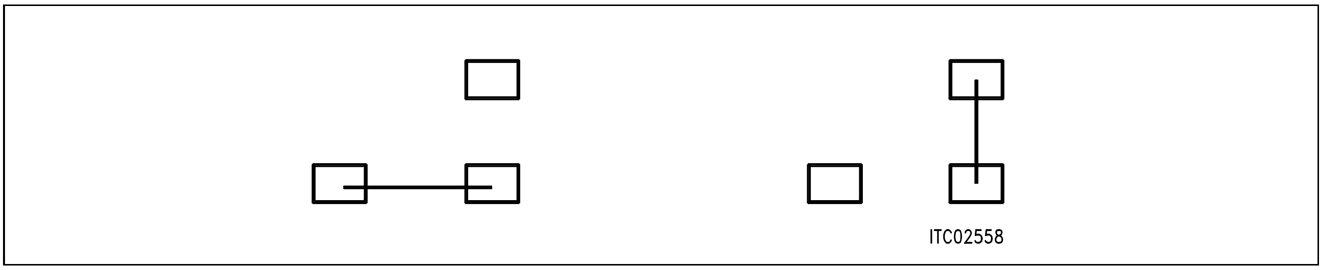


Figure 7
Solder Bridge 3. Left: Capacitor Multiplier is Active (R_R connected to pin 7). Right: Capacitor Multiplier is Inactive (R_R disconnected, pin 7 connected to pin 14)

4.1.3 Jumpers J1 ... J6

The jumpers J1 ... J6 select the digital interface for the SLIC. Jumpers J5 and J6 are to select serial or parallel interface mode. When jumpers J1 or J2 are set, being in the serial interface mode, the SLIC is connected to external hardware; instead, being in parallel interface mode, it is connected to the SICOFI signaling interface via the SLC. Operating in the serial interface mode, the SLIC may be clocked externally. Together with jumpers J1 and J2 jumpers J3 and J4 select the data clock source.

Serial interface mode

J1	J2	J3	J4	J5	J6	
set	open	set	open	set	set	SLIC-A, clocked internally
open	set	open	set	set	set	SLIC-B, clocked internally
open	open	set	open	set	set	SLIC-A, clocked externally
open	open	open	set	set	set	SLIC-B, clocked externally

Parallel interface mode

---------- not defined --------- open open

4.2 Mode Select

The actual modes of the SGS-THOMSON SLIC HC 3030 are selected by the digital interface. This interface is connected to the SIP line of the SICOFI via external hardware or to the signaling pins of the SICOFI when operating in the serial or parallel interface modes respectively. Information is transferred to the SLIC by the signaling byte of the SIP line. The signaling commands are different for the SICOFI Testboard STUT 2060 and for the SICOFI-2 Board SIPB 5135.

4.2.1 Mode Select for STUT 2060

The SLIC may be operated both in the serial or parallel interface mode. When working in the parallel mode, mode selection differs for the Testboard STUT 2060 being equipped with the SICOFI PEB 2060 or with the SICOFI-2 PEB 2260.

When using the Testboard STUT 2060 in the serial interface mode, the SLC2 requires the signaling byte at the SIP line 1 with the command SIG1 instead of SIG0.

Following byte sequences apply to the STUT 2060 using the **PEB 2060** or **PEB 2260** in **serial interface mode**:

SIG0 = 00	power down
SIG0 = 80	power up (I = 25 mA)
SIG0 = 81	power up (I = 30 mA)
SIG0 = 82	power up (I = 70 mA)
SIG0 = 83	power up (I = 45 mA)
SIG0 = C0	active, conversation
SIG0 = A0	ringing

The line status (OFF-hook/ground-key) can be read via the SICOFI SIP-line:

SIG0: 40	ON-hook
SIG0: C0	OFF-hook, ground-key not found
SIG0: 80	OFF-hook, ground-key found

The SCR register of the PBC has to be programmed to generate a signal at its SIGS pin. Using this signal the discrete logic creates a chip select signal for the SLIC. The particular SLIC is selected by:

SCR = 90	SLIC A
SCR = 50	SLIC B

Following byte sequences apply to use the **PEB 2060** in **parallel interface mode**:

SIG0 = 00 power down
SIG0 = 80 power up, conversation
SIG0 = E0 power up, ringing

The line status can be read from the SIP-line:

SIG0: 80 ON-hook
SIG0: 00 OFF-hook, no ground-key found
SIG0: 40 OFF-hook, ground-key found

Following byte sequences apply to using the **PEB 2260** in **parallel interface mode**:

SIG0 = 00 power down
SIG0 = 11 power up, conversation
SIG0 = 77 power up, ringing

The line status can be read from the SIP-line for both SLICs:

SIG0: 11 ON-hook
SIG0: 00 OFF-hook, no ground-key found
SIG0: 22 OFF-hook, ground-key found

4.2.2 Mode Select for SIPB 5135

Attention: In connection with the SICOFI-2 Board SIPB 5135 the SLIC Babyboard can be operated only in the parallel interface mode (jumpers J5 and J6 open).

Following byte sequences apply to the SIPB 5135 using the **PEB 2260** channel A (channel B = + 80_H):

C/I = 03 standby
C/I = 07 active, conversation
C/I = 4F ringing

The loop and ground key information is available for both SLICs:

C/I: 27 ON-hook
C/I: 03 OFF-hook, no ground-key found
C/I: 4B OFF-hook, ground-key found

5 Glossary

DIR	Direction signal (same as FSC)
FSC	Frame Synchronization Clock
PCM	Pulse Code Modulation
SICOFI	SIgnal processing COdec FIlter
SIG	SIGnaling byte at the SIP-line
SIP	Serial Interface Port
SIPB	Siemens ISDN PC User Board (system)
SLC	SLIC Interface Connector
SLD	Subscriber Line Data
SLIC	Subscriber Line Interface Circuit
STUS	Siemens Telecom User Board SLIC
STUT	Siemens Telecom User Board Testboard

6 Application and Example

The SGS-THOMSON Babyboard STUS 3030 is used in connection with the SICOFI Testboard STUT 2060 when an analog line card application is tested using SGS-THOMSON SLICs L3000/L3030. To demonstrate its functionality a set-up is given below: The Babyboard is connected to the Testboard via the SLIC connector SLC and configured as described in **chapter 4**. The required clocks are generated at the Testboard. The PCM4 is connected to the Testboard for to measure the transfer functions of the SICOFI and the SLIC. For the connection and programming procedures of the PCM4 refer to the SICOFI Testboard description.

The programming of SICOFI is listed in the SICOFI Application Note "SGS-THOMSON SLIC L3000/L3030". The byte file (L3030.BYT) is shown in the following **table 1** (serial interface mode):

Table 1
Byte File to Program the SICOFI® PEB 2060 in Serial Interface Mode

PSR = 36
CAM00 = 41
CAM20 = 40
SCR = 90
CIW0 = 06, F4, 80
CIW0 = 13, B0, BA, A1, 6A, BB, 19, DC, 22
CIW0 = 23, 00, 09, 8D, 5D, BA, 9B, 02, 35
CIW0 = 2B, 60, 1A, 9C, 42, 93, 3A, 14, 12
CIW0 = 30, 21, A2, 10, B3
CIW0 = 03, CC, 23, BB, AB, D6, A9, DC, B1
CIW0 = 0B, 00, FE, 69, B1, DD, F2, C1, DE
CIW0 = 18, 19, 19, 11, 19
CIW0 = 26, F4, 78
SIG0 = A0

Table 2
Byte File to Program the SICOFI-2 PEB 2260 Channel A in Serial Interface Mode

PSR = 36
CAM00 = 41
CAM20 = 40
CIW0 = 05, 00, 00
CIW0 = 13, B0, B4, A1, 6A, BB, 19, DC, 22
CIW0 = 23, 00, 09, 8D, 5D, BA, 9B, 02, 35
CIW0 = 2B, 60, 1A, 9C, 42, 93, 3A, 14, 12
CIW0 = 30, 10, B3, 80, 80
CIW0 = 3A, 21, A2
CIW0 = 03, CC, 23, BB, AB, D6, A9, DC, B1
CIW0 = 0B, 00, FE, 69, B1, DD, F2, C1, DE
CIW0 = 18, 19, 19, 11, 19
CIW0 = 25, 00, 00, FC
SIG0 = A0

Switch and Solder Bridge Settings

Before connecting the Testboard to the PCM4 and SLIC Babyboard respectively, make sure that all jumpers and switches are set correctly.

Testboard:	DIL switch 1.1 – 1.4 ON	
	DIL switch 2.1 – 2.4 ON	
Babyboard:	Switch S1	position int.
	Switch S2	position int.
	Solder bridge 1	open
	Solder bridge 2	open
	Solder bridge 3	bridged
	Jumpers J1, J3	set
	Jumpers J2, J4	open
	Jumpers J5, J6	set (serial interface mode)

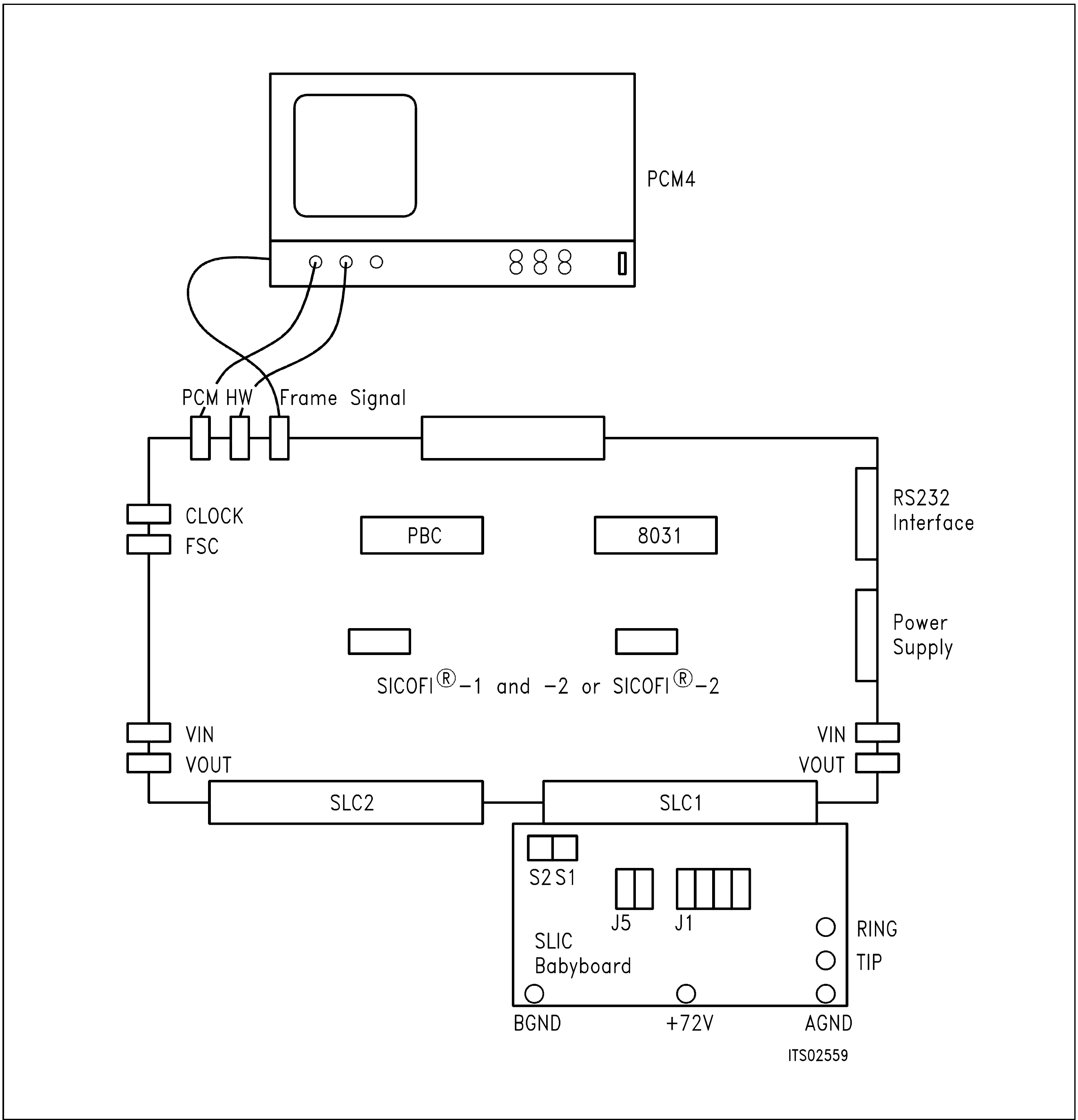


Figure 8
SICOFI® Measurement Set-Up

Required hardware for a measurement set-up:

1 PC IBM AT or compatible
1 PCM4 (Measuring set of Wandel & Goltermann)
1 SICOFI Testboard STUT 2060
1 SLIC Babyboard

SLIC Babyboard STUS 3090 for STM SLIC L3000/L3090

Contents **Page**

1 Features

- Interface to SICOFI Testboard STUT 2060
- Interface to SICOFI-2 Module SIPB 5135
- 4-wire side of the SLIC for internal or external measurements selectable
- Analog telephone directly connectable
- Battery voltage + 72 V can be connected via two banana plugs

2 Use

For one of our SLIC-applications a SGS-Thomson SLIC babyboard has been designed in order to connect it with the SICOFI-testboard STUT 2060.

With both boards it is possible to measure the transfer functions of the SGS-Thomson –SLIC L3090/L3000 together with the SICOFI and to check the calculations done with SICOFI coefficients program.

The switches S1 and S2 select the 4-wire side of the SLIC. In this way measurements with or without the SICOFI are possible. The signaling pins of SICOFI are connected with the control interface of the L3090 to control the SLIC functions. Therefore it is possible to select the modes

power down
power up
ringing

and to read out the status of

OFF- or ON-hook and
ground-key.

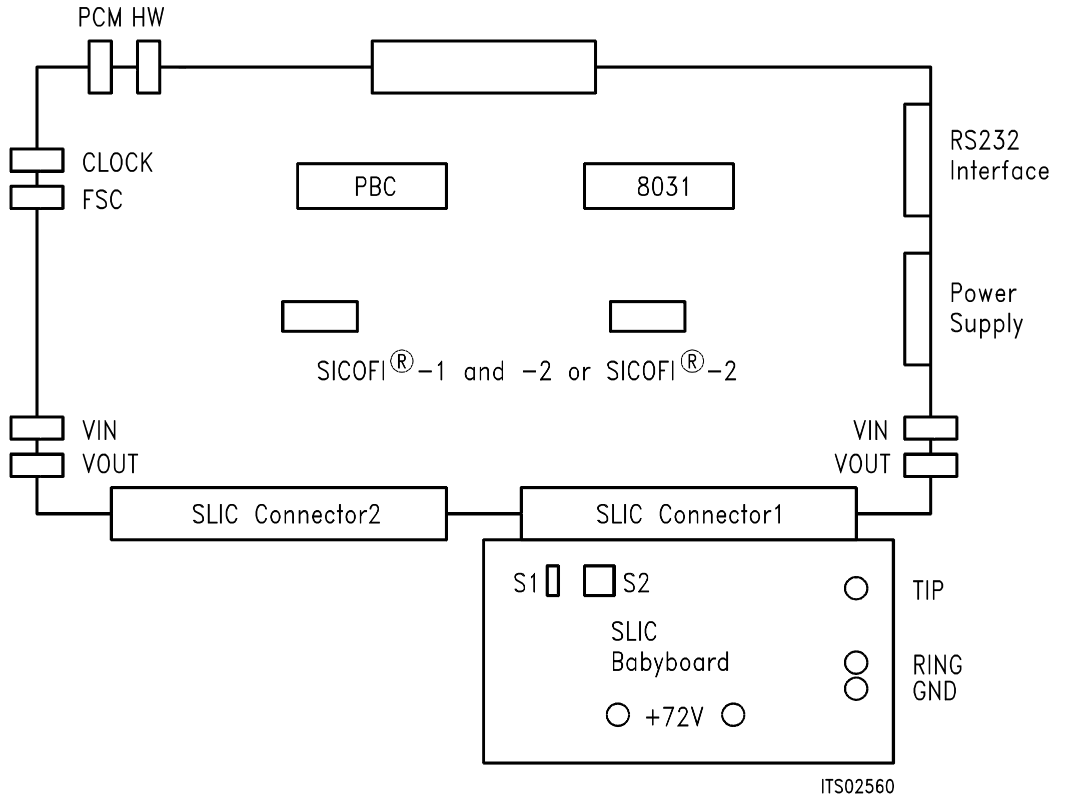


Figure 1
SLIC Connecting with the SICOFI® Testboard

Using a set-up like that shown in **figure 1**, the transfer measurements of an analog line card can be established. For programming, the Byte File are used which can be found in the SGS-Thomson L3090 Application Note.

3 Circuitry

3.1 Block Diagram

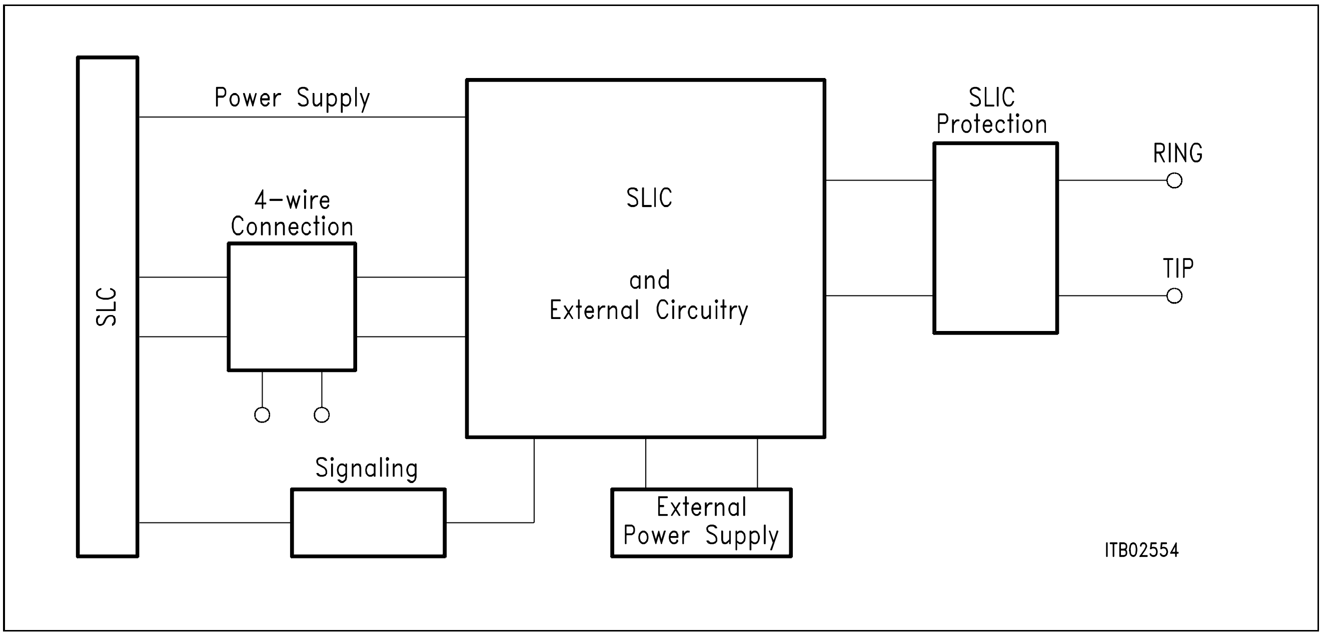


Figure 2
Block Diagram of the SLIC Babyboard STUS 3090

In **figure 2** the five functional blocks of the SLIC babyboard are shown:

– SLIC
– Protection circuit
– Signaling
– External power supply
– 4-wire connection

3.1.1 SLIC

The SLIC is divided into two parts, a low voltage part (L3090) and a high voltage part (L3000).

The high voltage part is connected with the line. It realizes the battery feeding and switches the ringing signal and the speech signal in both directions through the SLIC. The line current is programmable with 4 values and an internal temperature detection unit switches the line current off, when the temperature gets too high. The ringing signal is produced by the battery voltage and a slow control AC-voltage. The ringing signal starts and stops when the signal crosses zero. The low voltage and frequency signal is amplified and injected in balancemode into the line with a superimposed DC voltage of 22 V. The low voltage part synthesizes the DC characteristic, the output impedance performs the echo cancellation. Some of these functions can be realized by the SICOFI and therefore it was possible to reduce the number of external components. The L3090 has a digital parallel interface to control the SLIC modes. The modes are

– power down
– standby
– conversation
– ringing.

3.1.2 Protection Circuit

The protecting circuit protects the SLIC from high voltages (as lightning). This is realized by two protection circuits L 3121 from SGS-Thomson and some diodes. This circuit is designed between the a/b-lines.

3.1.3 Signaling

The signaling lines connect the SICOFI signaling interface with the digital SLIC interface. The SICOFI switches the SLIC into one of the four possible modes and the SLIC generates the information of the loop status (ground key and on/OFF-hook) for the SICOFI.

3.1.4 Power Supply

The SLIC gets the power from the SLIC connector. Only for the battery voltage + 72 V an external power supply has to be connected in some special applications.

3.1.5 4-Wire Selection

Two switches S1 and S2 select the 4-wire connection to measure the SLIC functions alone (ext.) or with SICOFI (int.).

3.2 Connector Pin-Outs

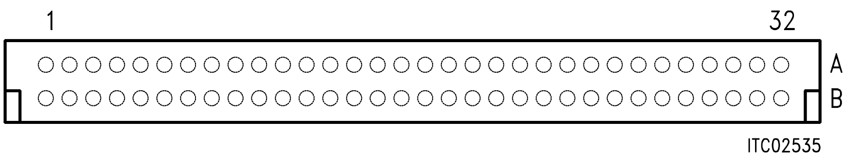


Figure 3
SLIC Connector SLC

Note: Pins not mentioned are not connected

Pin	Row	Function	Signal	Meaning
12	A	I	GND	Power supply
13	A	I	+ 5 V	Power supply
15	A	I	– 5 V	Power supply
19	A	I	– 48 V	Power supply
21	A	I	SO1	Signaling power up/down
22	A	I	SO2	Signaling ringing
23	A	I	SO3	Current limiting
24	A	O	SI1	Hook detection
25	A	O	SI2	Ground key
26	A	I	DGND	Digital ground
28	A	I	AGND	Analog ground
29	A	O	VIN	4-wire analog output
30	A	I	AGND	Analog ground
31	A	I	VOUT	4-wire analog input
32	A	I	AGND	Analog ground
21	C	O	SA	Pull up SICOFI input
22	C	O	SB	Pull up SICOFI input
23	C	O	SC	Pull up SICOFI input
24	C	O	SD	Pull up SICOFI input

3.3 Wiring Diagram

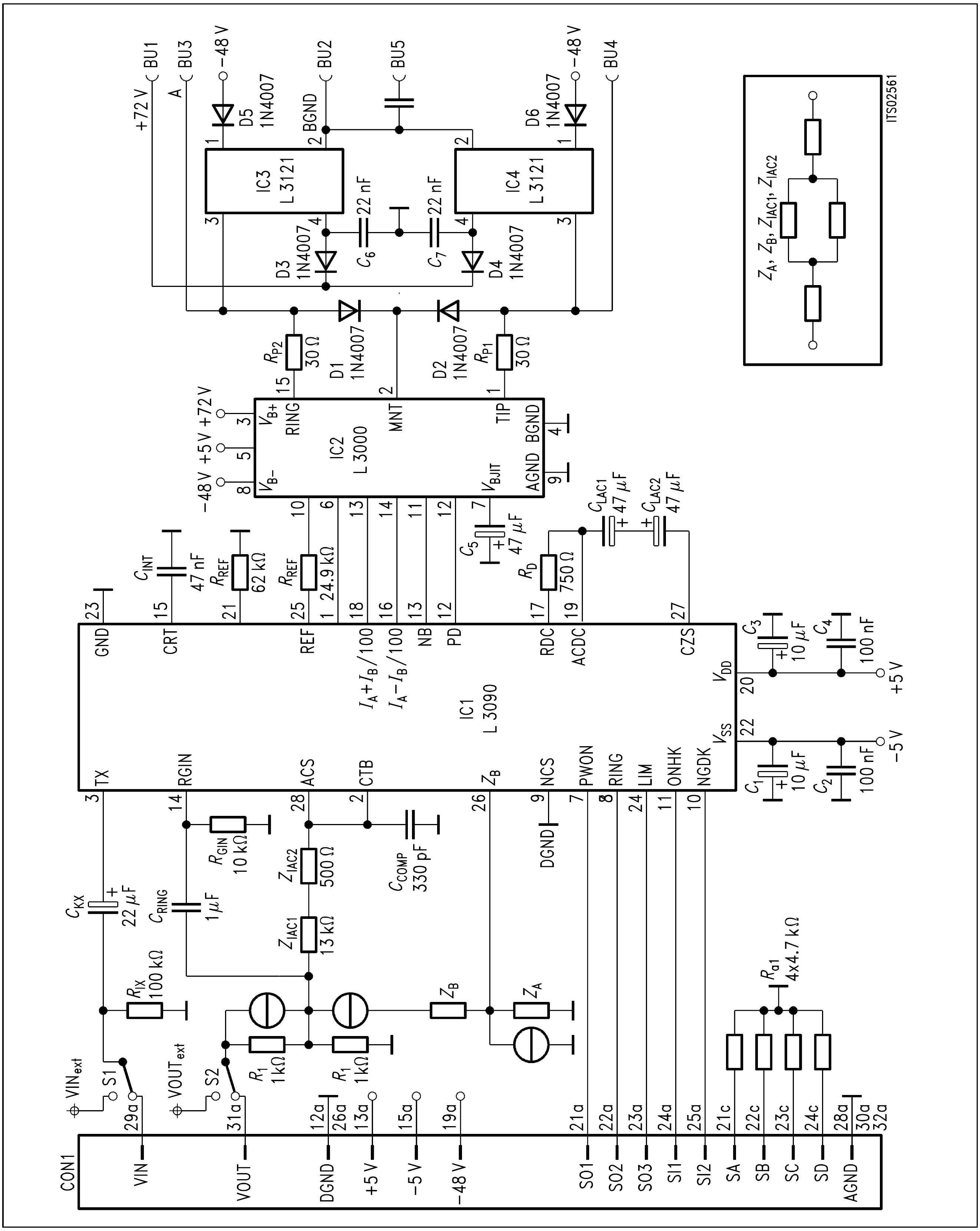


Figure 4
Wiring Diagram

3.4 List of Replaceable Parts

Component	Type
IC1	L3090
IC2	L3000
IC3, IC4	L3121
D1, D2, D3	1N4007
D4, D5, D6	1N4007
C_1, C_3	10 µF
C_2, C_4	100 nF
C_5	47 µF
C_6, C_7	22 nF
C_{kx}	22 µF
C_{ring}	1 µF
C_{comp}	330 pF
C_{int}	47 nF
C_{lac1}, C_{lac2}	47 µF
R_1, R_2	1 kΩ
R_{Gin}	10 kΩ
R_{ix}	100 kΩ
Z_{iac1}	13 kΩ
Z_{iac2}	500 Ω
R_D	750 Ω
R_{REF1}	62 kΩ
R_{REF2}	24.9 kΩ
R_{p1}, R_{p2}	30 Ω
R_{a1}	4 × 4.7 kΩ

3.5 Floor Plan

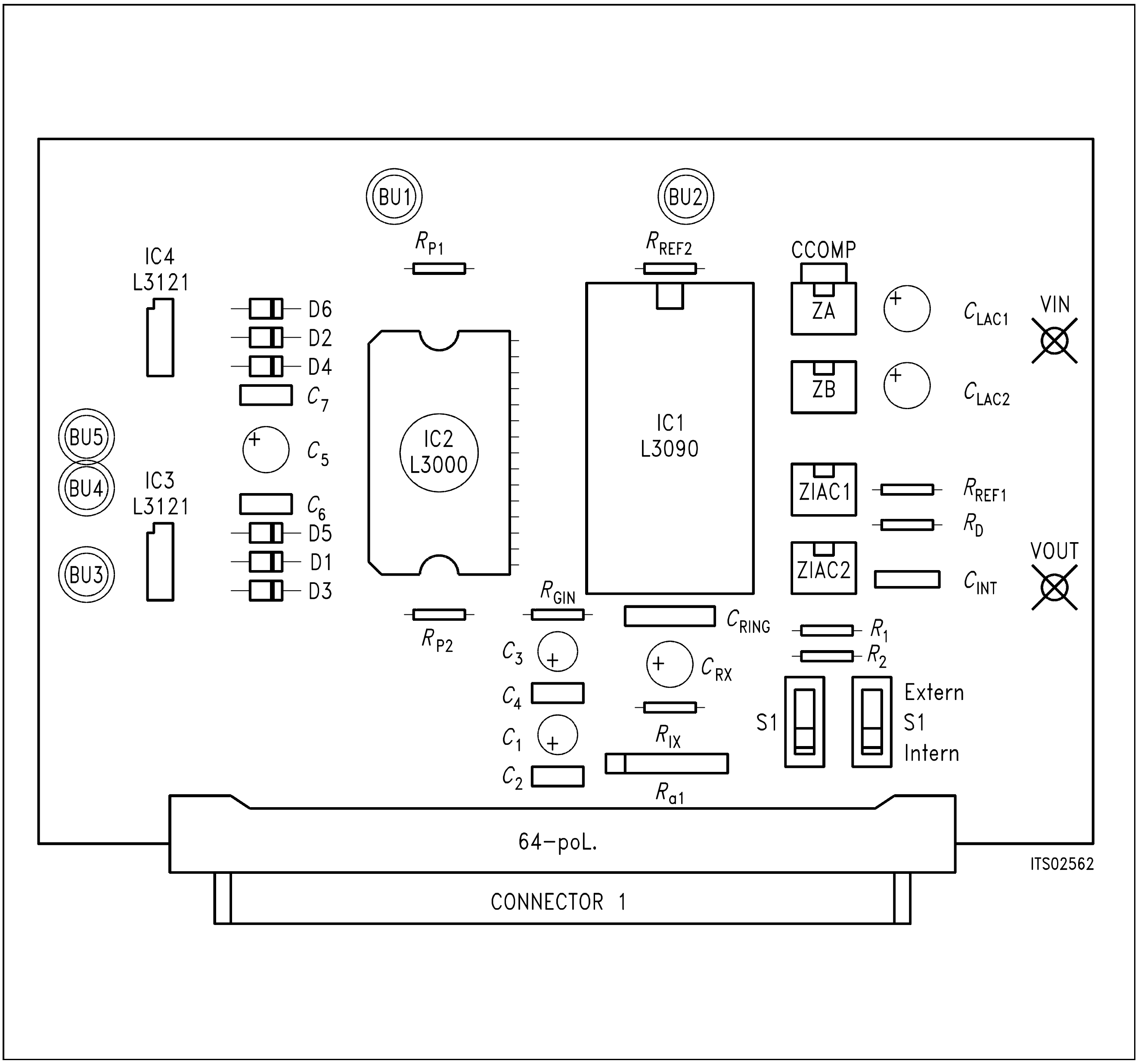


Figure 5
Floor Plan

4 Operational Information

4.1 Configuration

Before power is applied, the SLIC babyboard has to be configured by means of switches S1, S2 and connecting the solder bridge for a given application.
Possible configurations are:

– selecting the 4-wire analog side of the SLIC
– operating with Z_A, Z_B and the voltage divider in receive direction

4.1.1 Setting Switches S1 and S2

The babyboard contains two switches S1 and S2 to connect the 4-wire SLIC side to the pins at the SLIC connector SLC or to the external pins VIN/VOUT.

Switch	Position	Pin	Connection
S1	int.	VIN at SLC	SICOFI with SLIC
S1	ext.	VIN	SLIC with external pin VIN
S2	int.	VOUT at SLC	SICOFI with SLIC
S2	ext.	VOUT	SLIC with external pin VOUT

4.1.2 Solder Bridge

The solder bridges select the voltage divider and the impedances Z_A and Z_B.

Solder bridge (1) below R_1		
	open	the divider is active
	shorted	the divider is inactive
Solder bridge (2) close Z_A		
	open	the impedance Z_B is not connected to Z_{iac1}
	shorted	the impedance Z_B is connected to Z_{iac1}
Solder bridge (3) close Z_B		
	open	Pin ZB from the SLIC is open
	shorted	Pin ZB from the SLIC is shorted to ground

4.2 Mode Select

The mode of the SGS-Thomson SLIC L3090 is selected by the digital interface. This interface is connected with the signaling pins from SICOFI. The signaling pins are programmed with the SIG command of the SICOFI testboard. Following bytes sequences are possible:

SIG0 = A0	conversation, Ilim = 42 mA
SIG0 = 80	conversation, Ilim > 42 mA
SIG0 = 40	power down
SIG0 = C0	ringing

The line status (OFF-hook/ground-key) can be read out through the SICOFI (SIP-line).

SIG0: 00	ON-hook
SIG0: 40	OFF-hook
SIG0: 80	ground-key

5 Glossary

DIR	Direction signal (same as FSC)
FSC	Frame Synchronization Clock
PC	Personal Computer
PCM	Pulse Code Modulation
SICOFI	SIgnal processing COdec FIlter
SIG	SIGnaling byte at the SIP-line
SIP	Serial Interface Port
SIPB	Siemens ISDN PC Userboard (system)
SLD	Subscriber Line Data
STUS	Siemens Telecom Userboard SLIC
STUT	Siemens Telecom Userboard Testboard

6 Application and Example

The SGS-Thomson L3090 babyboard is used in applications with SICOFI testboard STUT 2060 in which an analog line card application is tested using this SLIC. To demonstrate its functionality a set-up is given. The clocks are generated on the testboard and the PCM4 can measure the transfer functions.

The babyboard is connected with the testboard via the SLIC connector SLC and configured as described in **chapter 4**. The connection and programming of the PCM4 are shown in the SICOFI testboard description.

The programming of SICOFI is listed in the SICOFI Application Note "SGS-Thomson SLIC L3090/L3000". The byte file (L3090.BYT) is shown in the following **table 1**:

Table 1
Byte File to Program the SICOFI®

PSR = 36
CAM00 = 41
CAM20 = 40
CIW0 = 06, F4, 80
CIW0 = 13, 30, D5, 1A, 5D, CB, B1, 25, 33
CIW0 = 23, 50, D8, 8C, 3C, A8, BC, 0A, A4
CIW0 = 2B, 40, C8, AD, 41, A4, 3A, 13, 12
CIW0 = 30, A0, C1, 10, 22
CIW0 = 03, 4B, 13, 14, 20, 14, B1, 42, BA
CIW0 = 0B, 00, 26, DD, 4D, 25, 72, 2B, 46
CIW0 = 18, 19, 19, 11, 19
CIW0 = 26, F4, 78
SIG0 = A0

Switch and Solder Bridge Setting

Before connecting the testboard with the PCM4 and SLIC babyboard, make sure that all jumpers and switches are set correctly.

Testboard:	DIL switch 1.1 – 1.4 ON	
	DIL switch 2.1 – 2.4 ON	
Babyboard:	switch 1	in position int.
	switch 2	in position int.
	solder bridge 1	open
	solder bridge 2	open
	solder bridge 3	shorted

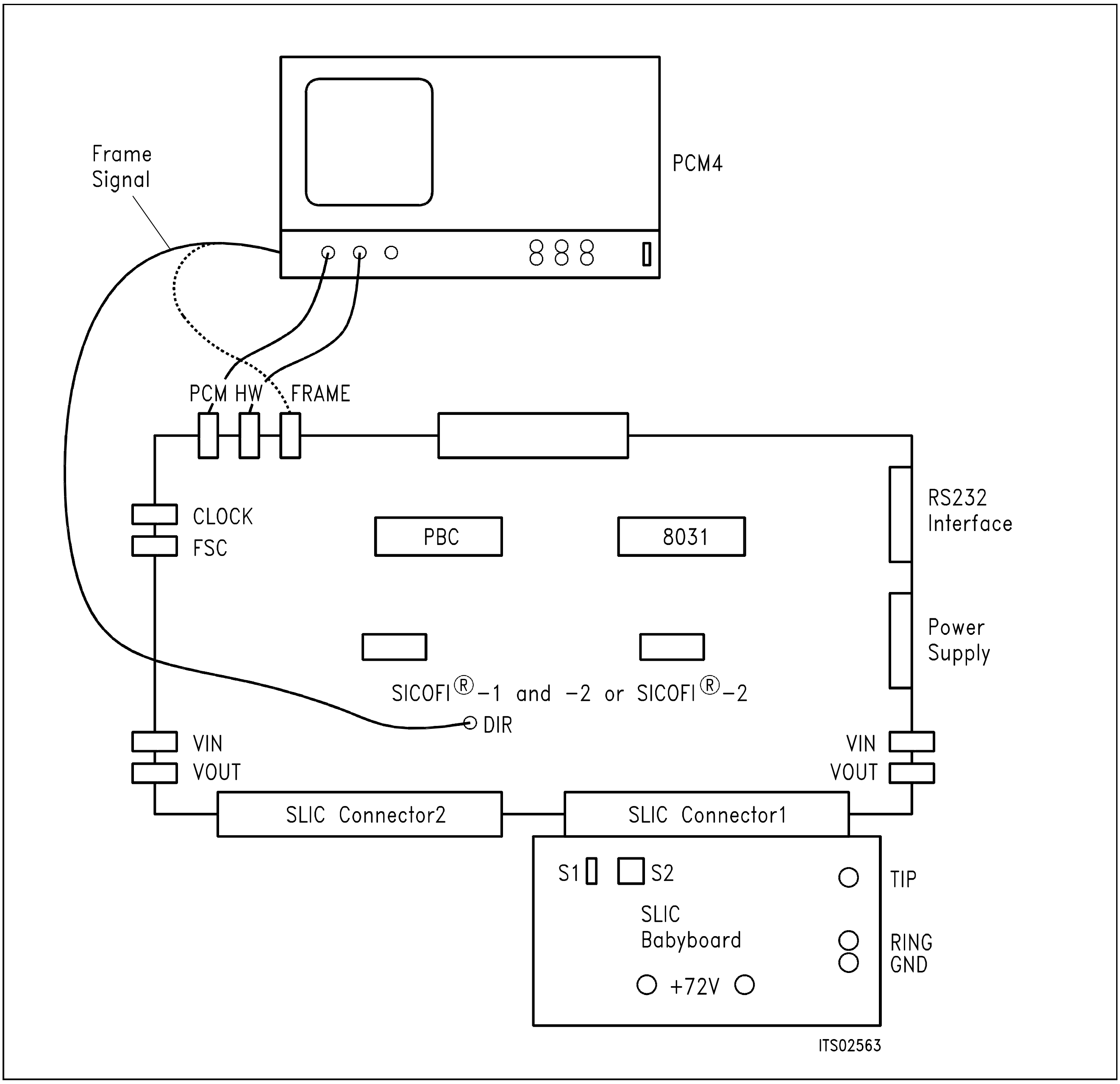


Figure 7
SICOFI® Measurement Tool

Required hardware for a measurement system:

1	PC IBM AT or compatible
1	PCM4 (Measurement set from Wandel & Goltermann)
1	SICOFI Testboard STUT 2060
1	SLIC Babyboard

SLIC Babyboard STUS 1001 for Transformer SLIC

Contents **Page**

1 Features

- Interface to SICOFI Testboard STUT 2060
- Interface to SICOFI-2 Board SIPB 5135
- Transformer SLIC to be used on board
- Only transverse feeding possible

2 Use

For one of our SLIC-applications a Transformer SLIC Babyboard has been designed in order to connect it with the SICOFI Testboard STUT 2060.
With both boards it is possible to measure the transfer functions of the Transformer SLIC together with the SICOFI and to check the calculations done with SICOFI coefficients program.

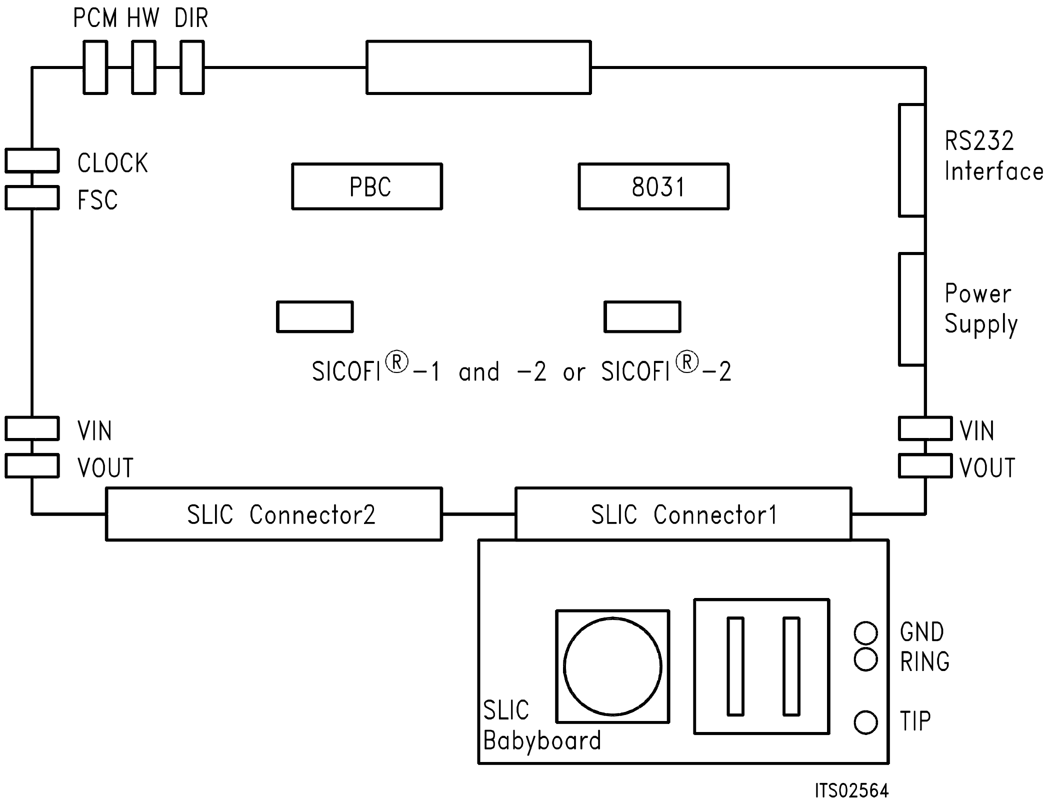


Figure 1
Connecting the SLIC Babyboard to the SICOFI® Testboard

For practical use the SLIC Babyboard STUS 1001 is inserted into one of the SLIC connectors SLC of the SICOFI Testboard STUT 2060. Using a set-up like that shown in **figure 1**, the transfer functions of an analog line card can be established. For programming, the Byte File is used which is to be found in the Transformer SLIC Application Note.

3 Circuitry

3.1 Block Diagram

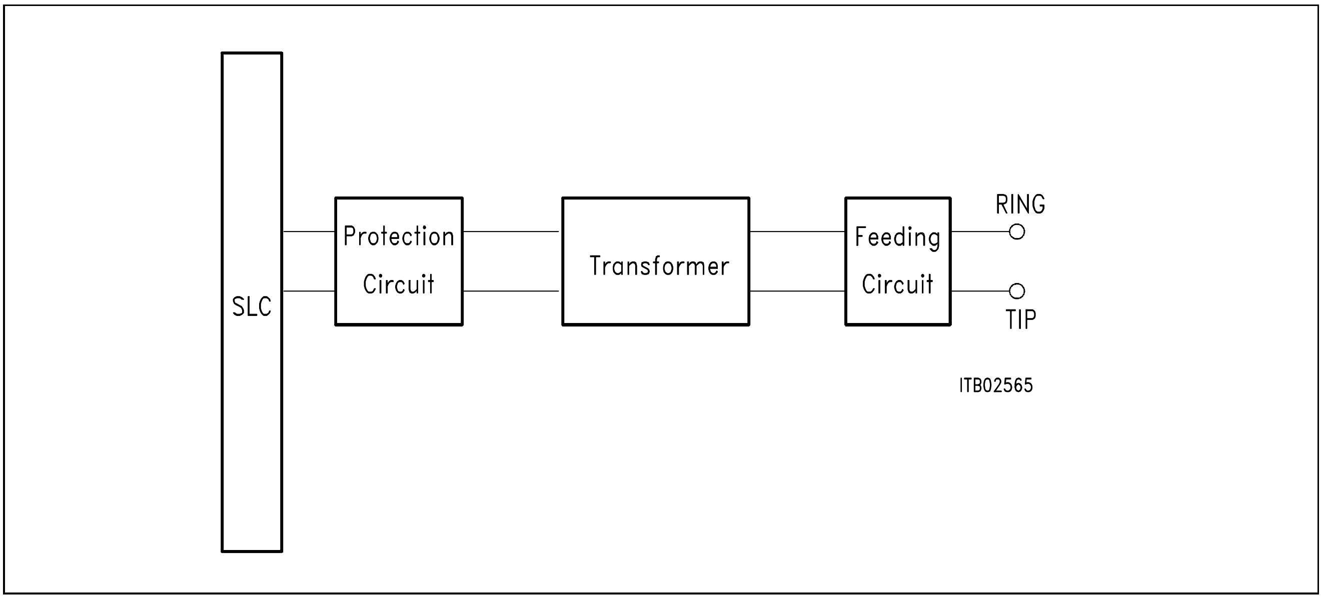


Figure 2
Block Diagram of the SLIC Babyboard STUS 1001

In **figure 2** the three functional blocks of the SLIC Babyboard are shown:

- SLIC
- Protection circuit
- Feeding circuit

3.1.1 SLIC

The SLIC contains two transformers. One of them (Tr1) transforms the analog signal to the a/b lines. The other one (Zsp) may be used for line feed. In a trunk application the SLIC may be fed externally.
This transformer SLIC can be used only in transverse (parallel) feeding configurations.

3.1.2 Protection Circuit

The protection circuit screens the SLIC against high voltages (secondary protection). This is realized by 2 diodes D1, D2 at the SICOFI input.

3.2 Connector Pin-Outs

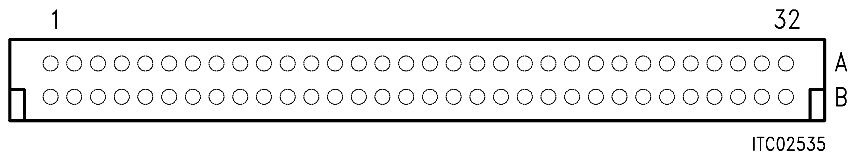


Figure 3
SLIC Connector SLC

Note: Pins not mentioned are not connected

Pin	Row	Function	Signal	Meaning
12	A	I	GND	Power supply
28	A	I	AGND	Analog ground
29	A	O	VIN	4-wire analog output
30	A	I	AGND	Analog ground
31	A	I	VOUT	4-wire analog input
32	A	I	AGND	Analog ground

3.3 Wiring Diagram

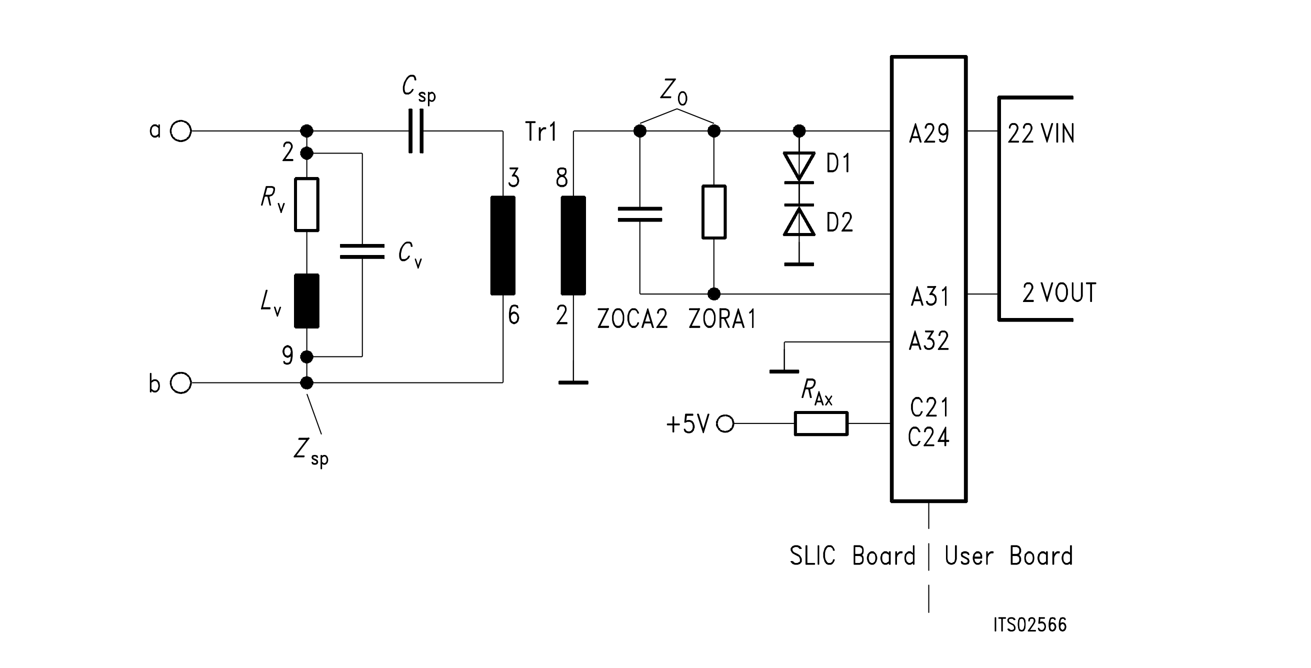


Figure 4
Wiring Diagram of the SLIC Babyboard STUS 1001

3.4 List of Replaceable Parts

Component	Type/Value
D1, D2	C2V7
C_{sp}	1 F
C_v	2 nF
Z_{oCA2}	100 nF
R_v	792 Ω
Z_{0RA1}	700 Ω
R_{ax}	4 × 4.7 kΩ
Zsp	V33101-G2039-B174
Tr1	U Transformer

3.5 Floor Plan

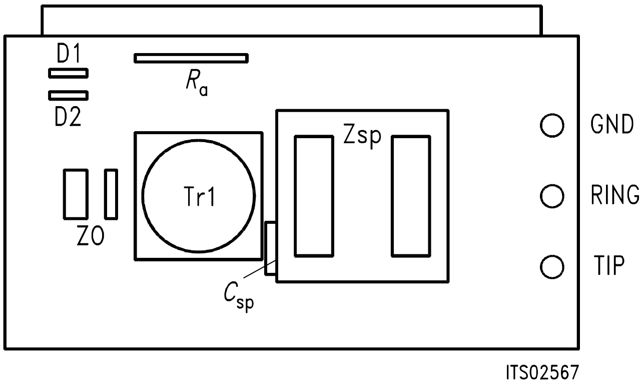


Figure 5
Floor Plan of the STUS 1001 Babyboard

4 Operational Information

4.1 Configuration

Before power is applied, the SLIC Babyboard has to be configured by means of setting the solder bridge.

Possible configurations are:

– with or without blocking capacitor in the a-line.

The solder bridge is at the soldering side underneath the capacitor C_{sp}. Bridging the solder bridge shorts the capacitor C_{sp}. In this case a DC current may flow through the transformer.

5 Glossary

DIR	Direction signal (same as FSC)
FSC	Frame Synchronization Clock
PC	Personal Computer
PCM	Pulse Code Modulation
SICOFI	SIgnal processing COdec FIlter
SIG	SIGnaling byte at the SIP-line
SIP	Serial Interface Port
SIPB	Siemens ISDN PC User Board (system)
SLC	SLIC Interface Connector
SLD	Subscriber Line Data
SLIC	Subscriber Line Interface Circuit
STUS	Siemens Telecom User Board SLIC
STUT	Siemens Telecom User Board Testboard

6 Application and Example

The Babyboard STUS 1001 is used in connection with the SICOFI Testboard STUT 2060 when an analog line card application is tested using the Transformer SLIC. To demonstrate its functionality a set-up is given below: The Babyboard is connected to the Testboard via the SLIC connector SLC and configured as described in **chapter 4**. The PCM4 is connected to the Testboard for to measure the transfer functions of the SICOFI and the SLIC. For the connection and programming procedures of the PCM4 refer to the SICOFI Testboard description.

The programming of SICOFI is listed in the SICOFI Application Note "SICOFI PEB 2060 + Transformer SLIC with Transverse Feeding". The Byte File is shown in the following **table 1** for the SICOFI Testboard STUT 2060 using the PEB 2060:

Table 1
Byte File to Program the SICOFI®

PSR = 36
CAM00 = 41
CAM20 = 40
CIW0 = 06, F4, 80
CIW0 = 13, 20, BA, 2A, 7B, 1B, 32, B2, 5B
CIW0 = 23, 70, E2, 97, 73, C1, D6, 03, 36
CIW0 = 2B, 70, 23, 8F, EC, 3C, AC, 0B, 50
CIW0 = 30, 41, C3, 00, C3
CIW0 = 03, BB, C1, DB, 2B, 46, 22, 21, 2B
CIW0 = 0B, 00, 2C, 31, C1, AA, 6F, 33, 23
CIW0 = 18, 19, 19, 11, 19
CIW0 = 26, F4, 78

Before connecting the Testboard to the PCM4 and SLIC Babyboard respectively, make sure that all jumpers and switches are set correctly.

Testboard: DIL switch 1.1 - 1.4 ON
DIL switch 2.1 - 2.4 ON

Babyboard: Solder bridge is OPEN

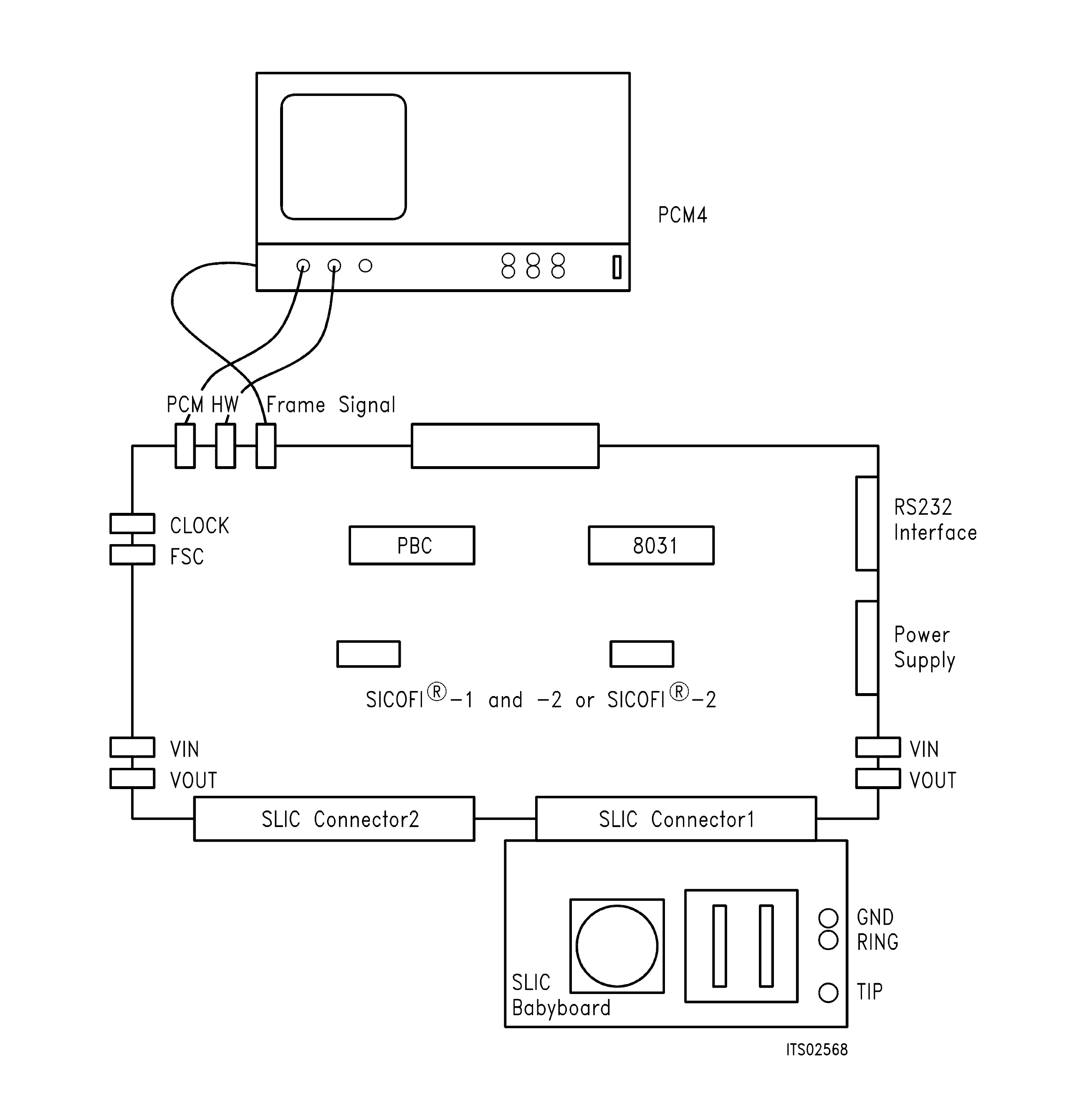


Figure 7
SICOFI® Measurement Set-Up

Required hardware for a measurement set-up:

1 PC IBM AT or compatible
1 PCM4 (Measuring set by Wandel & Goltermann)
1 SICOFI Testboard STUT 2060
1 SLIC Babyboard

SICOFI® Application Together with HARRIS-SLIC HC 5502

Contents **Page**

1 Introduction

This application note describes the combination of a codec filter device (SICOFI) with an electronic SLIC (HARRIS HC 5502A) as it can be used on a line card for the connection of analog subscribers.

This note consists of:

- A general description of the HARRIS-SLIC HC 5502A
- A proposal for the interconnection of SICOFI and SLIC
- A description of the model for the SLIC's function
- A listing of FORTRAN program to calculate SLIC transfer function
- Result of calculation and measurements generated for the requirements of the 'Deutsche Bundespost'.

2 Hardware SICOFI® and HARRIS-SLIC HC 5502

2.1 HARRIS-SLIC HC 5502

The HARRIS-SLIC HC 5502 combines many of the BORSHT-functions on a single chip. The functions are:
– Battery
– Overvoltage
– Ringing
– Signaling
– Hybrid

The SLIC needs a positive (+ 12 V) and a negative (– 48 V) supply voltage. The loop resistance can take on values between 200 Ω and 1200 Ω. The current through the loop is then between 21 mA and 30 mA typically. The SLIC in conjunction with an external protection bridge will with-stand high voltage lightning surges and power line crosses, for a short time (10 µs).
The HC 5502 has two logical input pins (RC, PD) and two logical output pins (SHD, GKD) and a ring synchronisation input RS.

– RC Ring command
– PD Power denial
– SHD Switch hook detection
– GKD Ground key detection

With the two input pins you can switch the SLIC into the three modes:

– Power down
– Power up
– Ringing

If the SLIC is switched into the ringing mode and the RS input has a positive voltage and the ring source then goes to zero, the ring relay driver output will go to low. It goes low only on the next rising edge of the ring synchronisation input, as long as the SLIC is not in the power denial state or the subscriber is not already in off-hook stage. The maximum voltage of the ring relay is 15 V.

The SLIC sends a too high DC voltage at the four wire side, therefore the voltage has to be blocked with one capacitor per wire (> 470 nF).

The digital interface is connected via 4 wires with the SICOFI. The two input pins of the SLIC are connected with two output pins of the SICOFI. The two output pins of the HARRIS SLIC are connected with the three input pins of the SICOFI. That we get no instability, we connect two input pins of the SICOFI with one output pin of the HARRIS SLIC.

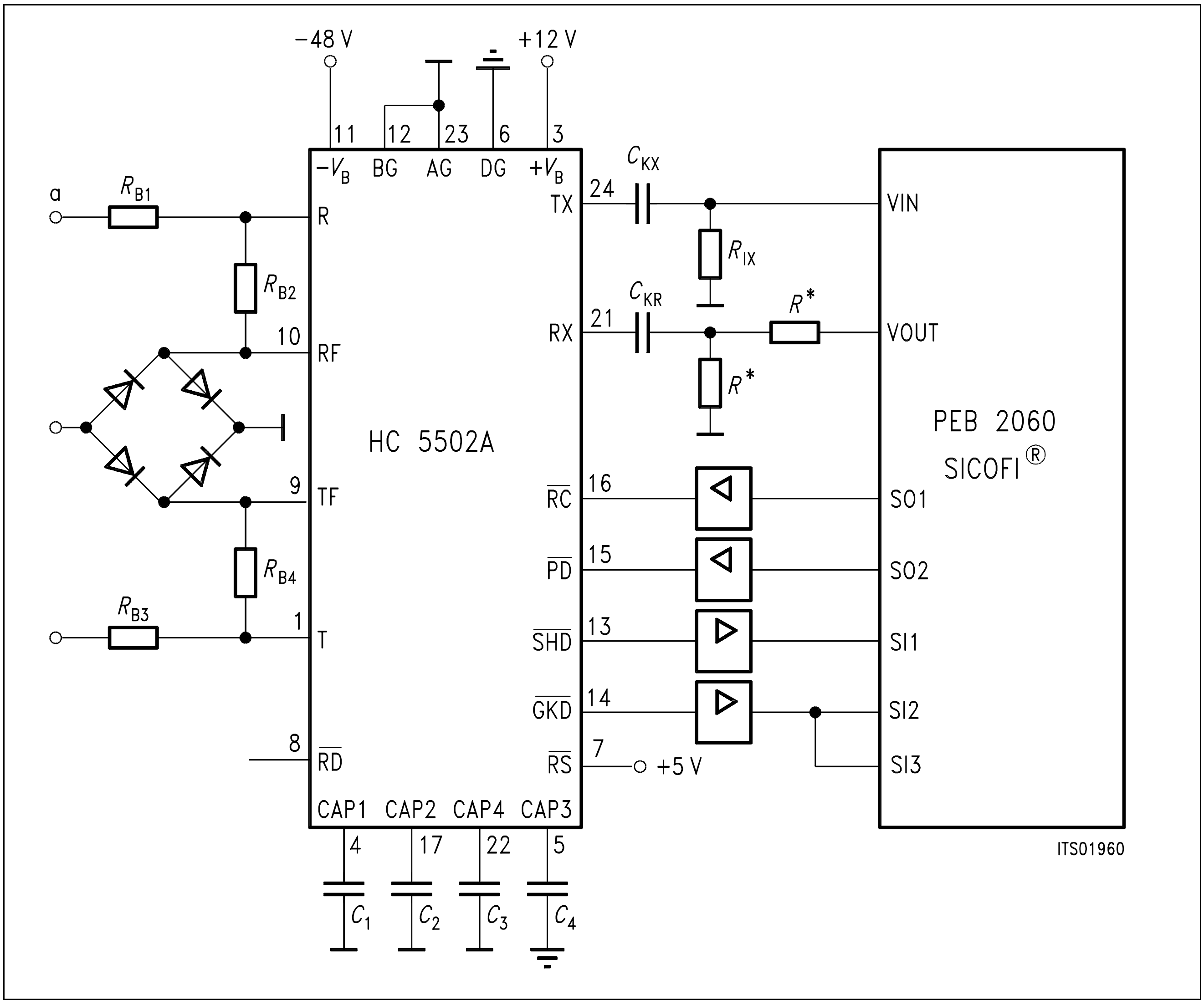


Figure 1

HARRIS SLIC HC 5502 A

Note: This voltage divider is used only for application that need high attenuation in receive direction ($R \geq 300\ \Omega$). The two resistors are not required by using the SICOFI PEB 2060 version. 4.x or the SICOFI-2 PEB 2260 (set attenuation AGR = 6 dB).

2.2 Programming the SICOFI® and SLIC

The signaling byte is used to program the SLIC via the SICOFI:
– Power down: SIG0 = 00
– Power up: SIG0 = C0
– Ringing: SIG0 = 40

The SLIC sends ground key and ON-/OFF-hook detection to the SICOFI:
– SIG0: = 1E Ground key
– SIG0: = 7E OFF-hook
– SIG0: = FE ON-hook

2.3 Model of the HARRIS-SLIC HC 5502

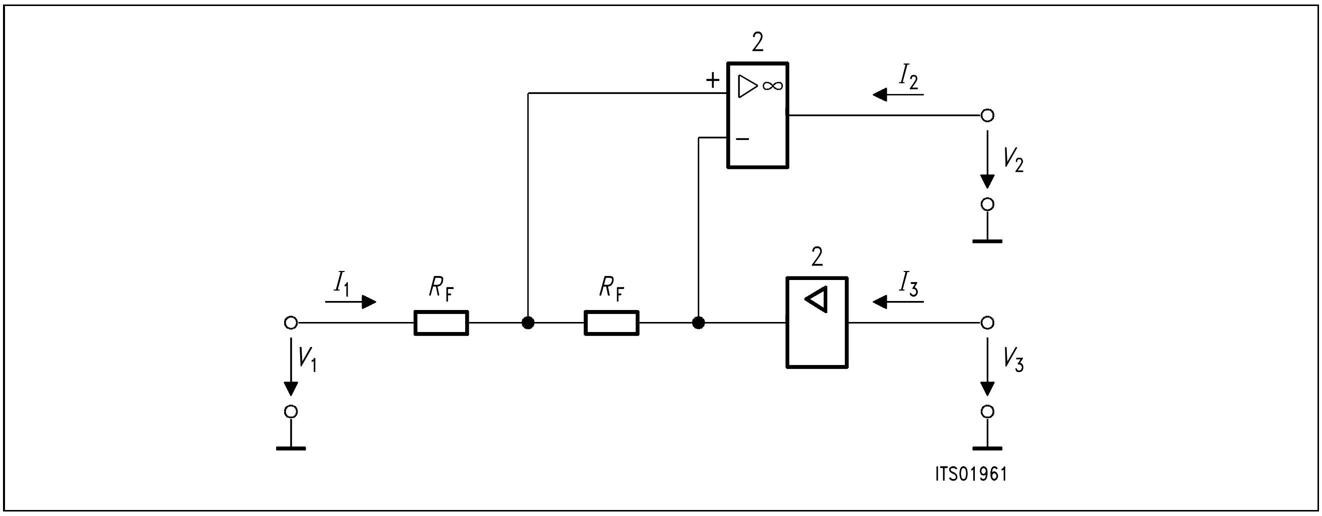


Figure 2

Note: $R_{F1} = R_{B1} + R_{B3}$
$R_{R2} = R_{B2} + R_{B4}$
The specification of 'Deutsche Bundespost' allows an attenuation of 7 dB in receive direction. Due to this we have more than 12 dB attenuation at the SICOFI and this is too much for the SICOFI. In this case either a voltage divider in receive direction is necessary or you can make an analog 6 dB attenuation by programming the AGR of the SICOFI PEB 2060 version 4.x or the SICOFI-2 PEB 2260.

3 Software for HARRIS-SLIC HC 5502

3.1 General SLIC-Parameters

To calculate the coefficients we need the mixed matrix parameters:

Objectives:
– Calculation of the mixed matrix parameters using a simplified three port model.

Method:
– A SLIC is a circuit with a number of elements accessible through three ports:

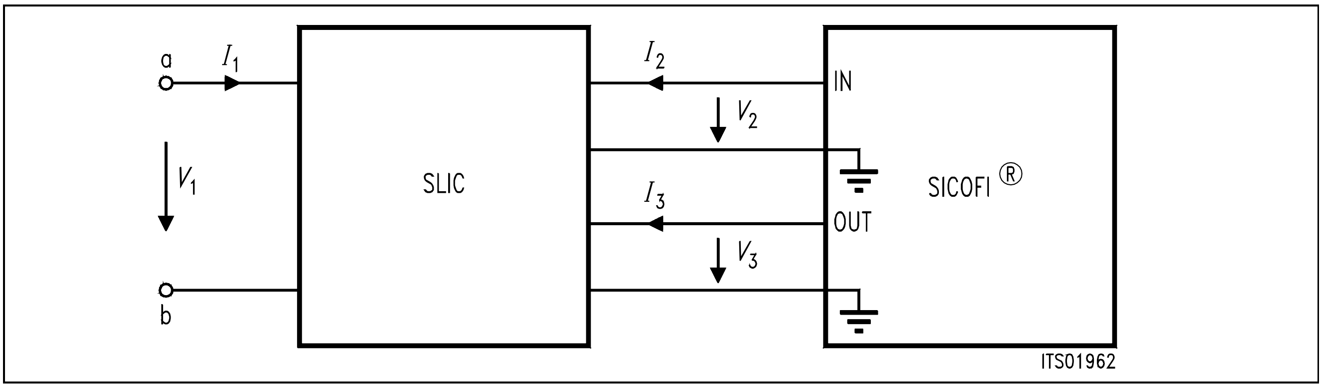
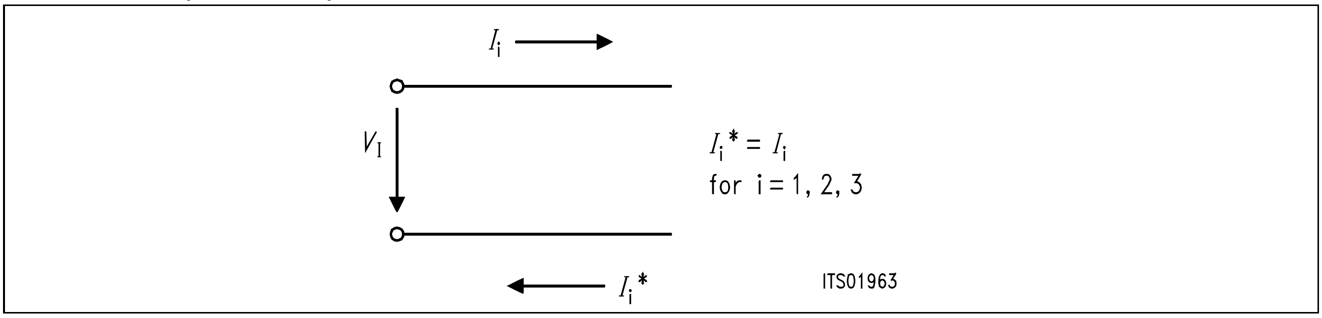


Figure 3

I_1, I_2 and I_3 are port currents
V_1, V_2 and V_3 are port voltages

$I_1 = M11 \times V_1 + M12 \times V_3 + M13 \times I_2$ (1)
$V_2 = M21 \times V_1 + M22 \times V_3 + M23 \times I_2$ (2)
$I_3 = M31 \times V_1 + M32 \times V_3 + M33 \times I_2$ (3)

Note: Description of a port:

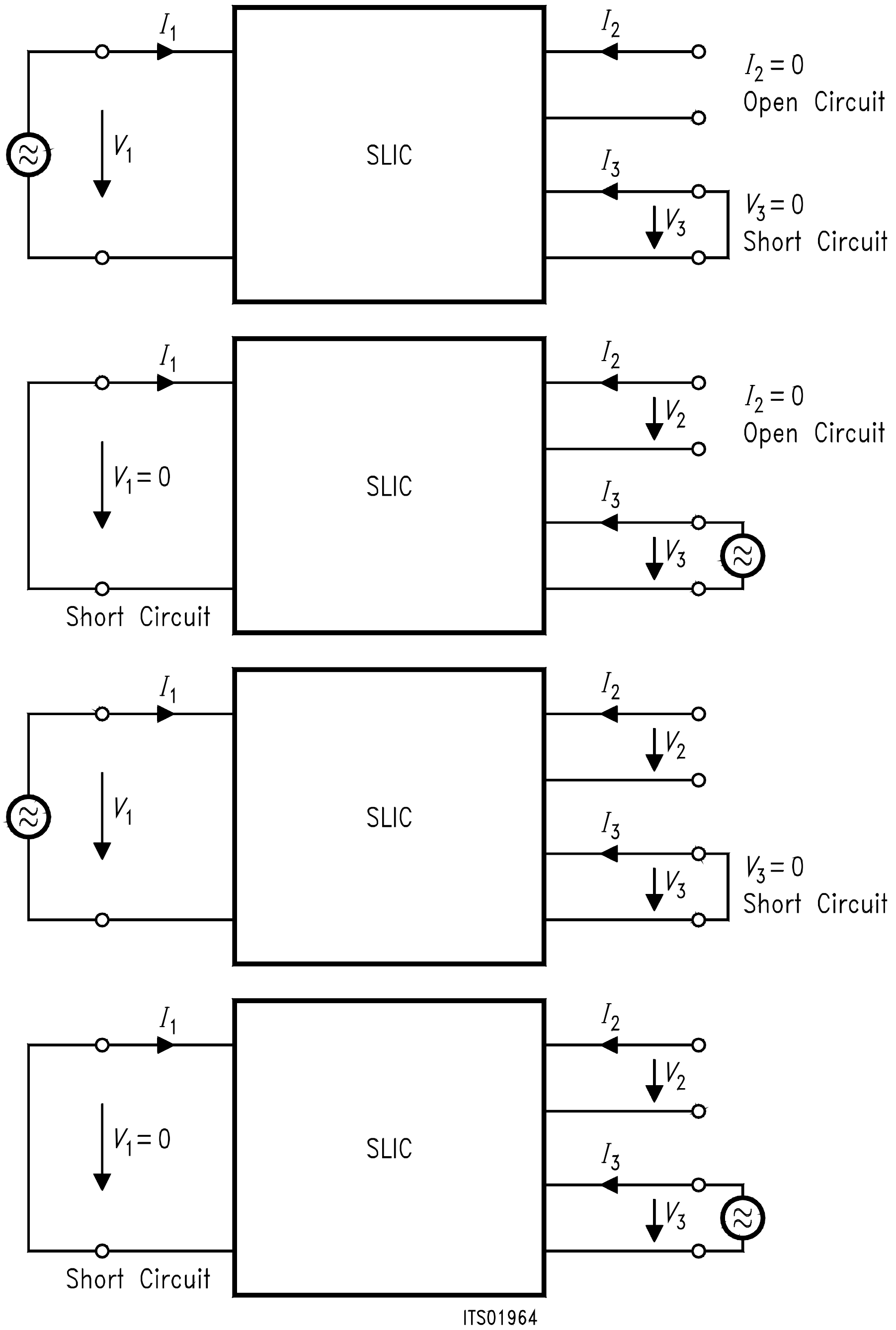


Simplification of the Three Port Model

When the SLIC is connected to the SICOFI, we can assume that:
– I_2 = 0 because the input impedance of SICOFI can be included in the three port model
– I_3 is not relevant in the following calculations because the equation (3) is not used in the SICOFI program.

$I_1 = M11 \times V_1 + M12 \times V_3$ (4)
$V_2 = M21 \times V_1 + M22 \times V_3$ (5)

The parameters M11, M12, M21 and M22 are determined as follows:



$$\mathrm{M11} = \frac{I_1}{V_1} \quad \text{for } V_3 = 0 \text{ (6)}$$

$$\mathrm{M12} = \frac{I_1}{V_3} \quad \text{for } V_1 = 0 \text{ (7)}$$

$$\mathrm{M21} = \frac{V_2}{V_1} \quad \text{for } V_3 = 0 \text{ (8)}$$

$$\mathrm{M22} = \frac{V_2}{V_3} \quad \text{for } V_1 = 0 \text{ (9)}$$

Figure 4

3.2 HARRIS-SLIC Parameter

The mixed matrix parameters are:

M11 = 1 / (2 $\times$ R_F)
M12 = – AR / R_F
M21 = AX
M22 = – 2 $\times$ AR $\times$ AX

3.3 Calculation

The SLIC has a 0 dB gain in receive direction and therefore the SICOFI must attenuate the incoming signal in order to match the german specs (GR = – 7 dB). Because of the attenuation being too high (> 12 dB absolute) for the SICOFI, either a voltage divider in receive direction is needed or the AGR of the SICOFI has to be programmed to 6 dB analog attenuation.

The SLIC-program is written in FORTRAN and the user may modify this for his own SLIC. The program needs an inputfile with the values of the external circuit, and then it calculates the mixed matrix parameters and writes them into a SLIC-file. Together with the SICOFI-program you are able to calculate the SICOFI coefficients. If you set both resistors of the voltage divider equal, then you do not have a V_{OR} = 0.5, because the input impedance of the SLIC in receive direction is only 90 kΩ. If you need the exact V_{OR} you must calculate it or use a different circuit. In this case you can use the internal OP of the HARRIS-SLIC. Now you do not note the input impedance in receive direction, but you have shifted the signal. In this case you have to write V_{OR} = – 0.5 into the input file.

4 Comparison between Calculation and Measurement

The values of the measurement are confirmed by the calculation. The difference between both are small (see results of calculation and measurement in the appendix). Only the high attenuation of calculated echo return loss (> 35 dB) cannot be reached by measurement.

5 Appendix

On the next pages you will find the following details:

- HARRIS-SLIC HC 5502 FORTRAN program listing
- Calculated SICOFI-HARRIS SLIC transfer functions for the HARRIS-SLIC model. The values of the external HARRIS-SLIC components are listed on bottom at page...

Note: R = 300 Ω Input impedance of SLIC = 90000 Ω. In this case: V_{OR} = 0.5

- Measured SICOFI-HARRIS-SLIC transfer functions.

```
C******************************* TOP ******************************
C#################################################################
C
      PROGRAM HARRIS
C     6.04.88 Udo Stueting / Klaus Kliese
C#################################################################
        IMPLICIT LOGICAL (A-K, M-Z), CHARACTER (L)
*
        INTEGER IN, OUT, I
        CHARACTER*14 BUF1, BUF2*7, BUF3*7, BUF4*7, BUF5*7
        CHARACTER*7 BUF6, BUF7*7, BUF8*7, BUF9*7, BUFF2*12, BUFF3*12
        CHARACTER BUFF1*12, FILEOUT*12, ANSW*1, INFILE*12
        REAL*8 HA(2), HB(2), HC(2), HD(2), FREQ, R0, AR(2), AX(2)
        REAL*8 VOR,RIR,CKR,VOX,RIX,CKX,PI2,ZSLI
*
          COMMON /ARC/ RIR,CKR,VOR
          COMMON /AXC/ RIX,CKX,VOX
          COMMON /PI2C/ PI2
C
C*****************************************************************
C      Initialisation part
C*****************************************************************
C
```

```
      DATA BUF1/'* HARRIS SLIC '/
      DATA BUF2/'* VOR ='/,BUF3/'  RIR ='/,BUF4/' CKR ='/
      DATA BUF5/'* VOX ='/,BUF6/'  RIX ='/,BUF7/' CKX ='/
      DATA BUF8/'* R0  ='/,BUF9/' ZSLI ='/
*
        OUT = 6
        IN   =5
        PI2     = 4.*DASIN(1.D0)
        FILEOUT = ' '
            WRITE(OUT,'(A)')
    &      ' Enter input file name(xxxxxxxx.INP):  '
10          READ (IN,'(A)') INFILE
             IF (INDEX(INFILE,' ').EQ.1
    &          .OR.(INDEX(INFILE.'.INP').EQ.0
    &              .AND.INDEX(INFILE,'.inp').EQ.0 )) THEN
                 WRITE (OUT,'(A)') ' ENTER correct input file
name:  '
                 INFILE=' '
                GOTO 10
             ENDIF
        WRITE (OUT,'(A)') ' Enter output file name
(xxxxxxxx.SLI):   '
20     READ (IN,'(A)') FILEOUT
        IF (INDEX(FILEOUT,' ').EQ.1) THEN
            WRITE (OUT,'(A)')
    &     ' Enter correct output file name (with extention  .SLI):
            FILEOUT=' '
            GOTO 20
        ENDIF
```

```
      OPEN (30, FILE=FILEOUT, ERR=1000, STATUS= 'UNKNOWN')
           OPEN (10, FILE=INFILE, ERR=1100, STATUS= 'OLD')
           READ(10,'(A)')
           WRITE(6,*) 'Reading input file'
           READ(10,*) VOR
           READ(10,'(A)')
           READ(10,*) RIR
           READ(10,'(A)')
           READ(10,*) CKR
           READ(10,'(A)')
           READ(10,*) VOX
           READ(10,'(A)')
           READ(10,*) RIX
           READ(10,'(A)')
           READ(10,*) CKX
           READ(10,'(A)')
           READ(10,*) R0
           READ(10,'(A)')
           READ(10,*) ZSLI
           CLOSE (10)
C
C *****************************************************************
C      Documentation part
C *****************************************************************
C
      WRITE (30,'(A)') BUF1
      WRITE (BUFF1,'(G12.5)') VOR
      WRITE (BUFF2,'(G12.5)') RIR
      WRITE (BUFF3,'(G12.5)') CKR
      WRITE (30,'(A)') BUF2//BUFF1//BUF3//BUFF2//BUF4//BUFF3
      WRITE (BUFF1,'(G12.5)') VOX
      WRITE (BUFF2,'(G12.5)') RIX
      WRITE (BUFF3,'(G12.5)') CKX
      WRITE (30,'(A)') BUF5//BUFF1//BUF6//BUFF2//BUF7//BUFF3
      WRITE (BUFF1,'(G12.5)') R0
      WRITE (30,'(A)') BUF8//BUFF1
      WRITE (30,'(A)') 'ZSLI'
      WRITE (30,'(G12.5)') ZSLI
```

```
C*******************************************************************
C      Calculation parta
C*******************************************************************
C
C        M11 = 1. / R0
C
        WRITE (OUT,*) ' Running M11 calcuation...'
        WRITE (30,'(A)') 'M11-TABLE'
        D0 100 I=1,399
             FREQ = DBLE(I*10)
             HA(1)=1.D0/R0
             HA(2)= 0.
             WRITE (30,*) FREQ,HA(1),HA(2)
100     CONTINUE
C
C        M12 = –2.*AR / R0
C
        WRITE (OUT,*) ' Running M12 calcuation...'
        WRITE (30,'(A)') 'M12-TABLE'
        D0 110 I=1,399
             FREQ = DBLE(I*10)
             CALL ARW(FREQ,AR)
             HB(1) = -AR(1)*2.D0/R0
             HB(2) = -AR(2)*2.D0/R0
           WRITE (30,*) FREQ,HB(1),HB(2)
110     CONTINUE
C
C        M21 = AX
C
        WRITE (OUT,*) ' Running M21 calcuation...'
        WRITE (30,'(A)') 'M21-TABLE'
        D0 120 I=1,399
             FREQ = DBLE(I*10)
             CALL AXW(FREQ,AX)
             HC(1)= 1.*AX(1)
             HC(2)= 1.*AX(2)
             WRITE (30,*) FREQ,HC(1),HC(2)
120     CONTINUE
```

```
C       M22 = -2.*AX*AR
C
        WRITE (OUT,*) ' Running M22 calcuation...'
        WRITE (30,'(A)') 'M22-TABLE'
        D0 130 I=1,399
             FREQ = DBLE(I*10)
             CALL AXW(FREQ,AX)
             CALL ARW(FREQ,AR)
             CALL CMUL(AR,AX,HD)
             HD(1)= -2.*HD(1)
             HD(2)= -2.*HD(2)
             WRITE (30,*) FREQ,HD(1),HC(2)
130     CONTINUE
          WRITE(30,'(A1)') ';'
          CLOSE (30)
        WRITE(OUT,'(A)') ' Data written in file: '//FILEOUT
        STOP
1000    WRITE(OUT,'(A)') ' OPEN ERROR AT OUTPUT-FILE: '//FILEOUT
        STOP 1
1100    WRITE(OUT,'(A)') ' OPEN ERROR AT INPUT-FILE: '//INFILE
          STOP 2
        END
C
C####################################################################
C
      SUBROUTINE ARW(FREQ,AR)
C
C####################################################################
C
C     Name of Subroutine:     ARW
C
C     Formal parameter list:  FREQ,AR
C
C     Input parameters:
C        FREQ    (DOUBLE)
C
C     Output parameters:
C        ARW     (DOUBLE)   ARRAY  2
C
C     Task of this routine:  Calculation of transfer function in
C                            receive path for RC highpass and
C                            voltage devider VOR
C
C                                AR = VOR*jwRIR*CKR/(1.+jwRIR*CKR)
C                                with w = 2.*PI*FREQ
C
C####################################################################
```

```
          IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)
*
          INTEGER LUOUT
          LOGICAL LTEST
          REAL*8 AR(2),FREQ,RIR,CKR,VOR,OMP,PI2,V1(2),V2(2)
*
          COMMON /ARC/ RIR,CKR,VOR
          COMMON /PI2C/ PI2
*
          OMP   = PI2*FREQ*RIR*CKR
          V1(1) = 0
          V1(2) = OMP
          V2(1) = 1.D0
          V2(2) = OMP
          CALL CDIV(V1,V2,AR)
          AR(1) = AR(1)*VOR
          AR(2)  = AR(2)*VOR
          RETURN
          END
C###################################################################
C
      SUBROUTINE AXW(FREQ,AX)
C
C###################################################################
C
C     Name of Subroutine:     AXW
C
C     Formal parameter list:  FREQ,AX
C
C     Input parameters:
C        FREQ    (DOUBLE)
C
C     Output parameters:
C        AX       (DOUBLE)  ARRAY  2
C
C     Task of this routine:  Calculation of transfer function in
C                            transmit path for RC highpass
C
C                                AX = VOX*jwRIX*CKX/(1.+jwRIX*CKX)
C                                with w = 2.*PI*FREQ
C
C###################################################################
C
```

```
          IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)
*
          INTEGER LUOUT
          LOGICAL LTEST
          REAL*8 AX(2),FREQ,RIX,CKX,VOX,OMP,PI2,V1(2),V2(2)
*
          COMMON /AXC/ RIX,CKX,VOX
          COMMON /PI2C/ PI2
*
          AX(1) = VOX
          AX(2) = 0.
          OMP   = PI2*FREQ*RIX*CKX
          V1(1) = 0
          V1(2) = OMP
          V2(1) = 1.D0
          V2(2) = OMP
          CALL CDIV(V1,V2,AX)
          AX(1) = AX(1)*VOX
          AX(2) = AX(2)*VOX
          RETURN
          END
C####################################################################
C
      SUBROUTINE CMUL(C,D,E)
C
C####################################################################
C
C     Name of Subroutine:     CMUL
C
C     Formal parameter list:  C,D,P
C
C     Input parameters:
C         C       (DOUBLE)   ARRAY [2]
C         D       (DOUBLE)   ARRAY [2]
C
C     Output parameters:
C         E       (DOUBLE)   ARRAY [2]
C
C     Task of this routine:
C         SUBROUTINE COMPLEX MULTIPLICATION
C     Routine called in the following subroutines or functions:
C
C####################################################################
C
```

```
      IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
*
      REAL*8 C(2),D(2),P(2),E(2)
*
      P(1)=C(1)*D(1)-C(2)*D(2)
      P(2)=C(2)*D(1)-C(1)*D(2)
      E(1)=P(1)
      E(2)=P(2)
      RETURN
      END
C####################################################################
C
      SUBROUTINE CDIV(C,D,E)
C
C####################################################################
C
C     Name of Subroutine:     CDIV
C
C     Formal parameter list:  C,D,P
C
C     Input parameters:
C         C       (DOUBLE)   ARRAY [2]
C         D       (DOUBLE)   ARRAY [2]
C
C     Output parameters:
C         E       (DOUBLE)   ARRAY [2]
C
C     Task of this routine:
C         SUBROUTINE COMPLEX DIVISION
C
C     Routine called in the following subroutines or functions:
C
C####################################################################
C
      IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
*
      REAL*8 C(2),D(2),P(3),E(2)
*
      P(2)=D(1)*D(1)-D(2)*D(2)
      P(1)=C(1)*D(1)-C(2)*D(2)
      P(3)=C(2)*D(1)-C(1)*D(2)
*
      E(1)=P(1)/P(2)
      E(2)=P(3)/P(2)
      RETURN
      END
C
C*****************************BOTTOM*******************************
```

```
Input_file_name: HARRIS.CTL            Date: 18.04.88  10:32
SPEC = HARRIS.SPE                          SLIC = HARRIS.SLI
BYTE = REF.BYT      CHNR =  0,A
PLQ  = N

ON = ALL                      REL = Y                  SHORT = N
OPT =  Z+X+R+B                ZXRB =  NNNN
   FZ =  300.00       3400.0        ZLIM =  2.00
ZREP  =Y                           ZSIGN =  1
  FR =   300.00       3400.0
RFIL =  Y             RREFQ = N       RREF = 0.12220
  FX =   300.00       3400.0
XFIL =  Y             XREFQ = N       XREF = -5.9995
  FB =   300.00       3400.0        BLIM =  2.00 TBM =  1
BREP = Y                           BSIGN =  1
APOF =  0.00E+00 DPOF =  0.00E+00 APRE =  0.00E+00 DPRE =  0.00E+00
XZQ =  -0.55664062500000000E-01   0.54687500000000000E+00
        0.28906250000000000E+00  -0.24597167968750000E+00
        0.19531250000000000E+00
XRQ =  0.9531250000  0.0468750000 -0.0449218750
       0.0039062500 -0.0019531250

XXQ =  1.5000000000  0.6328125000  0.0771484375
       0.0283203125  0.0019531250

XBQ =  -0.97656250000000000E-01  -0.42187500000000000E+00
        0.15649414062500000E+00   0.16406250000000000E+00
       -0.85937500000000000E-01
       -0.54199218750000000E-01   0.77148437500000000E-01
       -0.30334472656250000E-01  -0.48828125000000000E-03
        0.40283203125000000E-02
XGQ =  0.5625000000  1.2812500000

;

Bytes for Z-Filter (13):               20,BA,EA,25,23,41,C1,BB
BYtes for R-Filter (2B):               D0,C8,84,DC,B1,93,02,1D
Bytes for X-Filter (23):               50,C8,B5,4A,C2,21,04,90
Bytes for Gain-factors (30):           A0,11,20,92
2nd part of bytes B-Filter (0B):       00,97,FD,C8,DD,4C,C2,BC
1st part of bytes B-Filter (03):       C4,12,23,32,72,B9,B2,BA
Bytes for B-filter delay (18):         19,19,11,19

* HARRIS SLIC_
* VOR = 0.50000      RIR =  90000.      CKR = 0.10000E-05
* VOX =  1.0000      RIX = 0.10000E+06  CKX = 0.10000E-05
* R0  =  600.00
```

```
Run #    1

Z-FILTER calculation results
  Generator impedance ZI at a,b line!
  Calculated and quantized coefficients:

XZ  =   -0.05549   0.54647   0.29193  -0.24595   0.19619
XZQ =   -0.05566   0.54687   0.28906  -0.24597   0.19531
Bytes for Z-Filter (13):    20,BA,EA,25,23,41,C1,BB

RETURN LOSS

  FREQ        loss                    FREQ        loss
  (Hz)        (dB)                    (Hz)        (dB)
   100.      36.621                   1800.      23.691
   200.      34.580                   1900.      24.104
   300.      32.126                   2000.      24.653
   400.      30.127                   2100.      25.360
   500.      28.533                   2200.      26.258
   600.      27.251                   2300.      27.391
   700.      26.214                   2400.      28.815
   800.      25.373                   2500.      30.567
   900.      24.695                   2600.      32.512
  1000.      24.157                   2700.      33.815
  1100.      23.740                   2800.      33.009
  1200.      23.435                   2900.      30.551
  1300.      23.232                   3000.      27.877
  1400.      23.128                   3100.      25.483
  1500.      23.119                   3200.      23.405
  1600.      23.207                   3300.      21.590
  1700.      23.395                   3400.      19.985

Min. Z-loop reserve:      3.290 dB
       at frequency:      500.0 Hz
Min. Z-loop mirror signal reserve:      8.343 dB
                     at frequency:     7500.0 Hz


Warning! SICOFI specs(noise,gain tracking...) not guaranteed
Increase SLIC gain in transmit path at least by      0.17dB
Run #    2

X-FILTER calculation results
  Calculated and quantized coefficients:

XX  =    1.49519   0.63652   0.07668   0.02832   0.00308
XXQ =    1.50000   0.63281   0.07715   0.02832   0.00195
Bytes for X-Filter (23):    50,C8,B5,4A,C2,21,04,90
```

X-filter attenuation function (in dB),(always absolute values)

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
300.	-6.912	0.048	1900.	-4.040	0.009
400.	-6.839	0.046	2000.	-3.794	0.006
500.	-6.747	0.045	2100.	-3.545	0.004
600.	-6.636	0.043	2200.	-3.292	0.001
700.	-6.507	0.041	2300.	-3.036	-0.001
800.	-6.361	0.039	2400.	-2.776	-0.004
900.	-6.200	0.037	2500.	-2.512	-0.007
1000.	-6.025	0.034	2600.	-2.243	-0.010
1100.	-5.837	0.031	2700.	-1.970	-0.014
1200.	-5.638	0.028	2800.	-1.694	-0.018
1300.	-5.429	0.025	2900.	-1.415	-0.023
1400.	-5.211	0.023	3000.	-1.135	-0.028
1500.	-4.987	0.020	3100.	-0.856	-0.033
1600.	-4.757	0.017	3200.	-0.583	-0.039
1700.	-4.522	0.014	3300.	-0.320	-0.045
1800.	-4.283	0.011	3400.	-0.071	-0.052
1900.	-4.040	0.009	3500.	0.048	0.000
2000.	-3.794	0.006	3600.	0.046	1.008

GX results:
All attenuation values (in dB) refer to FREF = 1014. Hz

RLX		SLIC+Z		VREF/VSICOFI		XREF		GX	
0.00	-	3.75	-	4.42	-	-6.00	=	-2.17	ideal
0.02	=	3.75	+	4.42	+	-6.00	+	-2.15	quant

Second byte for Gain: ,20,92
Calculation of transmit transfer function (AD)
All attenuation values (in dB) refer to FREF = 1014.0 Hz
Generator impedance ZI at a,b line!

TGREF CA = 0.259 ms   TGREF CB = 0.273 ms

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
100.	13.827	2.523	2000.	0.017	0.010
200.	0.339	1.786	2100.	0.011	0.015
300.	0.006	0.589	2200.	0.004	0.021
400.	0.028	0.287	2300.	-0.003	0.027
500.	0.025	0.166	2400.	-0.009	0.035
600.	0.016	0.103	2500.	-0.014	0.044
700.	0.007	0.067	2600.	-0.015	0.054
800.	0.001	0.044	2700.	-0.013	0.079
900.	-0.002	0.028	2800.	-0.006	0.079
1000.	-0.002	0.018	2900.	0.006	0.095
1100.	0.000	0.011	3000.	0.025	0.115
1200.	0.004	0.006	3100.	0.051	0.139
1300.	0.009	0.003	3200.	0.087	0.169
1400.	0.014	0.001	3300.	0.137	0.208
1500.	0.019	0.000	3400.	0.212	0.262
1600.	0.022	0.000	3500.	0.335	0.339
1700.	0.024	0.001	3600.	0.565	0.456
1800.	0.024	0.003	3700.	1.071	0.649
1900.	0.022	0.006	3800.	2.402	0.984

```
Run #    2

R-FILTER calculation results
  Calculated and quantized coefficients:

XR  =    0.95239   0.04758  -0.04485   0.00311  -0.00350
XRQ =    0.95312   0.04687  -0.04492   0.00391  -0.00195
Bytes for R-Filter (2B):    D0,C8,84,DC,B1,93,02,1D

R-filter attenuation function (in dB),(always absolute values)
```

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
300.	0.350	-0.004	1900.	0.008	0.010
400.	0.326	-0.003	2000.	0.026	0.010
500.	0.298	-0.002	2100.	0.051	0.010
600.	0.266	-0.001	2200.	0.085	0.010
700.	0.232	0.001	2300.	0.127	0.010
800.	0.197	0.002	2400.	0.177	0.009
900.	0.161	0.003	2500.	0.236	0.008
1000.	0.127	0.004	2600.	0.303	0.007
1100.	0.095	0.005	2700.	0.379	0.005
1200.	0.066	0.006	2800.	0.462	0.004
1300.	0.041	0.007	2900.	0.552	0.002
1400.	0.021	0.008	3000.	0.647	-0.001
1500.	0.006	0.009	3100.	0.746	-0.004
1600.	-0.003	0.009	3200.	0.846	-0.006
1700.	-0.006	0.010	3300.	0.945	-0.009
1800.	-0.002	0.010	3400.	1.039	-0.012
1900.	0.008	0.010	3500.	-0.004	0.000
2000.	0.026	0.010	3600.	-0.003	0.887

```
GX results:
All attenuation values (in dB) refer to FREF=    1014. Hz

   -RLR    SLIC+Z    VSICOFI/VREF    RREF          GR
   7.00 -   6.29  -      -4.42    -   0.12    =      5.01  ideal
   6.99 =   6.29  +      -4.42    +   0.12    +      5.00  quant

First byte for Gain (30):      A0,11
Calculation of receive transfer function (DA)
All attenuation values (in dB) refer to FREF =     1014.0 Hz
  Terminating impedance ZI at a,b line!

TGREF CA =   0.236 ms      TGREF CB =   0.219 ms
```

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
100.	-0.001	0.013	2000.	-0.010	0.041
200.	-0.001	0.002	2100.	-0.015	0.047
300.	-0.002	0.000	2200.	-0.021	0.054
400.	-0.002	0.000	2300.	-0.026	0.062
500.	-0.003	0.000	2400.	-0.029	0.071
600.	-0.003	0.001	2500.	-0.032	0.081
700.	-0.004	0.002	2600.	-0.031	0.093
800.	-0.004	0.004	2700.	-0.028	0.106
900.	-0.003	0.005	2800.	-0.020	0.121
1000.	-0.002	0.007	2900.	-0.007	0.139
1100.	0.000	0.009	3000.	0.012	0.160
1200.	0.001	0.011	3100.	0.039	0.186
1300.	0.003	0.013	3200.	0.078	0.219
1400.	0.004	0.016	3300.	0.136	0.261
1500.	0.004	0.019	3400.	0.225	0.317
1600.	0.003	0.022	3500.	0.373	0.397
1700.	0.001	0.026	3600.	0.642	0.516
1800.	-0.001	0.030	3700.	1.203	0.712
1900.	-0.005	0.035	3800.	2.612	1.049

```
Run #    2

B-FILTER calculation results
  Terminating impedance ZL at a,b line!

Calculated and quantized coefficients:

XB  =   -0.09979  -0.41835   0.15620   0.16296  -0.08400
        -0.05427   0.07695  -0.03033  -0.00038   0.00406
XBQ =   -0.09766  -0.42187   0.15649   0.16406  -0.08594
        -0.05420   0.07715  -0.03033  -0.00049   0.00403
2nd part of bytes B-Filter (0B):    00,97,FD,C8,DD,4C,C2,BC
1st part of bytes B-Filter (03):    C4,12,23,32,72,B9,B2,BA
```

TRANS HYBRID LOSS

FREQ (Hz)	loss (dB)	FREQ (Hz)	loss (dB)
100.	52.656	1800.	54.439
200.	45.934	1900.	54.867
300.	49.743	2000.	54.697
400.	51.739	2100.	54.142
500.	51.819	2200.	53.518
600.	51.108	2300.	53.043
700.	50.330	2400.	52.826
800.	49.712	2500.	52.922
900.	49.300	2600.	53.364
1000.	49.100	2700.	54.195
1100.	49.113	2800.	55.481
1200.	49.340	2900.	57.354
1300.	49.788	3000.	60.071
1400.	50.461	3100.	63.930
1500.	51.350	3200.	65.910
1600.	52.410	3300.	61.158
1700.	53.520	3400.	56.393

Additional B-filter delay (in seconds): .625E-04
Bytes for B-filter delay (18): 19,19,11,19

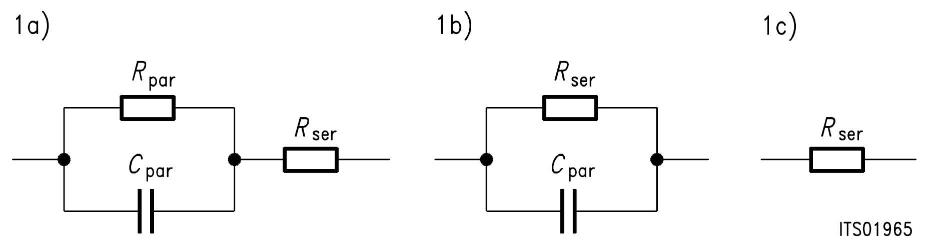


Figure 5

Equivalent Circuit Diagram 1

The configurations 1b) and 1c) can be derived from the equivalent circuit diagram 1a) by zeroing the elements that are not used.

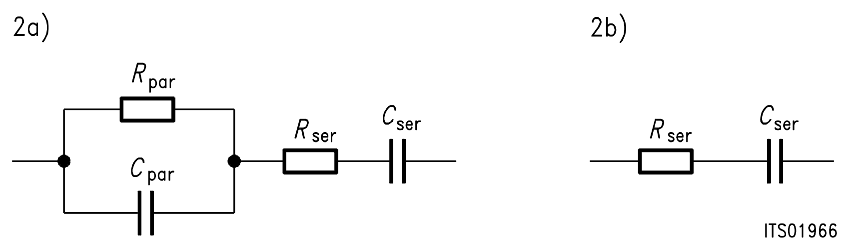


Figure 6

Equivalent Circuit Diagram 2

With R_{par} = 0 the entry of a series impedance 2b) becomes possible with equivalent circuit diagram 2a).

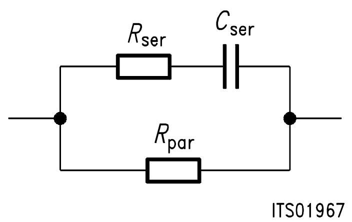


Figure 7

Equivalent Circuit Diagram 3

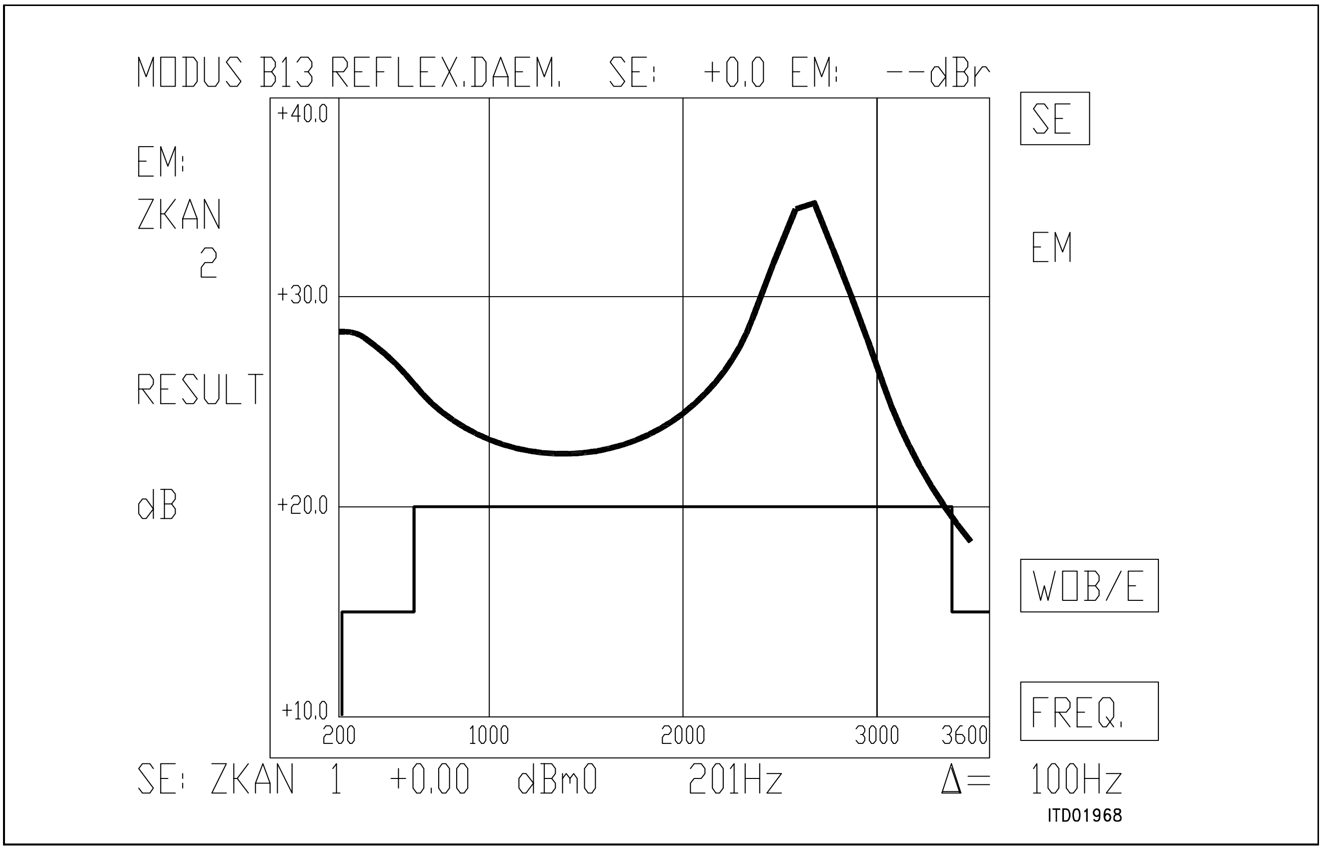


Figure 8

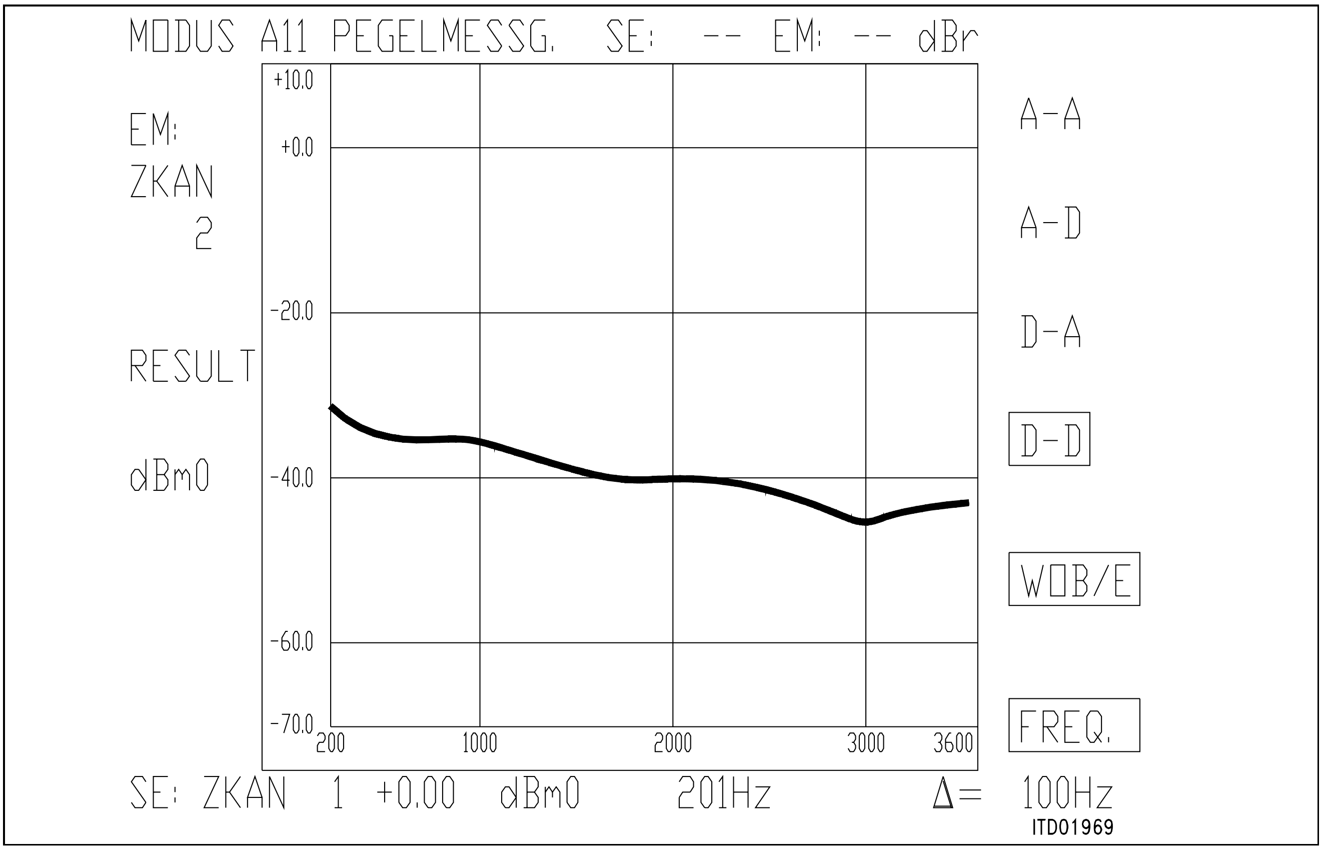


Figure 9

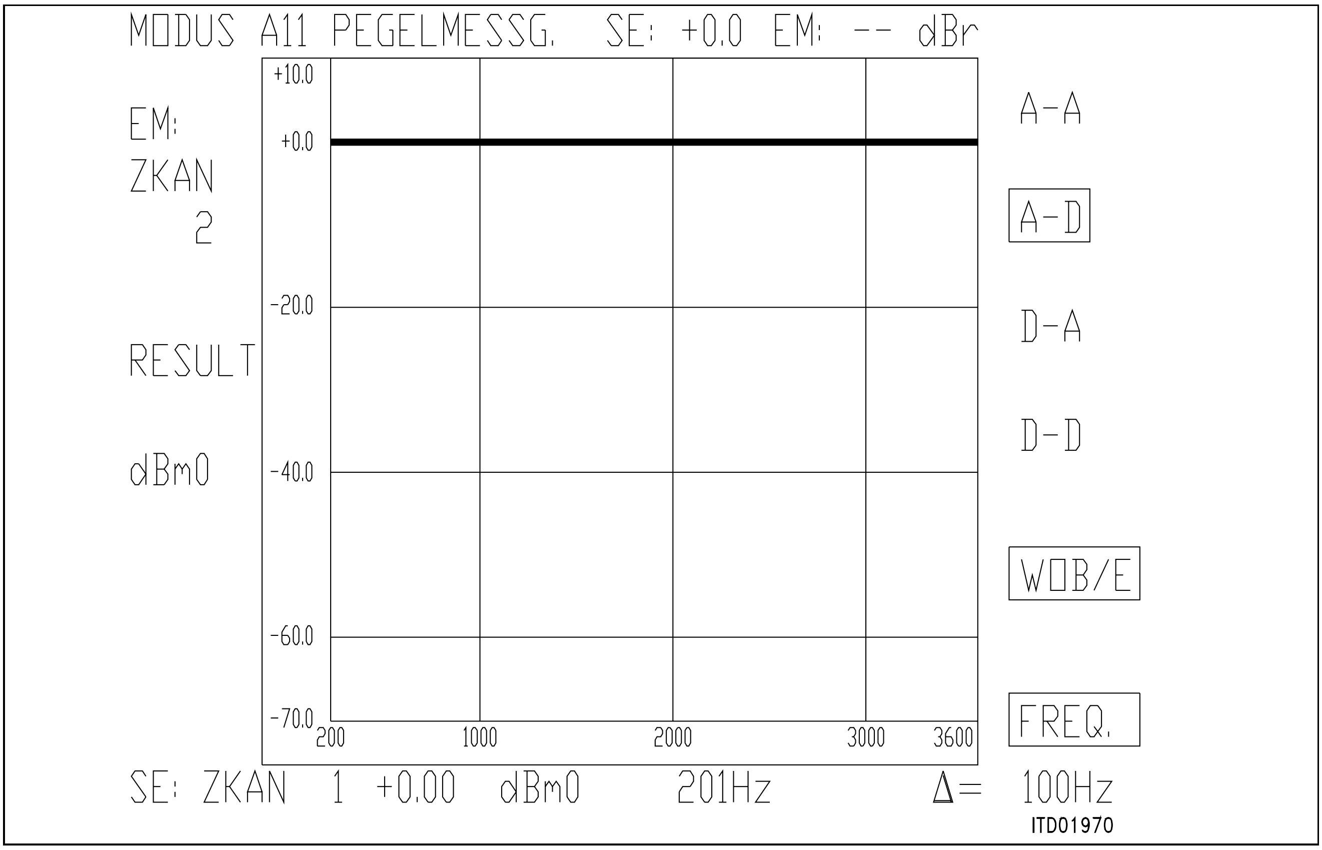


Figure 10

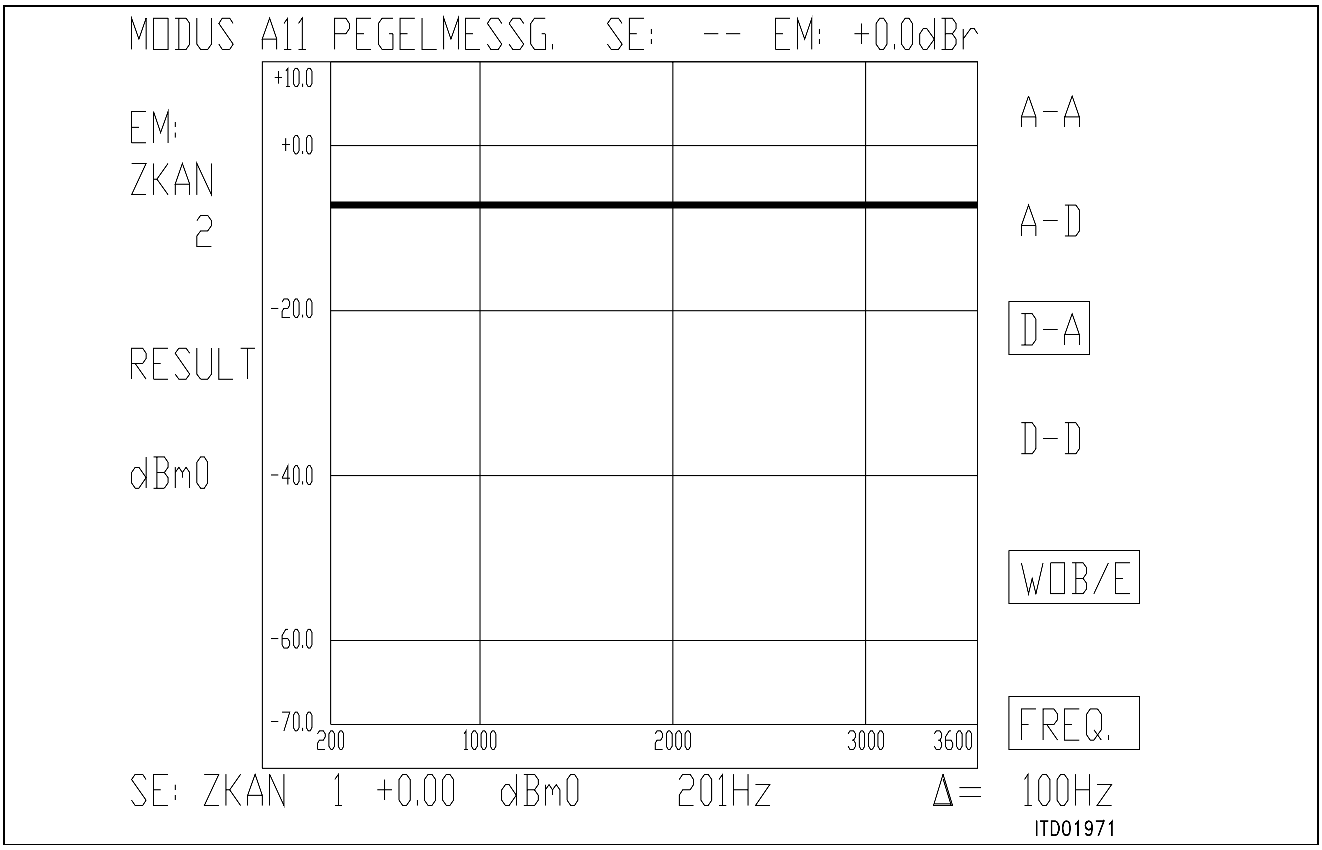


Figure 11

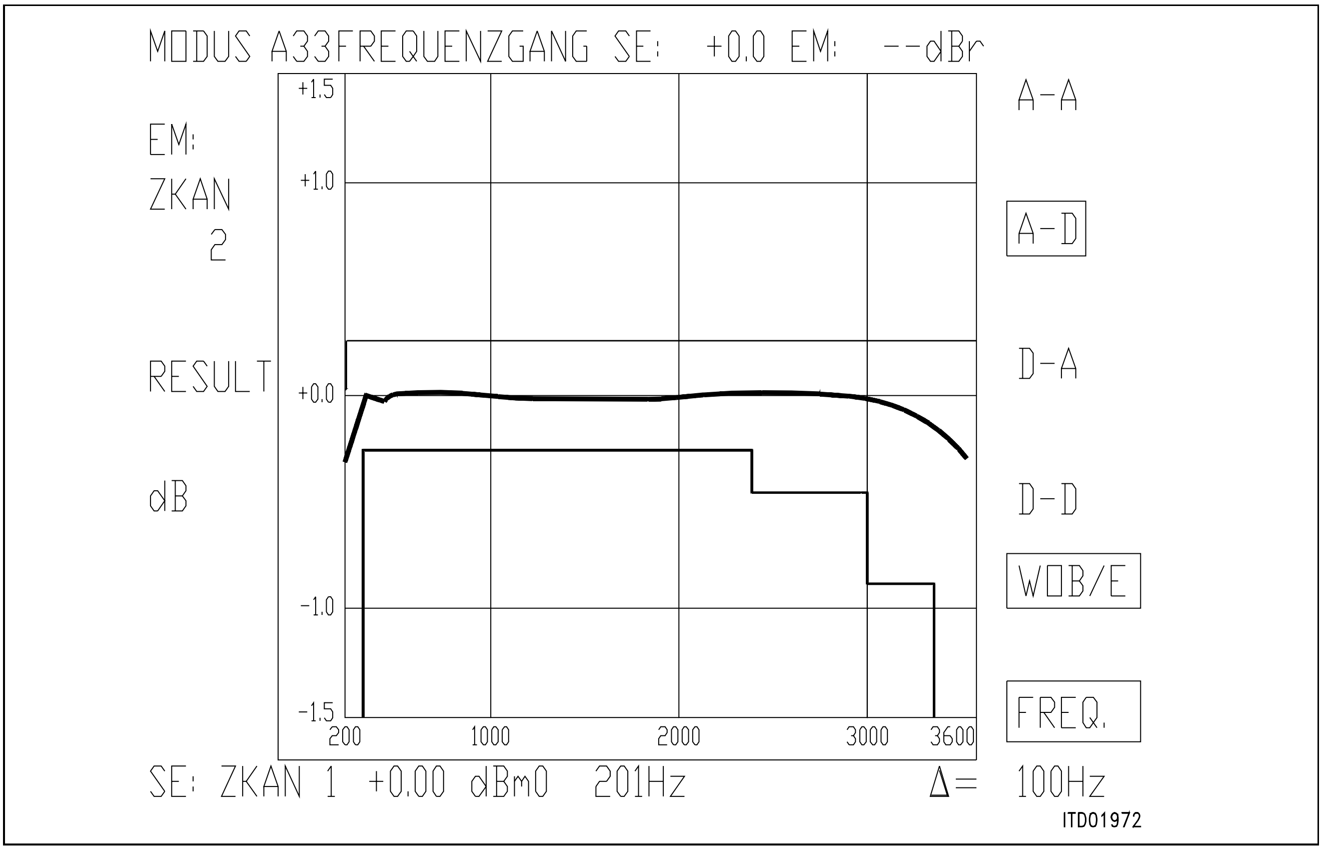


Figure 12

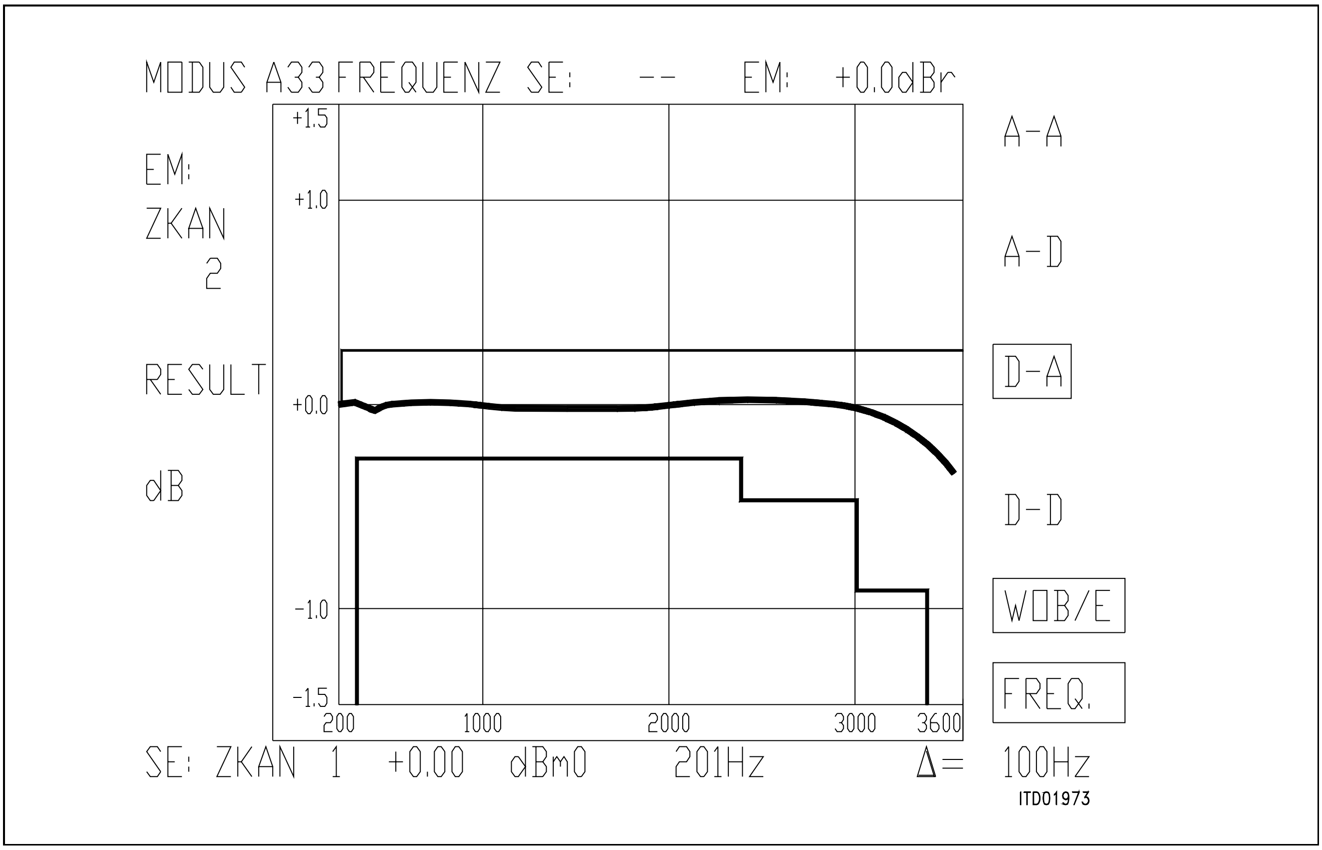


Figure 13

SICOFI® Application together with ERICSSON SLIC PBL 3762

Contents **Page**

1 Introduction

1.1 General

The introduction of digital switching systems has led to a significant reduction of the **central** part of the hardware constituent. In order to achieve further integration at the periphery, i.e. at the interface to the analog subscriber, the state of the art is to split up the analog subscriber circuit into a line driver and sensor chip (solid state SLIC: Subscriber Line Interface Circuit) on the one hand and a signal processor (in our case SICOFI) on the other; an even more cost effective possibility is to use a dual channel SICOFI (SICOFI-2) and two SLIC’s for a group of two analog subscribers.

In this note, we will call SLIC the combination of the solid state SLIC and the other discrete components which are not integrated and have an influence on the transmission characteristics.

We will call Subscriber Line MODULE the combination SLIC + SICOFI.

The aim of this paper is to describe an example of design of such a module for given specifications. It includes the corresponding hardware, the calculations necessary to build up a mathematical model of the SLIC, the software using this model and the results of the calculations with the SLIC and SICOFI software, which will permit to adapt the module to the specifications.

The Siemens **SI**gnal processing **CO**dec **FI**lter (SICOFI) PEB 2060 is a fully integrated PCM Codec (coder/decoder) and transmit/receive filter produced in an advanced low power CMOS technology.

It can be used in combination with a variety of solid state Subscriber Line Interface Circuits (SLIC).

This note describes an example of application with the ERICSSON SLIC PBL 3762 which allows a compact and low cost realisation of PABX subscriber line cards.

Other realisations (e.g. in central offices) are also possible with the full feature Ericsson SLIC’s PBL 3736 and 3739. The corresponding software will be included in an other application note.

The combination of SICOFI and PBL 3762 provides a costeffective solution because few external components are necessary and a high flexibility because of the flexibility of the digital signal processing:

– The ERICSSON PBL 3762 performs BORSCHT functions as loop current, resistive battery feed, ring relay driver and signaling functions as well as signal transmission including 2- to 4-wire and 4- to 2-wire conversion. The 2-wire termination impedance ("hybrid function" or "impedance matching") is adjustable by external impedances.
– The PEB 2060 (SICOFI) consists of several digital filters (Z,B,GR,GX,R and X-filters), which provide software controlled adjustment of the analog behavior of the digital switching system.
– These adjustments include improved hybrid function ("Z-filter"), transhybrid balancing function ("B-filter") as well as frequency correction ("R and X-filters") and level control in receive and transmit direction ("GR and GX-filters").

Furthermore the programmable parallel signaling inputs and outputs of the PEB 2060 (SICOFI) provides a flexible interface to the PBL 3762 signaling pins.

1.2 Overview

In the chapter 2, an example of design of a subscriber line interface module using the SICOFI and the PBL 3762 will be given (basic set-up).

The chapter 3 explains in details the calculation of a mathematical model of this SLIC.

This model allows to write a program described in chapter 4.

The program enables to calculate parameters describing the SLIC as a function of the frequency. With these parameters, coefficients can be calculated with the SICOFI coefficient program for the PEB 2060 (SICOFI) in chapter 5.

These coefficients have then to be programmed into the SICOFI.

Results of measurements are given in chapter 6.

The last chapter shows the good correlation between the calculated results and the measured ones for various configurations and specifications.

1.3 Glossary

PBX : Private Branch eXchange (USA)
PABX : Private Automatic Branch eXchange (= PBX in Europe)
C.O. : Central Office
SICOFI : PEB 2060
SICOFI software : See SICOFI software description
SLIC : ERICSSON PBL 3762
SLIC + SICOFI : Subscriber Line MODULE
(SLIC + SICOFI) + Peripheral Board Controller + Microprocessor
+ discrete components + ... (= all BORSCHT functions)
: Subscriber Line Interface Circuit
SLIC In our model : PBL 3762 + discrete components
BORSCHT : Battery feed
Overvoltage protection
Ringing
Supervision
Codec + filtering
Hybrid
Testing

2 BASIC Set-Up SICOFI®-PBL 3762

2.1 Circuit Diagram

The diagram of the basic set-up can be seen in **figure 1**.

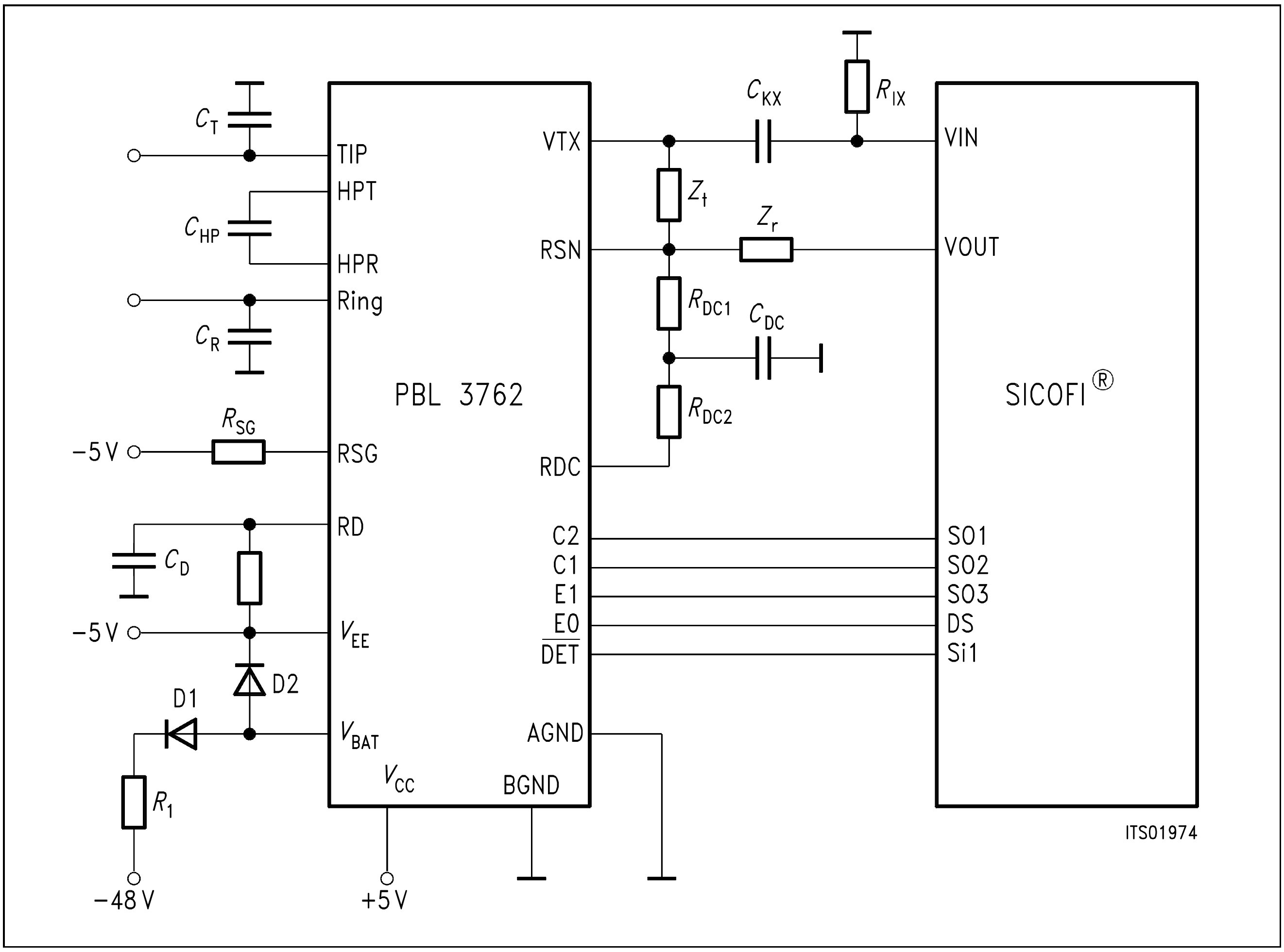


Figure 1

Basic Set-Up SICOFI® + ERICSSON PBL 3762

Parts list corresponding to **figure 1**.

Capacitors:

C_r	= 2.2 nF
C_t	= 2.2 nF
C_{HP}	= 10 nF
C_{DC}	= 3.3 µF
C_{KX}	= 1 µF
C_D	= 15 nF

Resistors: (1/4 W, 10% if not else specified)

Z_t	= 600 kΩ 0.5%
Z_r	= 300 kΩ 0.5%
R_{DC1}	= 20 kΩ
R_{DC2}	= 20 kΩ
R_{IX}	= 24 kΩ
R_{SG}	= 20 kΩ
R_D	= 39 kΩ
R_1	= 5.6 Ω

Diodes:

D1	= 1N4007
D2	= 1N4148

2.2 Application Hints

No attention has been paid to the overvoltage protection, signaling and loop monitoring functions in this application note because they should not influence the transmission characteristics.

Circuit Design

1. The capacitors C_t and C_r are used to stabilize the circuit at high frequencies; a value of 2.2 nF for both is correct.

2. The two impedances Z_t (matching impedance) and Z_r (gain impedance) have been exactly measured in order to make correct calculations. These are sensitive components and have to be precise (at least 1%).

3. The RSN pin is very sensitive to noise and therefore the leads to Z_t, R_{DC1} and Z_r should be kept as short as possible and close to the ground plane.

4. The C_{KX} capacitor and the R_{IX} resistor (decoupling circuit) are not necessary with the SICOFI version V4.x and later: The PBL 3762 DC offset is limitted to +/– 25 mV and the maximum allowed input DC offset of the SICOFI V4.x is +/– 50 mV.

5. A diode (D1) and a resistor (R_1) prevent having currents flowing in the wrong direction and limits the di/dt at the V_{Bat} pin of the PEB 3762.

6. A diode (D2) prevents V_{EE} to become lower than V_{Bat}. D1, D2 and R_1 may be shared by several SLIC's.

Control Inputs

The SICOFI PEB 2060 has three output signaling pins and four programmable signaling pins which allow an easy control of the two control pins C1 and C2 and of the two enable inputs E0 and E1 of the PBL 3762.

The DET output of the PBL 3762 is connected to the SI1 input pin of the SICOFI.

Connections

SICOFI		PBL3762
SO1	---------	C2
SO2	---------	C1
SO3	---------	E1
SD	---------	E0
SI1	---------	DET

With:

C2	C1	E1	E0	x	x	x	x	
SO1	SO2	SO3	SD	SC	SB	SA	SEL	
1	0	0	0	0	0	0	0	:= 80

in the SICOFI signaling byte, the SLIC is programmed in active state and DET as ground key status.

Loop Monitoring Functions

The loop current, ground key and ring trip detectors report their status via a common output: DET (pin 14).

The detector connected to DET is selected via the four bit wide control interface C2,C1,E1,E0.

The threshold for the loop current detector is set-up by the resistor R_D by the following formula:
I loop threshold = I_{lth} = 375 / R_D (Amperes)

In our application R_D = 39 kΩ gives I_{lth} = 9.6 mA.

C_D is then calculated by C_D = 0.5 ms / R_D.

For more details see the PBL 3762 data sheet.

Hybrid Function

There is no need of extra external components to build the echo attenuation path because this is taken care of by the SICOFI B-filter.a

AC-DC Decoupling Capacitor

The high pass filter capacitor C_{HP} connected between pin 1 and pin 22 of the PBL 3762 provides decoupling of circuits sensing tip-to-ring conditions and circuits processing AC signals.

C_{HP} should be choosen as high as possible in order to have a low cut off frequency:
$f_{CHP} = 1/(C_{HP} \times R_{HP} \times 2\pi)$.

R_{HP} is a PBL 3762 internal resistor with a value of 400 kΩ.

We have choosen a worst case (C_{HP} = 10 nF, f_{CHP} = 40 Hz) in our basic setup (**see circuit diagram in figure 1**).

A value of 33 nF for C_{HP} is counselled; it will position f_{CHP} at 14 Hz and so have less influence on the transmission characteristics.

Battery Feed and Saturation Guard

Case 1: Active state ($V_{tr} < V_{REF}$)

For a tip-to-ring voltage V_{tr} less than the saturation guard reference voltage V_{REF}, the SLIC emulates a resistive feed characteristic with an apparent battery voltage of 50 V (independent of the actual battery voltage V_{Bat} connected).

The voltage at the line is: $V_{tr} = 50 \times R_l / (R_l + (R_{DC1} + R_{DC2})/50)$ with R_L = loop resistance (DC).

For – 24 V < V_{Bat} < – 28 V, V_{REF} is correctly set with the pin RSG not connected. For higher battery voltages, V_{REF} may be adjusted to let resistive feed as described above remain in force until the tip-to-ring DC voltage approches the supply voltage.

Guide line:

Adjust $V_{REF} = 15.5 + 500\,000/R_{SG}$ to approximately: $V_{REF} = |V_{Bat}| - 8$ V i.e.:

$$R_{SG} = \frac{500\,000}{|V_{Bat}| - 8.0 - 15.5}$$

In our case V_{Bat} = – 48 V therefore R_{SG} = 20 kΩ.

Case 2: Active state and saturation guard ($V_{tr} > V_{REF}$)

When the tip-to-ring voltage V_{tr} exceeds V_{REF}, the feed characteristic changes in order to prevent the line drive amplifiers from distorting the AC signal (may occur by insufficient amplifier bias voltages).

This has an influence on the transmission characteristics, especially on the return loss.

Case 3: $C_1 = C_2 = 1$

With the SLIC in disabled state ("stand by") a high resistance feed characteristic is enabled.

DC Path

The DC feed resistance is programmed by two resistors R_{DC1} and R_{DC2} connected in series to the receive summing node (RSN) and decoupled from AC by the capacitor C_{DC} (recommended cutoff frequency: 14 Hz).

This has only a small influence on the transmission caracteristics depending on the cutoff frequency value of the system R_{DC1}, R_{DC2}, C_{DC}.

3 Mathematical Model

3.1 Circuit Model

A software emulation of the SLIC is necessary in order to produce a file of the so-called **"K-parameters"** (see **chapter 3.4.1**) to interface with the SICOFI program.

We need first to calculate a mathematical model of the SLIC which will then be used to write a SLIC program (see **chapter 4**).

This model must include all external components which influence the transfer functions of the whole circuit.

Therefore in the next pages we will call SLIC the part of our basic setup composed by all analog external components and by the PBL 3762.

The resistors and capacitors of the circuit drawing are transformed in complex impedances in order to be as general as possible (see impedance model in chapter 4.3).

For more details about the ERICSSON SLIC model see the PBL 3762 data sheet.

Figure 2 shows the grounded model which has been choosen for its simplicity.

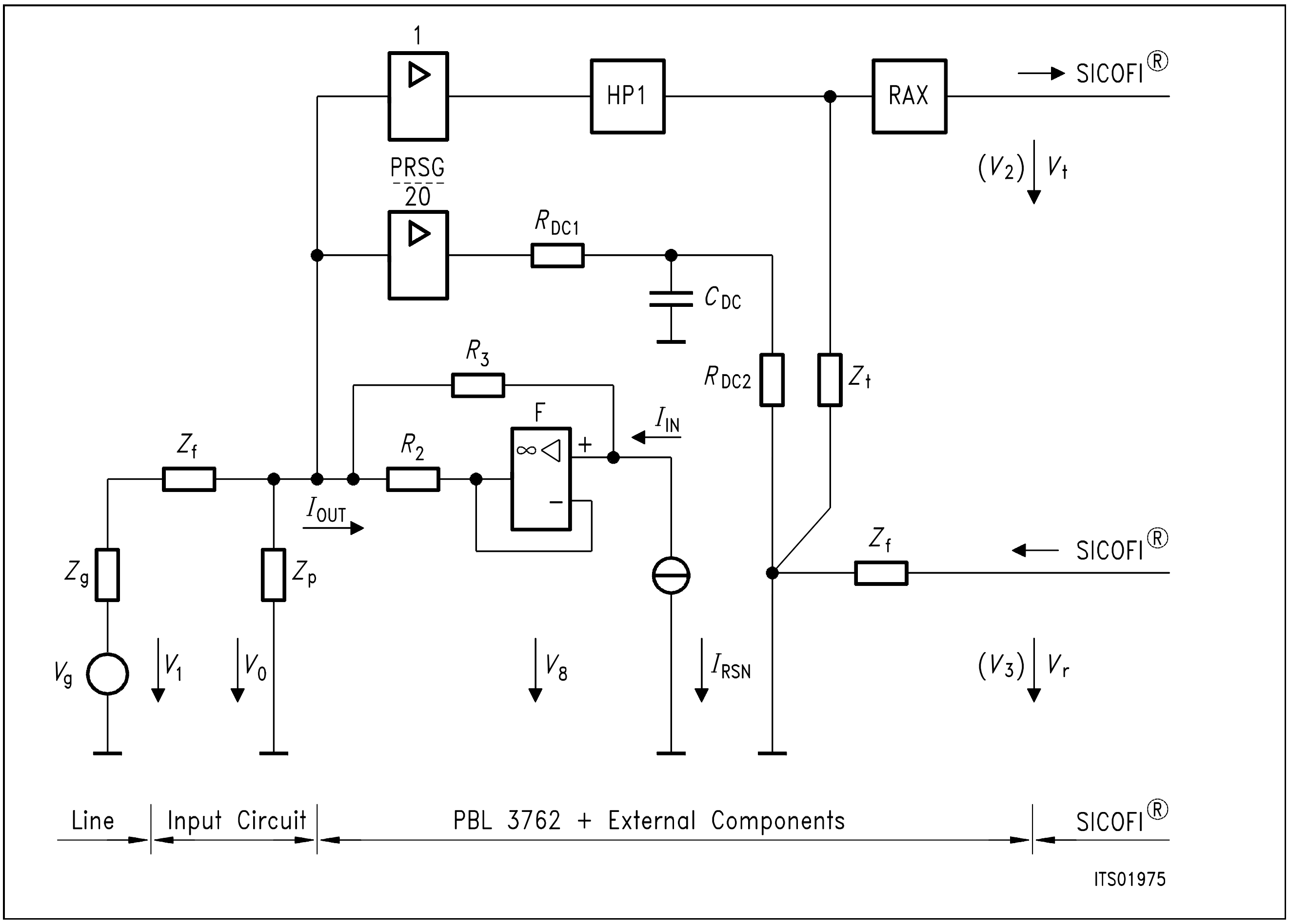


Figure 2

Equivalent Model of the SLIC

3.2 Preliminary Data and Symbols Meaning

The values of the different parameters from figure 2 are listed hereunder:

R_2	= 20 Ω	gain setting of output current amplifier
R_3	= 9.98 kΩ	gain setting of output current amplifier
C_{HP}	= 10 nF	high pass filter in transmit direction
R_{HP}	= 400 kΩ	high pass filter in transmit direction
R_{DC1}	= 20 kΩ	DC path
R_{DC2}	= 20 kΩ	DC path
C_{DC}	= 3.3 µF	DC path
Z_t	= 600 kΩ	matching impedance

Z_r	= 300 kΩ	gain impedance (gain 4w – 2w # – Z_t / 2 × Z_r)
Z_p	= 2.2 nF	parallel impedance at (a,b) line: This grounded impedance will be doubled in the program PBL 3762. FOR because there are two of them at the SLIC input.
Z_f	= 20 Ω	fuse impedance
Z_g	= 600 Ω	line/generator AC impedance
RAX		DC decoupling circuit in transmit direction
PRSG		coefficient for saturation guard (7 when saturation guard, 1 normally)

f_{CDC}: cut-off frequency of the DC low pass filter

$$f_{CDC} = \frac{1}{((R_{DC1}+R_{DC2})/2) \times C_{DC} \times 2\pi)}$$

HP1: high pass filter in transmit direction

$$HP1 = \frac{j \times 2 \times \pi \times f \times C_{HP} \times R_{HP}}{1 + j \times 2 \times \pi \times f \times C_{HP} \times R_{HP}} = \frac{1}{1 - j \times f_{CHP} / f}$$

RAX: Decoupling circuit in transmit direction

RAX = j × C_{KX} × R_{IX} × OMEGA / (1. + j × C_{KX} × R_{IX} × OMEGA)

PRSG: Saturation guard:

$$HSG = \frac{Z_T \times PRSG}{20. \times ((R_{DC1} + R_{DC2}) / 2) \times (1 + j \times f / f_{CDC})}$$

X: Total correction factor

1/X = HP1 + HSG

The AC output stage of the PBL 3762 is a current controlled current source (CCS) which amplifies the current at the RSN summing point (I_{RSN}) and which is loaded by the input circuit.

F: Open loop gain of the current amplifier

F = 10000. / (1. + j × f/100)

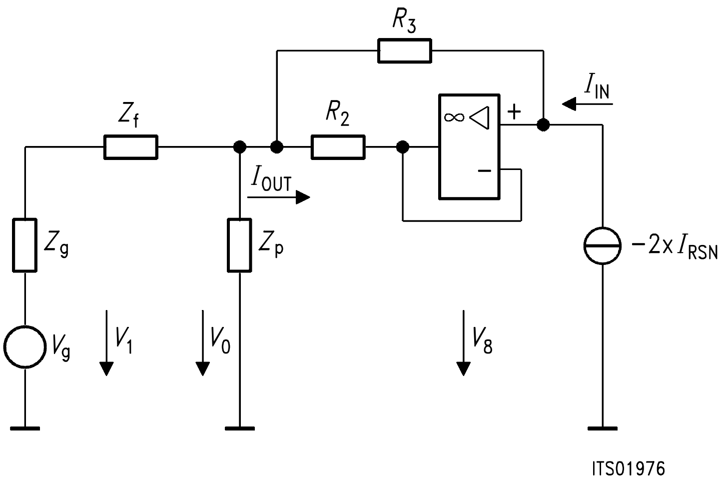


Figure 3

Current Controlled Current Source Amplifier (CCS) and Input Circuit

3.3 Input Circuit

The **figure 4** shows the input circuit of the SLIC where Z_{OUT} is the equivalent output impedance of the CCS.

The equivalent impedance (Z_{eq}) of the input circuit needs to be calculated:

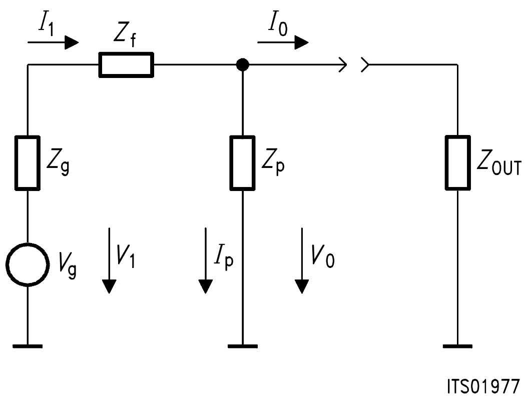


Figure 4

Equations:

$I_0 = I_1 - I_p$ (10)

$V_0 = -I_1 \times (Z_g + Z_f) + V_g$ (11)

$I_p = V_0 / Z_p$ (12)

$I_0 = -V_0 / Z_{OUT}$ (13)

$V_0 = Z_p \times I_p$ (12)

From (10) & (11) & (12), we can deduce:

$I_0 = V_0 / Z_p + V_g / Z_g - (V_g - V_0) / (Z_g + Z_f)$

that is:

$$I_0 = V_g / (Z_g + Z_f) - V_0 / Z_{eq} \quad (14)$$

with

$$Z_{eq} = Z_p // (Z_g + Z_f) \quad (15)$$

3.4 Calculations

The PBL 3762 has a current output; therefore we need to work with the K-parameters which do not require to short-circuit the output (for more information about these parameters see the SICOFI software description).

3.4.1 K-Parameters

A SLIC with a symmetrical generator V_g and a symmetrical line impedance Z_g can be considered as a circuit accessible through the currents and voltages of a three port: (V_1, I_1), (V_2, I_2), (V_3, I_3).

Three equations are sufficient to describe the SLIC completely and any linear combination of the variables is possible.

Let us take the following combination:

(100) a1 = $V_1 + Z_g \times I_1$

(200) b1 = $V_1 - Z_g \times I_1$

Then using these new variables, the model of the SLIC becomes:

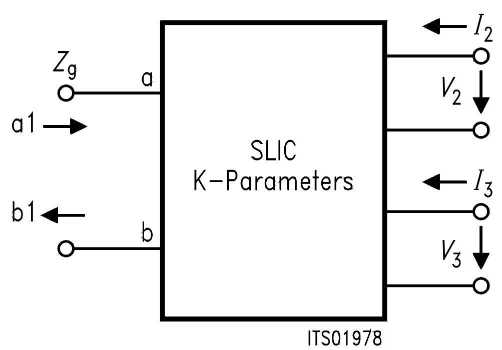


Figure 5

K-1 Three Port Model with the Variables a1 and b1

Following equations can now be written:

(300) b1 = K11 × a1 + K12 × V_3 + K13 × I_2

(400) V_2 = K21 × a1 + K22 × V_3 + K23 × I_2

(500) I_3 = K31 × a1 + K32 × V_3 + K33 × I_2

When the SLIC is connected to the SICOFI, we can assume that:
*I_2 = 0 because the input impedance of SICOFI is very high.
*I_3 is not relevant in the SICOFI calculations.

According to these remarks, the equations system can be simplified as follow:

(600) b1 = K11 × a1 + K12 × V_3

(700) V_2 = K21 × a1 + K22 × V_3

Parameter K11

Equation (600) gives K11 = b1/a1 when $V_3 = 0$

From (100) and (200) we can deduce:

$$b1/a1 = (V_1 - Z_g \times I_1) / (V + Z_g \times I_1)$$
$$= (V_1 / I_1 - Z_g) / (V_1 / I_1 + Z_g)$$

Let us call Z_{IN} the input impedance of the SLIC:

$$Z_{IN} = V_1 / I_1$$

Therefrom

$$K11 = (Z_{IN} - Z_g) / (Z_{IN} + Z_g) \text{ for } V_3 = 0$$

Parameter K12

$$K12 = b1 / V_3 \text{ when } a1 = 0$$

From (100) follows:

$$V_1 + Z_g \times I_1 = 0$$

i.e. $V_1 = - Z_g \times I_1$

Thus

$$b1 = V_1 - Z_g \times I_1 = V_1 + V_1$$

Therefrom

$$K12 = 2 \times V_1 / V_3 \text{ for } V_1 = - Z_g \times I_1$$

Parameter K21

$$K21 = V_2 / a1 \text{ when } V_3 = 0$$

In this case:

$$a1 = V_1 + Z_g \times I_1 = V_g$$

Then

$$K21 = V_2 / V_g \text{ for } V_3 = 0$$

Parameter K22

From (100) and a1 = 0 follows: $V_1 = - Z_g \times I_1$
And we can deduce from (700) and a1 = 0:

$$K22 = V_2 / V_3 \text{ for } V_1 = - Z_g \times I_1$$

Remarks:

1. All these parameters are accessible by measurement with a symmetrical ground free generator and a complex voltmeter.

2. $R_L = - 20 \times \log10 (|K11|)$ is nothing else than the return loss of the SLIC without SICOFI.

3.4.2 Starting Equations

Using the data given by ERICSSON one can write the following starting equations:

Cf figure 2 and figure 3

(1) $V_8 = (V_i - V_8) \times F$

(2) $I_0 = (V_0 - V_t) / R_2 - I_i$

(3) $I_0 = V_g / (Z_g + Z_f) - V_0 / Z_{eq}$

(4) $V_i = V_0 + I_i \times R_3$

Current summation point RSN:

(5) $$I_i = -2 \times \left(\frac{V_0}{Z_t \times \text{HP1} \times \text{RAX}} + \frac{\text{RAR} \times V_r}{Z_r} + \frac{V_0}{\text{HRSG}} \right)$$

(6) $$F = \frac{1E + 04}{1 + j \times f / 100}$$ (open loop gain)

(7) $G = -I_i / I_0$ (total current gain)

(8) $V_1 = V_g - Z_g \times I_1$

The transmit path is simply described by:

(9) $V_t / V_0 = \text{RAX} \times \text{HP1}$

3.4.3 Calculation of K11

K11 is defined by $(Z_{IN} - Z_g) / (Z_{IN} + Z_g)$

(1) & (4) → $$V_8 = \frac{F}{(1 + F)} \times (V_0 + I_i \times R_3) \quad (20)$$

(20) & (2) → $$I_0 = \frac{V_0}{R_2} - \frac{F \times V_0}{R_2 \times (1 + F)} - \frac{F \times I_i \times R_3}{R_2 \times (1 + F)} - I_i$$

$$I_0 = \frac{V_0 - F \times R_3 \times I_i - R_2 \times (1 + F) \times I_i}{R_2 \times (1 + F)} \quad (21)$$

($V_r = 0$) & (5) → $$I_i = -\frac{2 \times V_0}{Z_t \times X} \quad (22)$$

Where 1/X = HP1 + HSG

(22) and (21) → $$I_0 = \frac{V_0 \times Z_t \times X + V_0 \times 2 \times F \times R_3 + V_0 \times 2 \times R_2 \times (1 + F)}{R_2 \times Z_t \times X \times (1 + F)}$$

$V_0 / I_0 = 1 / Z_{OUT}$

$$1 / Z_{OUT} = \frac{2 \times F (R_2 + R_3) + 2 \times R_2 + Z_T \times X}{Z_t \times X \times R_2 \times (1 + F)} \quad (23)$$

$$1 / Z_P = j \times f \times C_{tr} \times 2\pi \quad (24)$$

$Z_{IN} = Z_f + Z_p \,/\!/\, Z_{OUT}$ (25)

$$K11 = (Z_{IN} - Z_g) / (Z_{IN} + Z_g) \quad (26)$$

3.4.4 Calculation of K12

K22 is defined by: $2 \times V_1 / V_3$ when $V_g = 0$

Let us calculate first the current gain G (**cf figure 3**):

$(V_g = 0)$ & (3) → $V_0 = - I_0 \times Z_{eq}$ (30)

(30) & (2) → $R_2 \times (I_0 + I_i) + V_8 = I_0 \times Z_{eq}$ (31)

(1) ↔ $V_8 = V_i \times F / (1 + F)$ (32)

(4) → $V_I = - I_0 \times Z_{eq} + I_i \times R_3$

(32) & (4) & (31) → $R_2 \times (I_0 + I_i) + (- I_0 \times Z_{eq} + I_I \times R_3) \times F / (1 + F) = - I_0 \times Z_{eq}$

$$I_0 \times (R_2 \times (1 + F) + Z_{eq}) = I_I \times (R_2 \times (1 + F) - R_3 \times F) \quad (33)$$

$$G = - I_0 / I_i = \frac{R_3 \times F + R_2 \times (1 + F)}{R_2 \times (1 + F) + Z_{eq}} \quad (34)$$

calculation of V_0 / V_r:

$(V_g = 0)$ & (3) → $I_0 = - V_0 / Z_{eq} = - I_i \times G$ (35)

(35) & (5) → $V_0 / (G \times Z_{eq}) = - 2 \times V_0 / (Z_t \times X \times RAX) - 2 \times V_r / Z_r$ (36)

and by regrouping the terms in V_0 and V_r:

$$\frac{V_0}{V_r} = \frac{- 2 \times G \times Z_{eq} / Z_r}{1 + 2 \times G \times Z_{eq} / Z_t \times X \times RAX} \quad (37)$$

we have to calculate now V_1 / V_0:

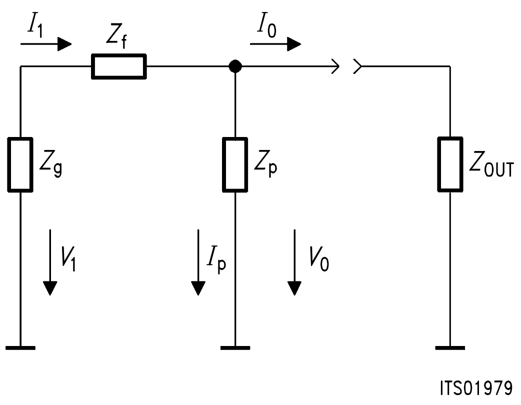


Figure 6

Z_f and Z_g form a voltage divider; the calculations are then straightforward:

$$V_1 / V_0 = Z_g / (Z_g + Z_f) \qquad (38)$$

Thus

(37) & (38) →

$$2 \times V_1 / V_r = \frac{Z_g}{Z_g + Z_f} \times \frac{-2 \times 2 \times G \times Z_{eq} / Z_r}{1 + 2 \times G \times Z_{eq} / Z_t \times X \times RAX} \qquad (39)$$

3.4.5 Calculation of K21

K21 is defined by V_t / V_g when $V_r = 0$

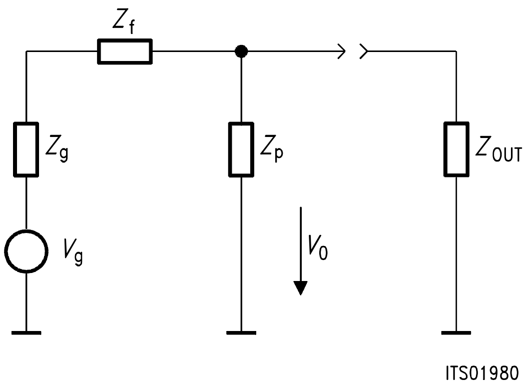


Figure 7

we have a simple voltage divider:

$$\frac{V_g}{Z_f + Z_g + Z_p / Z_{OUT}} = \frac{V_0}{Z_p // Z_{OUTt}} \qquad (40)$$

$$V_t / V_g = (V_t / V_0) \times (V_0 / V_g)$$

hence:

(40) & (9) →

$$V_t / V_g = \frac{RAX \times HP1 \times (Z_p // Z_{OUT})}{Z_f + Z_g + (Z_p // Z_{OUT})} \qquad (41)$$

3.4.6 Calculation of K22

K22 is defined by V_t / V_r when $V_g = 0$

(37) & (9) →

$$V_t / V_r = RAX \times HP1 \times \frac{-2 \times G \times Z_{eq} / Z_r}{1 + 2 \times G \times Z_{eq} / Z_t \times X \times RAX} \qquad (50)$$

3.5 Summary

$$1 / Z_{OUT} \quad \frac{2 \times F (R_2 + R_3) + 2 \times R_2 + Z_T \times X}{Z_T \times X \times R_2 \times (1 + F)} \tag{23}$$

$$Z_{IN} = Z_f + Z_p // Z_{OUT} (25)$$

$$K11 = (Z_{IN} - Z_g) / (Z_{IN} + Z_g) \tag{26}$$

$$Z_{eq} = Z_p // (Z_g + Z_f) \tag{15}$$

$$K12 \quad \frac{Z_g}{Z_g + Z_f} \times \frac{-2 \times 2 \times G \times Z_{eq} / Z_r}{1 + 2 \times G \times Z_{eq} / Z_t \times X \times RAX} \tag{39}$$

$$K21 \quad \frac{RAX \times HP1 \times (Z_p // Z_{OUT})}{(Z_p // Z_{OUT}) + Z_f + Z_g} \tag{41}$$

$$K22 = RAX \times HP1 \times \frac{-2 \times G \times Z_{eq} / Z_r}{1 + 2 \times G \times Z_{eq} / Z_t \times X \times RAX} \tag{50}$$

R_2	= 20 Ω	gain setting of output current amplifier
R_3	= 9.98 kΩ	gain setting of output current amplifier
C_{HP}	= 10 nF	high pass filter in transmit direction
R_{HP}	= 400 kΩ	high pass filter in transmit direction
R_{DC1}	= 20 kΩ	DC path
R_{DC2}	= 20 kΩ	DC path
C_{DC}	= 3.3 µF	DC path
Z_t	= 600 kΩ	matching impedance
Z_r	= 300 kΩ	gain impedance (gain 4w – 2w # $- Z_t / 2 \times Z_r$)
Z_p	= 2.2 nF	parallel impedance at (a,b) line
Z_f	= 20 Ω	fuse impedance
Z_g	= 600 Ω	line/generator AC impedance
RAX		decoupling circuit in transmit direction (high pass C_{KX}, R_{IX})
PRSG		coef. for saturation guard (7 when saturation guard, 1 normally)

f_{CDC} : cut-off frequency of the DC low pass filter

$$f_{CDC} \quad \frac{1}{((R_{DC1} + R_{DC2}) / 2) \times C_{DC} \times 2\pi)}$$

HP1 : high pass filter in transmit direction

$$HP1 \quad \frac{j \times 2\pi \times f \times C_{HP} \times R_{HP}}{1 + j \times 2\pi \times f \times C_{HP} \times R_{HP}}$$

$$\frac{1}{1 - j \times f_{CHP} / f_{req}}$$

RAX : connection circuit in transmit direction

RAX $= j \times C_{KX} \times R_{IX} \times$ OMEGA / (1. + j $\times C_{KX} \times R_{IX} \times$ OMEGA)

HSG : Saturation guard

$$\text{HSG} \quad \frac{Z_T \times \text{PRSG}}{20. \times ((R_{DC1} + R_{DC2}) / 2) \times (1 + j \times f / f_{CDC})}$$

X : total correction factor

1 / X = HP1 + HSG

I_i : current summation point RSN

$$I_i = -2 \times \left(\frac{V_0}{Z_t \times \text{HP1} \times \text{RAX}} + \frac{\text{RAR} \times V_r}{Z_r} + \frac{V_0}{\text{HRSG}} \right) \quad (5)$$

F : open loop gain of current amplifier

$$F = \frac{10\,000}{1 + j \times f_{REQ} / 100} \quad (6)$$

G : total current gain:

$$G = -I_i / I_0 \quad (7)$$

V_1 : voltage at (a,b) line:

$$V_1 = V_g - Z_g \times I_1 \quad (8)$$

The transmit path is simply described by:

$$V_t / V_0 = \text{RAX} \times \text{HP1} \quad (9)$$

4 Software

Each K-parameter is expressed in the PBL 3762.FOR program as an algebraic equation, combination of the various SLIC parameters which are provided by the SLIC input file PBL 3762.INP.

According to the values of the SLIC input data, the SLIC program PBL 3762.EXE calculates the values of the K-parameters in function of the frequency and writes them in an output file PBL 3762.SLI. This file will be used by the SICOFI program to calculate the coefficients for the PEB 2060 (for more information about the use of the SICOFI program see the SICOFI software description).

Explanations about the input file and the subroutines of the program are given in the following pages as well as a listing of the source file (ERIC.FOR).

Please note that the program has been written in FORTRAN (and compiled with the Microsoft FORTRAN optimizing compiler); therefore it is important to respect the FORTRAN convention of using a "." (POINT) for each REAL value.

4.1 Input File

The input file PBL 3762.INP is listed hereunder:

```
test (T:test=>amplitude and phase of Kij;  x:normal calculation)
x
*ZfRa1, ZfCA1, ZfCA2, ZfRA2, ZfRS, ZfCS   : fuse impedance Zf
  0.   0.      0.      0.    20.2  0.
*ZtRA1, ZtCA1, ZtCA2, ZtRA2, ZtRS, ZtCS   : matching impedance Zt
598.E+03  0.   0.     0.     0.    0.
*ZrRA1, ZrCA1, ZrCA2, ZrRA2, ZrRS, ZrCS   : gain impedance Zr
300.E+03  0.   0.     0.     0.    0.
CHP : capacitor for internal high pass
10.18E-09
*ZpRA1, ZpCA1, ZpCA2, ZpRA2, ZpRS, ZpCS   : parallel impedance Zp
                                            (= Ct = Cr)
0.      0.     0.     0.     0.    2.24E-09
CKX = High pass in transmit direction
0.98E-06
RIX = High pass in transmit direction
23.7E+03
RDC1          RDC2          CDC           : DC path
20.40E+03     20.4E+03      3.33E-06
PRSG = Saturation guard (Yes = 7. no = 1.)
1.
*ZSLI = Half loop attenuation
0.5
*Zg : source/line impedance  (with 6 elements )
*ZgRA1, ZgCA1, ZgCA2, ZgRA2, ZgRS, ZgCS
600.   0.   000.E-00   0.    000.  0.
```

Remark:
Because the line impedance is embedded in the K-parameters, the SLIC file has to be recalculated every time the line impedance is changed.

4.2 Test Mode

TEST = "T"
In order to make a rough adaptation of the PBL 3762 to the required specifications, it is interesting to work first with the SLIC alone without SICOFI and to be able to view the different transfer functions and the input impedance.

A test mode was therefore inserted in the SLIC program:

When the switch TEST equals "T", the program writes the amplitude and phase (polar coordinates) of the input impedance and of all Kij parameters as a function of the frequency in the output file PBL 3762.SLI at 100 Hz steps.

The transformation cartesian to polar coordinates is made by the subroutine CPOL.

If TEST is other than "T" (default mode) then the program calculates the K-parameters for the SICOFI program. Real and imaginary part (cartesian coordinates) are written as a function of the frequency to the output file PBL 3762.SLI at 10 Hz steps.

4.3 Model for Impedances

In order to match any specification with the SICOFI + SLIC circuit, all the impedances Z_t, Z_f, Z_r, Z_p and Z_g can have complex values (**see figure 1 and figure 2**). They are described in the subroutine IMPED6 using 6 resistors and capacitors; a component value set to 0 means that this component does not exist.

The equivalent circuit diagram is the following:

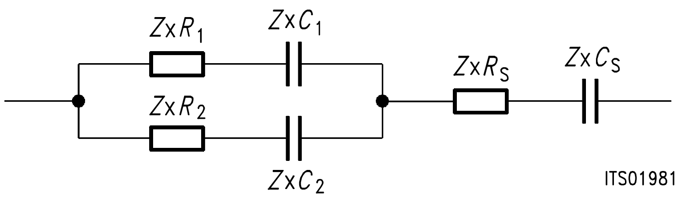


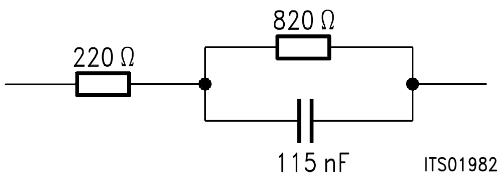
Figure 8

where * stands for f, t, r, g or b. *R* means resistor; *C* means capacitance; S means series. These values are read from the input file.

Example:

*Zg : source/line impedance (with 6 elements)
*ZgRA1, ZgCA1, ZgCA2, ZgRA2, ZgRS, ZgCS
820. 0. 115.OE-9 0. 220. 0.

is the equivalent impedance corresponding to a resistor of 220 Ω in series with 820 Ω in parallel with 115 nF:



4.4 Other Input Parameters

Half loop attenuation ZSLI:

ZSLI = V_t /V_r in worst case and with SICOFI filters OFF.

ZSLI is a variable controlling the SICOFI + SLIC Z-filter loop. It should be measured in a worst case condition (for instance Z_g = 1 MΩ). For more information see the chapter about input file in the SICOFI software description.

The other parameters are allready defined in the preceding chapter.

4.5 FORTRAN Source File

Listing of PBL 3762.FOR

```
************************* Siemens A.G.******************************
*
      PROGRAM PBL3762
*
*  Version  V3.0        16 Nov. 88   Mr. GLASSER  HL IT PD 22
*  Revision V3.1        25 Jan. 89
*  Revision V3.2         5 Juni 89
*
*  Revision V3.3        14 Sept. 89  Subroutine IMPED6
*                       Mr. KLIESE   HL IT AT
*
*  PBL 3762 and following
*
********************************************************************
*
        IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
*
        INTEGER      IN,OUT,I,N10,N399,TYPE
        CHARACTER*13 FILEOUT,INFILE
        CHARACTER*1  TEST
*
        REAL  ZtR1,ZtR2,ZtC1,ZtC2,ZtRS,ZtCS
        REAL  ZrR1,ZrR2,ZrC1,ZrC2,ZrRS,ZrCS
        REAL  ZfR1,ZfR2,ZfC1,ZfC2,ZfRS,ZfCS
        REAL  ZpR1,ZpR2,ZpC1,ZpC2,ZpRS,ZpCS
        REAL  ZgR1,ZgR2,ZgC1,ZgC2,ZgRS,ZgCS
        REAL  RIX,CKX,RZT,RZR,CHP,RHP,Cab
        REAL  FREQ,FCHP,FCDC
        REAL  DB,PH,HAHA(2),HAP(2),PI
        REAL  FLP1,PRSG
        REAL  PI2,ZSLI
        REAL  RDC1,RDC2,CDC,R2,R3
*
       COMPLEX K11T(399),K12T(399),K21T(399),K22T(399),KDETT(399)
       COMPLEX K11,K12,K21,K22,KDET
       COMPLEX Zout,ZIN,Zp,ZL,ZT,ZR,ZF,ZG,DEN
       COMPLEX G,LP1,RAX,O,F,Yab,Y,Yp,Yout,HP1,Z1,X
       COMPLEX ZINT(399),ZpT(399),ZLT(399)
       COMPLEX VAR1,Zeq
*
* data storage  for line/source impedance Zg, Zt, Zr, fuse
* impedance Zf, Zp
       COMMON /QZg/ZgR1,ZgR2,ZgC1,ZgC2,ZgRS,ZgCS
       COMMON /QZt/ZtR1,ZtR2,ZtC1,ZtC2,ZtRS,ZtCS
       COMMON /QZr/ZrR1,ZrR2,ZrC1,ZrC2,ZrRS,ZrCS
       COMMON /QZf/ZfR1,ZfR2,ZfC1,ZfC2,ZfRS,ZfCS
       COMMON /QZp/ZpR1,ZpR2,ZpC1,ZpC2,ZpRS,ZpCS
*
       COMMON /QK/K11,K12,K21,K22,KDET
       COMMON /QPI2/ PI2
       COMMON /QP/ PI
```

5 Coefficient Calculation

The execute file PBL 3762.EXE is a compiled version of the file PBL 3762. FOR. It gives an output file named PBL 3762.SLI using the input file PBL 3762.INP. PBL 3762. SLI used in combination with the specification file allows the SICOFI coefficient program to calculate and optimize the SICOFI coefficients.

In order to show the accuracy of the model, we have choosen to calculate using the **measured** values of the components on the test board.

In practice it will be sufficient to calculate for the nominal values, but Z_t and Z_r are sensitive components and have to be precise (1% or better 0.5%).

Several runs have been made with automatic Z- and B-filter calculations.

5.1 Input File

Hereunder is a listing of our input file PBL 3762.INP with the measured values:

```
test (T:test=>amplitude and phase of Kij;  x:normal calculation )
x
*ZfRA1, ZfCA1, ZfCA2, ZfRA2, ZfRS, ZfCS   : impedance Zf
  0.   0.      0       0.    20.2  0.
*ZtRA1, ZtCA1, ZtCA2, ZtRA2, ZtRS, ZtCS   : impedance Zt
598.E+03  0    0      0.     0.    0.
*ZrRA1, ZrCA1, ZrCA2, ZrRA2, ZrRS, ZrCS   : impedance Zr
300.E+03  0    0      0.     0.    0.
CHP : capacitor for internal high pass
10.18E-09
*ZpRA1, ZpCA1, ZpCA2, ZpRA2, ZpRS, ZpCS   : impedance Zp(=Ct=Cr)
0       0      0      0.     0.    2.24E-09
CKX = Decoupling circuit in transmit direction (RAX)
0.98E-06
RIX = Decoupling circuit in transmit direction (RAX)
23.7E+03
RDC1           RDC2           CDC             :  DC path
20.40E+03      20.4E+03       3.33E-06
PRSG = Saturation guard (Yes = 7. no =1.)
1.
*ZSLI = Half loop attenuation
0.5
*Zg : source/line impedance  (with 6 elements)
*ZgRA1, ZgCA1, ZgCA2, ZgRA2, ZgRS, ZgCS
600.   0.   000.E-00   0.    000.  0.
```

```
C*******************************************************************
C      Initialisation part
C*******************************************************************
* internal data given by ERICSSON
        FLP1 = 100.0
        RHP  = 400.E+03
        R2   = 20.
        R3   = 9.98E+03
* other data
        N10  = 10
        OUT  = 6
        IN   = 5
        PI2  = 4.*ASIN(1.)
        PI   = PI2/2.
        FILEOUT = ' '
        INFILE = ' '
*
C*******************************************************************
C      Inputs
C*******************************************************************
*
        WRITE(OUT,'(A)')' Enter input file name :  '
50      READ (IN,'(A)') INFILE
        IF ( INDEX(INFILE,' ').EQ.1  )  THEN
           WRITE (OUT,'(A)')' Enter correct input file name:  '
           INFILE=' '
           GOTO 50
        ENDIF
        WRITE (OUT,'(A)') ' Enter output file name :  '
10      READ (IN,'(A)') FILEOUT
        IF (INDEX(FILEOUT,' ').EQ.1) THEN
            WRITE (OUT,'(A)')' Enter correct output file name :  '
            FILEOUT=' '
            GOTO 10
        ENDIF
        OPEN (30, FILE=FILEOUT, ERR=1000, STATUS= 'UNKNOWN')
*
        WRITE(6,*) ' READING input file...'
*
        OPEN (10, FILE=INFILE, ERR=1100, STATUS= 'OLD')
        READ(10,'(A)')
        READ(10,'(A)') TEST
        READ(10,'(A)')
        READ(10,*) ZfR1,ZfC1,ZfC2,ZfR2,ZfRS,ZfCS
        READ(10,'(A)')
        READ(10,*) ZtR1,ZtC1,ZtC2,ZtR2,ZtRS,ZtCS
        READ(10,'(A)')
        READ(10,*) ZrR1,ZrC1,ZrC2,ZrR2,ZrRS,ZrCS
        READ(10,'(A)')
        READ(10,*) CHP
        READ(10,'(A)')
        READ(10,*) ZpR1,ZpC1,ZpC2,ZpR2,ZpRS,ZpCS
        READ(10,'(A)')
        READ(10,*) CKX
        READ(10,'(A)')
        READ(10,*) RIX
```

```
READ(10,'(A)')
        READ(10,*) RDC1,RDC2,CDC
        READ(10,'(A)')
        READ(10,*) PRSG
        READ(10,'(A)')
        READ(10,*) ZSLI
        READ(10,'(A)')
        READ(10,'(A)')
        READ(10,*) ZgR1,ZgC1,ZgC2,ZgR2,ZgRS,ZgCS
        CLOSE (10)
C*******************************************************************
C      Documentation part
C*******************************************************************
C
        WRITE (30,*) '* ERICSSON SLIC:  ',INFILE

        WRITE (30,*) '* Fuse impedance'
        WRITE (30,*) '*ZfR1= ',ZfR1,'    ZfR2= ',ZfR2
        WRITE (30,*) '*ZfC1= ',ZfC1,'    ZfC2= ',ZfC2
        WRITE (30,*) '*ZfRS= ',ZfRS,'    ZfCS= ',ZfCS

        WRITE (30,*) '* line/generator impedance'
        WRITE (30,*) '*ZgR1= ',ZgR1,'    ZgR2= ',ZgR2
        WRITE (30,*) '*ZgC1= ',ZgC1,'    ZgC2= ',ZgC2
        WRITE (30,*) '*ZgRS= ',ZgRS,'    ZgCS= ',ZgCS

        WRITE (30,*) '* matching impedance'
        WRITE (30,*) '*ZtR1= ',ZtR1,'    ZtR2= ',ZtR2
        WRITE (30,*) '*ZtC1= ',ZtC1,'    ZtC2= ',ZtC2
        WRITE (30,*) '*ZtRS= ',ZtRS,'    ZtCS= ',ZtCS

        WRITE (30,*) '* gain impedance',
        WRITE (30,*) '*ZrR1= ',ZrR1,'    ZrR2= ',ZrR2
        WRITE (30,*) '*ZrC1= ',ZrC1,'    ZrC2= ',ZrC2
        WRITE (30,*) '*ZrRS= ',ZrRS,'    ZrCS= ',ZrCS

        WRITE (30,*) '* parallel impedance at (a,b) line'
        WRITE (30,*) '*ZpR1= ',ZpR1,'    ZpR2= ',ZpR2
        WRITE (30,*) '*ZpC1= ',ZpC1,'    ZpC2= ',ZpC2
        WRITE (30,*) '*ZpRS= ',ZpRS,'    ZpCS= ',ZpCS

        WRITE (30,*) '* other data'
        WRITE (30,*) '* RIX= ',RIX, '    CKX = ',CKX
        WRITE (30,*) '* CHP= ',CHP, '    RHP = ',RHP
        WRITE (30,*) '*RDC1= ',RDC1,'    RDC2= ',RDC2,'    CDC= ',CDC
        WRITE (30,*) '*PRSG= ',PRSG
        FCHP = 1./(CHP*PI2*RHP)
        FCDC  = 1./( CDC*PI2*(RDC1*RDC2)/(RDC1+RDC2) )
        WRITE (30,*) '*FCHP= ',FCHP
        WRITE (30,*) '*FCDC= ',FCDC
* test
       IF (TEST.EQ.'T') then
            WRITE (*,*) '*test: 100 Hz steps and Polar coordinates'
            N10 = 100
        END IF
C
```

```
C*********************************************************************
C      Calculation part
C*********************************************************************

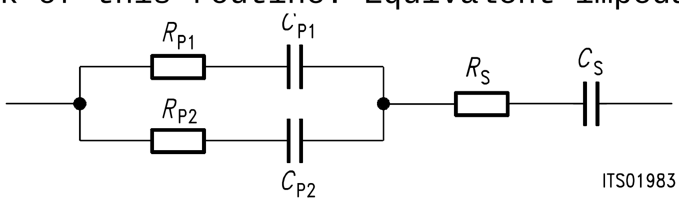
        N399= (4000/N10)-1
*
        WRITE (OUT,*) ' Running preliminary calculations...'
        DO 123,I=1,N399
        FREQ = REAL(I*N10)
        call imped6(ZgR1,ZgR2,ZgC1,ZgC2,ZgRS,ZgCS,FREQ,Zg)
        call imped6(ZfR1,ZfR2,ZfC1,ZfC2,ZfRS,ZfCS,FREQ,Zf)
        call imped6(ZtR1,ZtR2,ZtC1,ZtC2,ZtRS,ZtCS,FREQ,Zt)
        call imped6(ZrR1,ZrR2,ZrC1,ZrC2,ZrRS,ZrCS,FREQ,Zr)
        call imped6(ZpR1,ZpR2,ZpC1,ZpC2,ZpRS,ZpCS,FREQ,Zp)
* Zp is parallel at the output and connected to ground:
* it must be doubled in our grounded model
        Zp = 2.*Zp
* open loop gain
        F  = 10000. / CMPLX(1.,FREQ/FLP1)
* X:
c        IF (TYPE.EQ.3762) THEN
        X  =          1./                                     (
     &       (1./cmplx(1.,-FCHP/FREQ) )
     &     + (ZT*PRSG /( 20.*(RDC1+RDC2)*cmplx(1.,FREQ/FCDC)) ) )
c        ELSE
c        X  =          1./                                     (
c     &       (1./cmplx(1.,-FCHP/FREQ) )
c     &     + (ZT*PRSG /
c     & ( 20.*(RDC1+RDC2)*cmplx(1.,FREQ/FCDC)*cmplx(1.,FREQ/FCHP)) ) )
c        ENDIF
* Yp
        Yp = 1./Zp
* RAX = j*ckx*rix*omega/1.+j*ckx*rix*omega :
* CKX = 0   => no filter
        IF (CKX.le.(1.e-12)) THEN
           RAX = CMPLX(1.,0)
        ELSE
           VAR1 = CMPLX(0,CKX*RIX*PI2*FREQ)
           RAX = VAR1/(1.+ VAR1)
        ENDIF
*
* Zload equivalent: Zeq = Zp//(Zf+Zg)
        Zeq = (Zp*(Zf+Zg))/(Zp+Zg+Zf)
* G
        G   =     ( R2*(1.+F) + F*R3 ) /
     &            ( R2*(1.+F) + Zeq  )
*
* Zout
      Zout =        (   ZT*X*R2*(1.+F)  )   /
     &          ( 2.*F*(R3+R2) + 2.*R2 + ZT*X  )
      Yout = 1./Zout
*
* Zin
        ZIN = Zf + 1./( Yp+Yout )
*
```

```
        K11 = (ZIN-ZG)/(ZIN+ZG)
*
C HP1 = j*2π*freq*CHP*RHP/ 1 + j*2π*freq*CHP*RHP
        HP1 =              1./
     &         CMPLX(1.,(-FCHP/FREQ))
*
*K12 = 2*Gain 2w-4w ( but difference of measuring point)
        K12 = ( -2.*(Zt/Zr)*Zg/(Zg+Zf) ) /
     &        ( (Zt/(2.*G*Zeq)) + (1./(X*RAX))   )
*
*K21 = Gain 4w-2w with divider Zout, Zg, Zp, Zf
        Z1 =   (Zp*Zout)/(Zout + Zp)
        K21 =  RAX*HP1*Z1/( Z1 + Zf+Zg )
*
*K22 = Gain 4w-4w
        K22 =   -(2.*G*RAX*HP1*Zeq/Zr ) /
     &       (  1. + 2.*G*Zeq/(ZT*X*RAX)  )
*
* write the tables
        ZINT(i)=ZIN
        K11T(i)=K11
        K12T(i)=K12
        K21T(i)=K21
        K22T(i)=K22
* intermediate results
        IF (   FREQ.EQ.300.
     &      .or.FREQ.eq.1000.
     &      .or.FREQ.eq.3000.)then
          WRITE (*,*)   '* FREQ:',INT(FREQ)
          WRITE (*,999) '* Zin= ',ZINT(i)
        ENDIF
123     CONTINUE
*
* if test, gives module and phase of Zin as a function of frequency
       IF (TEST.EQ.'T') then
         WRITE (30,*)
     &  '*   freq              |ZIN|           Phi(Zin) '
         DO 189 I=1,N399
               FREQ = REAL(I*N10)
               HAHA(1) = REAL(ZINT(i))
               HAHA(2) = IMAG(ZINT(i))
               CALL CPOL(HAHA,HAP)
               DB= 20.*LOG10(HAP(1)+1.E-20)
               PH= 360.*HAP(2)/PI2
               WRITE (30,*) FREQ,HAP(1),PH
189      CONTINUE
       ENDIF
*
777    FORMAT( A1,F7.1,2(F13.3),A3,2(F13.3) )
888    FORMAT( A1,F6.0,F10.1)
999    FORMAT( A7,G17.9,G17.9)
*
        WRITE (30,'(A)') 'ZSLI'
        WRITE (30,'(G12.5)') ZSLI
        WRITE (OUT,*) ' Running K11 calculation...'
        WRITE (30,'(A)') 'K11-TABLE'
```

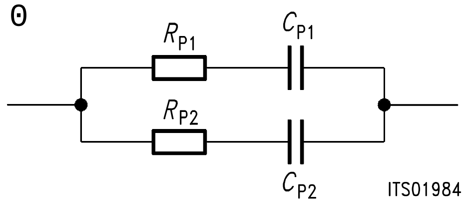
```
      DO 100 I=1,N399
           FREQ = REAL(I*N10)
           HAHA(1)=REAL(K11T(i))
           HAHA(2)=IMAG(K11T(i))
           IF (TEST.EQ.'T') THEN
             CALL CPOL(HAHA,HAP)
             DB= 20.*LOG10(HAP(1)+1.E-20)
             PH= 360.*HAP(2)/PI2
             WRITE (30,*) FREQ,DB,PH
           ELSE
            WRITE (30,*) FREQ,REAL(K11T(I)),IMAG(K11T(i))
           ENDIF
100   CONTINUE
C
      IF (TEST.EQ.'T') THEN
          WRITE (OUT,*) ' Running K12/2. calculation...'
      WRITE (30,'(A)') 'K12/2-TABLE'
      ELSE
          WRITE (OUT,*) ' Running K12 calculation...'
      WRITE (30,'(A)') 'K12-TABLE'
      ENDIF
      DO 110 I=1,N399
           FREQ = REAL(I*N10)
           HAHA(1)=REAL(K12T(i))
           HAHA(2)=IMAG(K12T(i))
           IF (TEST.EQ.'T') THEN
             CALL CPOL(HAHA,HAP)
             DB= 20.*LOG10(HAP(1)+1.E-20)
             PH= 360.*HAP(2)/PI2
c             WRITE (30,*) FREQ,DB,PH
             WRITE (30,*) FREQ,DB-6.,PH
           ELSE
             WRITE (30,*) FREQ,REAL(K12T(I)),IMAG(K12T(i))
           ENDIF
110   CONTINUE
C
      WRITE (OUT,*) ' Running K21 calculation...'
      WRITE (30,'(A)') 'K21-TABLE'
      DO 120 I=1,N399
           FREQ = REAL(I*N10)
           HAHA(1)=REAL(K21T(i))
           HAHA(2)=IMAG(K21T(i))
           IF (TEST.EQ.'T') THEN
             CALL CPOL(HAHA,HAP)
             DB= 20.*LOG10(HAP(1)+1.E-20)
             PH= 360.*HAP(2)/PI2
             WRITE (30,*) FREQ,DB,PH
           ELSE
             WRITE (30,*) FREQ,REAL(K21T(I)),IMAG(K21T(i))
           ENDIF
120   CONTINUE
C
      WRITE (OUT,*) ' Running K22 calculation...'
      WRITE (30,'(A)') 'K22-TABLE'
      DO 130 I=1,N399
           FREQ = REAL(I*N10)
```

```
            HAHA(1)=REAL(K22T(i))
            HAHA(2)=IMAG(K22T(i))
            IF (TEST.EQ.'T') THEN
              CALL CPOL(HAHA,HAP)
              DB= 20.*LOG10(HAP(1)+1.E-20)
              PH= 360.*HAP(2)/PI2
              WRITE (30,*) FREQ,DB,PH
            ELSE
              WRITE (30,*) FREQ,REAL(K22T(I)),IMAG(K22T(i))
            ENDIF
130      CONTINUE
1111     CONTINUE
           WRITE(30,'(A1)') ';'
           CLOSE (30)
         WRITE(OUT,'(A)') ' Data written in file: '//FILEOUT
         STOP
1000     WRITE(OUT,'(A)') ' OPEN ERROR AT OUTPUT-FILE: '//FILEOUT
         STOP 1
1100     WRITE(OUT,'(A)') ' OPEN ERROR AT INPUT-FILE: '//INFILE
           STOP 2
         END
C
C###################################################################
C
      SUBROUTINE CPOL(Z,ZP)
C
C###################################################################
C
C     Name of Subroutine:     CPOL
C
C     Formal parameter list:  Z,ZP
C
C     Input parameters:
C         ZP      (DOUBLE)   ARRAY [2]
C
C     Output parameters:
C         ZP      (DOUBLE)   ARRAY [2]
C
C     Common blocks:
C         P
C
C     Task of this routine:
C         COORDINATE TRANSFORMATION  CARTESIAN --> POLAR
C
C     Required functions:
C         ATAN,SQRT
C
C###################################################################
C
      IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
      REAL  Z(2),ZP(2),PI,E,D
*
      COMMON /QP/ PI
*
      ZP(1) = SQRT(Z(1)*Z(1)+Z(2)*Z(2))
      ZP(2) = ATAN(Z(2)/(Z(1)+1.0E-20))
```

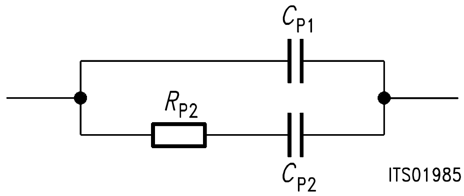
```
      E      = Z(1)
      D      = Z(2)
      IF (E) 1,4,4
1     IF (D) 2,2,3
2     ZP(2) = ZP(2)-PI
      RETURN
3     ZP(2) = ZP(2)+PI
4     RETURN
      END
C
C#################################################################C
C###                                                           ###C
      SUBROUTINE IMPED6(RP1,RP2,CP1,CP2,RS,CS,FREQ,Zeq)
C###                                                           ###C
C###  Note : when a parameter is set to 0 then the             ###C
C###  corresponding resistor or capacitance does not           ###C
C###  exist                                                    ###C
C###                                                           ###C
C###  Formal parameter list:RP1,RP2,CP1,CP2,RS,CS,FREQ,Zeq     ###C
C###                                                           ###C
C###  Input parameters:                                        ###C
C###      RS     [ REAL ]   ; series resistance                ###C
C###      CS     [ REAL ]   ; series capacitance               ###C
C###      RP1    [ REAL ]   ; parallel resistance              ###C
C###      RP2    [ REAL ]   ; parallel resistance              ###C
C###      CP1    [ REAL ]   ; parallel capacitance             ###C
C###      CP2    [ REAL ]   ; parallel capacitance             ###C
C###      FREQ   [ REAL ]   ; frequency                        ###C
C###                                                           ###C
C###  Output parameters:                                       ###C
C###      Zeq     [ COMPLEX ]                                  ###C
C###                                                           ###C
C###  Common blocks:  QPI2                                     ###C
C###                                                           ###C
C###  Task of this routine: Equivalent impedance of:           ###CC
```



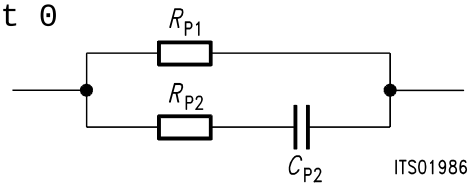

```
C### SPECIAL CASES:                                            ###C
C###          A. SYSTEM Parallel                               ###C
C###             1. CP1 not 0                                  ###C
C###                1.1 rp1 not 0                              ###C
C###                                                           ###C
C###                                                           ###C
C###                                                           ###C
C###                                                           ###C
C###                                                           ###C
C###                                                           ###C
```



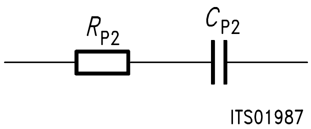

```
C###                1.2 rp1 = 0                                ###C
C###                                                           ###C
C###                                                           ###C
C###                                                           ###C
C###                                                           ###C
C###                                                           ###C
```



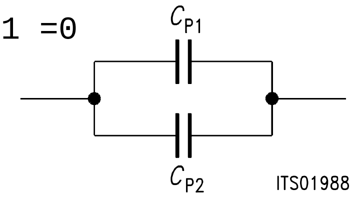
```
C###                  2. CP1 =0                                    ###c
 C###                     2.1 rp1 not 0                              #
```



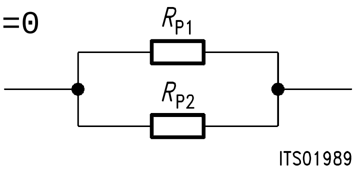

```
 C###                     2.2 rp1 =0                                 #
```



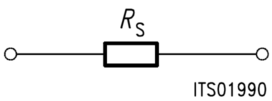

```
 C###                 3. idem  if CP2  = 0                           #
 c###                                                               ###
 c###                 4. RP2 =0 and rp1 =0                           #
```



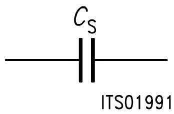

```
 c###                 5.CP2 =0 and CP1 =0                            #
```




```
 C###              B. SYSTEM Series                                  #
 C###                 1. CS = 0                                      #
```




```
 C###                 1. RS = 0                                      #
 C###                 idem  system A                                 #
```




```
 C###              C.Conclusion: Zeq = sum of the two                #
 C###                            systems in any case                ###
c###                                                               ###c
c#################################################################c
C
      IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
      REAL CP1,CP2,RP1,RP2
      REAL CS,RS,N,UL
      REAL FREQ,PI2,OMEGA
      COMPLEX D,C,Zeq,ZA,ZB
*
      COMMON /QPI2/ PI2
*
      OMEGA = PI2*FREQ
      IF (CP1.EQ.0) THEN
         C=CMPLX(RP1,0.)
      ELSE
         C = RP1 + (1. / CMPLX(0.,OMEGA*CP1))
      ENDIF
      IF (CP2.EQ.0) THEN
         D=CMPLX(RP2,0.)
      ELSE
         D = RP2 + (1. / CMPLX(0.,OMEGA*CP2))
```

```
      ENDIF
      N  = CABS(C)
      UL = CABS(D)
* if one of them is 0 then no parallel calculation
      IF ((N.EQ.0.).OR.(UL.EQ.0.)) then
           ZA=C+D
      ELSE
*  ZA = C & D in parallel
           ZA=C*D/(C+D)
      ENDIF
C System series
      IF (CS .EQ.0) THEN
         ZB=CMPLX(RS,0.)
      ELSE
         ZB = RS +( 1. / CMPLX(0.,OMEGA*CS))
      ENDIF
c both
       Zeq=ZA+ZB
       RETURN
       END
C
c##############################################################c
```

5.2 Specification File

The SPEC file for 600 Ω specifications BUSA.SPE is following:
(Please notice: * A-Law and not μ-Law has been used
* The limit values of the trans-hybrid loss in DD spec have been set artificially higher than required so that the SICOFI program calculates coefficients which will give some margin between the required and the measured trans-hybrid loss)

BUSA.SPE

```
FREF = 1004.0    LAW = A
UREF = 0.7750    RLX = 0.    RLR =    0.0
ABIMP  = ZI
 ZLRP1=   0.      ZLCP1= 0.      ZLRP2= 0.      ZLCP2= 0.E-0
 ZLRS = 600.      ZLCS = 0.
 ZIRP1=   0.      ZICP1= 0.      ZIRP2= 0.      ZICP2= 0.E-0
 ZIRS = 600.      ZICS = 0.
 Z3RP1=   0.      Z3CP1= 0.      Z3RP2= 0.      Z3CP2= 0.E-0
 Z3RS = 600.      Z3CS = 0.
 ZRRP1=   0.      ZRCP1= 0.      ZRRP2= 0.      ZRCP2= 0.E-0
 ZRRS = 600.      ZRCS = 0.

ZIN
FR            300        500       1k      3.4k
AT-           0          26        30       30
AT+          20         26        30          0

ZMIR
FR             4k        12k
AT-           30         3
AT+           30         3

DA,UPPER
FR          300    500    2.7k     3k      3.4k
AT-        100    .75    .25       .35       .75
AT+         .75    .25    .35       .75     100

DA,LOWER
FR          300         3.4k
AT-         0           -.25
AT+         -.25         0

DA,DELAY
FR            500        600       1k       2.6k    2.8k
GD-          10k       .420      .150      .085      .150
GD+          .420        .150       .085       .150    10k
```

```
AD,UPPER
FR          300    500    2.7k      3k       3.41k
AT-        100    .75    .25        .35        .75
AT+         .75    .25    .35        .75      100

AD,LOWER
FR          300          3.39k
AT-        0             -.25
AT+         -.25          0

AD,DELAY
FR            500          600        1k          2.6k     2.8k
GD-          10k        .420        .150        .085        .150
GD+          .420          .150         .085         .150     10k
DD
FR            300          500        2.5k       3.4k
AT-        0           27            27          23
AT+          23            27            27        0
```

6 Measurement Results

The outputs of the SICOFI program are:

A **byte file** (PBL 3762.BYT) to be transferred to the SICOFI evaluation board. A **result file** (PBL 3762.RES) with all the coefficients, some comments about the SLIC (beginning with "*") and the calculated transfer functions.

The measurements on the following pages correspond well with the calculated values and the specifications are fulfilled.

Byte file: PBL 3762.BYT

```
PSR=36
CAM00=41
CAM20=40
CIW0=26,F4,80
CIW0=13,30,22,2A,6B,2B,22,B3,22
CIW0=23,F0,BC,37,72,49,36,0F,A6
CIW0=2B,F0,2B,97,74,2A,27,02,CE
CIW0=03,35,12,52,91,BE,F9,A9,F4
CIW0=0B,00,33,AB,23,32,73,39,FA
CIW0=18,19,19,11,19
CIW0=30,61,B1,00,B4
SIG0=80
CIW0=26,F4,78
```

Result file: PBL 3762.RES

```
Input_file_name: PBL 3762.CTL            Date: 08.12.88  11:16
SPEC = BUSA.SPE                             SLIC = PBL 3762.SLI
BYTE = REF.BYT      CHNR = 0,A
PLQ  = N
ON = ALL                     VERSION = V3.1          SHORT = N
OPT =  Z+X+R+B               ZXRB =  NNNN            REL = Y

ZAUTO = Y
        PZIN= 11        PSP =  3
FZ =     300.00       500.00       1000.0       1300.0       1500.0
         2000.0       2500.0       2900.0       3000.0       3200.0
         3400.0       7000.0       10000.       14000.

WFZ =    .100         1.00         2.00         1.50         1.00
         3.00         1.00         1.00         1.00         3.00
         2.80         .230         1.00         1.00
   FZ =  300.00       3400.0        ZLIM = 10.00

ZREP  =Y                           ZDIS  =  1
  FR =   200.00       3400.0

RDISP=  N             RREFQ = N       RREF =  .29230E-01
```

```
  FX =   300.00       3400.0
XDISP=  N             XREFQ = N       XREF = -.21669
BAUTO = Y
        PB  = 10        GWFB=  .500E-01 BDF =  1
FB =     300.00       500.00       700.0        1000.0       1500.0
         2100.0       2300.0       2900.0       3200.0       3300.0
WFB =    4.0000       2.0000       1.0000       5.0000       1.0000
         2.0000       1.0000       5.0000       1.0000       1.0000
  FB =   300.00       3400.0        BLIM = 10.00 BDF =  1
BREP = Y                           BDIS  =  1
AREC =   .00     DREC =   .00     AXMI =   .00     DXMI =   .00

XZQ =  -.16406250E+00   .32031250E+00   .13183590E-01
       -.30468750E+00   .16406250E+00
XRQ =   .98535160E+00   .10253910E-01   .53710940E-02
        .36621090E-02  -.65917970E-02
XXQ =   .10117190E+01   .17562870E-01   .36621090E-02
        .90332030E-02  -.73852540E-02
XBQ =  -.26550290E+00  -.49804690E+00  -.49316410E+00
        .26171880E+00   .17187500E+00
       -.24798580E+00   .34179690E-02   .28515630E+00
       -.28906250E+00   .13867190E+00
XGQ =   .51123050E+00   .20546880E+01
;

Bytes for Z-Filter (13):            30,22,2A,6B,2B,22,B3,22
Bytes for R-Filter (2B):            F0,2B,97,74,2A,27,02,CE
Bytes for X-Filter (23):            F0,BC,37,72,49,36,0F,A6
Bytes for Gain-factors (30):        61,B1,00,B4
2nd part of bytes B-Filter (0B):    00,33,AB,23,32,73,39,FA
1st part of bytes B-Filter (03):    35,12,52,91,BE,F9,A9,F4
Bytes for B-Filter delay (18):      19,19,11,19

 * ERICSSON SLIC ERIC.INP

 * TEST= x

 * Fuse impedance
 *ZfR1=    0.000000E+00    ZfR2=    0.000000E+00
 *ZfC1=    0.000000E+00    ZfC2=    0.000000E+00
 *ZfRS=       20.200000    ZfCS=    0.000000E+00

 * line/generator impedance
 *ZgR1=      600.000000    ZgR2=    0.000000E+00
 *ZgC1=    0.000000E+00    ZgC2=    0.000000E+00
 *ZgRS=    0.000000E+00    ZgCS=    0.000000E+00

 * matching impedance
 *ZtR1=   598000.000000    ZtR2=    0.000000E+00
 *ZtC1=    0.000000E+00    ZtC2=    0.000000E+00
 *ZtRS=    0.000000E+00    ZtCS=    0.000000E+00
 * gain impedance
```

```
*ZrR1=   300000.000000    ZrR2=    0.000000E+00
*ZrC1=    0.000000E+00    ZrC2=    0.000000E+00
*ZrRS=    0.000000E+00    ZrCS=    0.000000E+00

* parallel impedance at (a,b) line
*ZbR1=    0.000000E+00    ZbR2=    0.000000E+00
*ZbC1=    0.000000E+00    ZbC2=    0.000000E+00
*ZbRS=    0.000000E+00    ZbCS=    2.240000E-09

* other data
* RIX=    23700.000000    CKX =    9.800000E-07
* CHP=    1.018000E-08    RHP =   400000.000000
*RDC1=    20400.000000    RDC2=    20400.000000    CDC=    3.330000E-06
*PRSG=        1.000000
*FCHP=       39.085200
*FCDC=        4.685713

RUN #     1

Z-FILTER calculation results
  Reference impedance for optimization:

ZIRP1=      0. ZICP1=  .000     ZIRP2=      0. ZICP2=  .000
ZIRS =    600. ZICS =  .000

  Calculated and quantized coefficients:

XZ  =    -.16279    .31968    .01322   -.30409    .16758
XZQ =    -.16406    .32031    .01318   -.30469    .16406
Bytes for Z-Filter (13):    30,22,2A,6B,2B,22,B3,22

RETURN LOSS
 FREQ        loss                        FREQ        loss
 (Hz)        (dB)                         (Hz)        (dB)
  100.      15.460                       1800.      36.898
  200.      21.477                       1900.      36.337
  300.      25.144                       2000.      35.902
  400.      27.876                       2100.      35.599
  500.      30.134                       2200.      35.433
  600.      32.130                       2300.      35.412
  700.      33.973                       2400.      35.549
  800.      35.716                       2500.      35.860
  900.      37.354                       2600.      36.372
 1000.      38.807                       2700.      37.117
 1100.      39.912                       2800.      38.134
 1200.      40.477                       2900.      39.435
 1300.      40.434                       3000.      40.878
 1400.      39.920                       3100.      41.813
 1500.      39.164                       3200.      41.100
 1600.      38.347                       3300.      38.833
 1700.      37.575                       3400.      36.154
Min. Z-loop reserve:      5.315 dB
```

```
      at frequency:     8500.0 Hz
Min. Z-loop mirror signal reserve:      9.927 dB
                     at frequency:     9000.0 Hz

Run #    1

X-FILTER calculation results

  Reference impedance for optimization:
ZIRP1=      0. ZICP1=  .000     ZIRP2=      0. ZICP2=  .000
ZIRS =    600. ZICS =  .000

  Calculated and quantized coefficients:

XX  =    1.01241    .01756    .00367    .00912   -.00740
XXQ =    1.01172    .01756    .00366    .00903   -.00739
Bytes for X-Filter (23):    F0,BC,37,72,49,36,0F,A6

GX results:
All attenuation values (in dB) refer to FREF =    1004. Hz
    RLX    SLIC+Z    VREF/VSICOFI    XREF          GX
    .00 -    .29  -      6.17    -   -.22    =     -6.25  ideal
   -.01 =    .29  +      6.17    +   -.22    +     -6.25  quant
Second byte for Gain:      ,00,B4
Calculation of transmit transfer function (AD)
All attenuation values (in dB) refer to FREF =     1004.0 Hz

TGREF CA =    .278 ms      TGREF CB =    .291 ms
```

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
100.	14.017	2.890	2000.	.063	.010
200.	.419	1.880	2100.	.053	.016
300.	.061	.629	2200.	.041	.022
400.	.069	.309	2300.	.027	.030
500.	.055	.179	2400.	.015	.039
600.	.036	.112	2500.	.005	.049
700.	.020	.073	2600.	.000	.060
800.	.008	.049	2700.	.003	.073
900.	.001	.032	2800.	.015	.088
1000.	-.001	.021	2900.	.038	.105
1100.	.003	.013	3000.	.074	.126
1200.	.010	.008	3100.	.124	.151
1300.	.021	.004	3200.	.192	.182
1400.	.033	.001	3300.	.283	.223
1500.	.045	.000	3400.	.410	.277
1600.	.056	.000	3500.	.596	.355
1700.	.065	.001	3600.	.906	.473
1800.	.069	.003	3700.	1.507	.666
1900.	.068	.006	3800.	2.952	1.001

```
Run #    1

R-FILTER calculation results

  Reference impedance for optimization:
ZIRP1=      0. ZICP1=  .000     ZIRP2=      0. ZICP2=  .000
ZIRS =    600. ZICS =  .000

  Calculated and quantized coefficients:

XR  =     .98529    .01014    .00518    .00364   -.00655
XRQ =     .98535    .01025    .00537    .00366   -.00659
Bytes for R-Filter (2B):    F0,2B,97,74,2A,27,02,CE

GR results:
All attenuation values (in dB) refer to FREF=    1004. Hz

   -RLR    SLIC+Z    VSICOFI/VREF    RREF          GR
    .00 -     .31  -     -6.17    -    .03    =      5.83  ideal
    .00 =     .31  +     -6.17    +    .03    +      5.83  quant

First byte for Gain (30):      61,B1
Calculation of receive transfer function (DA)
All attenuation values (in dB) refer to FREF =     1004.0 Hz


TGREF CA =    .059 ms      TGREF CB =    .042 ms
```

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
100.	-.319	.000	2000.	.060	.210
200.	-.003	.113	2100.	.055	.216
300.	.049	.143	2200.	.046	.224
400.	.057	.155	2300.	.035	.232
500.	.050	.162	2400.	.023	.242
600.	.038	.167	2500.	.012	.252
700.	.025	.170	2600.	.004	.264
800.	.014	.173	2700.	.001	.278
900.	.005	.176	2800.	.004	.293
1000.	-.000	.179	2900.	.016	.311
1100.	-.001	.181	3000.	.039	.333
1200.	.002	.183	3100.	.074	.358
1300.	.010	.185	3200.	.125	.391
1400.	.020	.188	3300.	.200	.432
1500.	.031	.190	3400.	.309	.488
1600.	.042	.193	3500.	.480	.566
1700.	.052	.196	3600.	.775	.685
1800.	.058	.200	3700.	1.365	.879
1900.	.061	.205	3800.	2.803	1.214

```
Run #    1

B-FILTER calculation results

  Reference impedance for optimization:
ZLRP1=      0. ZLCP1=  .000     ZLRP2=      0. ZLCP2=  .000
ZLRS =    600. ZLCS =  .000

  Calculated and quantized coefficients:
XB  =    -.26544   -.49818   -.49274    .26327   -.17247
         -.24799    .00340    .28698   -.28981    .13867
XBQ =    -.26550   -.49805   -.49316    .26172    .17188
         -.24799    .00342    .28516   -.28906    .13867
2nd part of bytes B-Filter (0B):    00,33,AB,23,32,73,39,FA
1st part of bytes B-Filter (03):    35,12,52,91,BE,F9,A9,F4

TRANS HYBRID LOSS

  FREQ        loss                         FREQ        loss
  (Hz)        (dB)                          (Hz)        (dB)
   100.      24.567                        1800.      32.593
   200.      18.341                        1900.      30.544
   300.      24.229                        2000.      29.354
   400.      32.242                        2100.      28.809
   500.      49.612                        2200.      28.837
   600.      35.027                        2300.      29.452
   700.      30.733                        2400.      30.751
   800.      28.902                        2500.      32.940
   900.      28.233                        2600.      36.340
  1000.      28.362                        2700.      40.076
  1100.      29.199                        2800.      38.391
  1200.      30.816                        2900.      34.673
  1300.      33.513                        3000.      32.338
  1400.      38.230                        3100.      31.366
  1500.      50.024                        3200.      31.773
  1600.      43.144                        3300.      34.032
  1700.      36.075                        3400.      38.314

Additonal  B-filter delay (in seconds):   .625E-04
Bytes for B-filter delay (18):   19,19,11,19
```

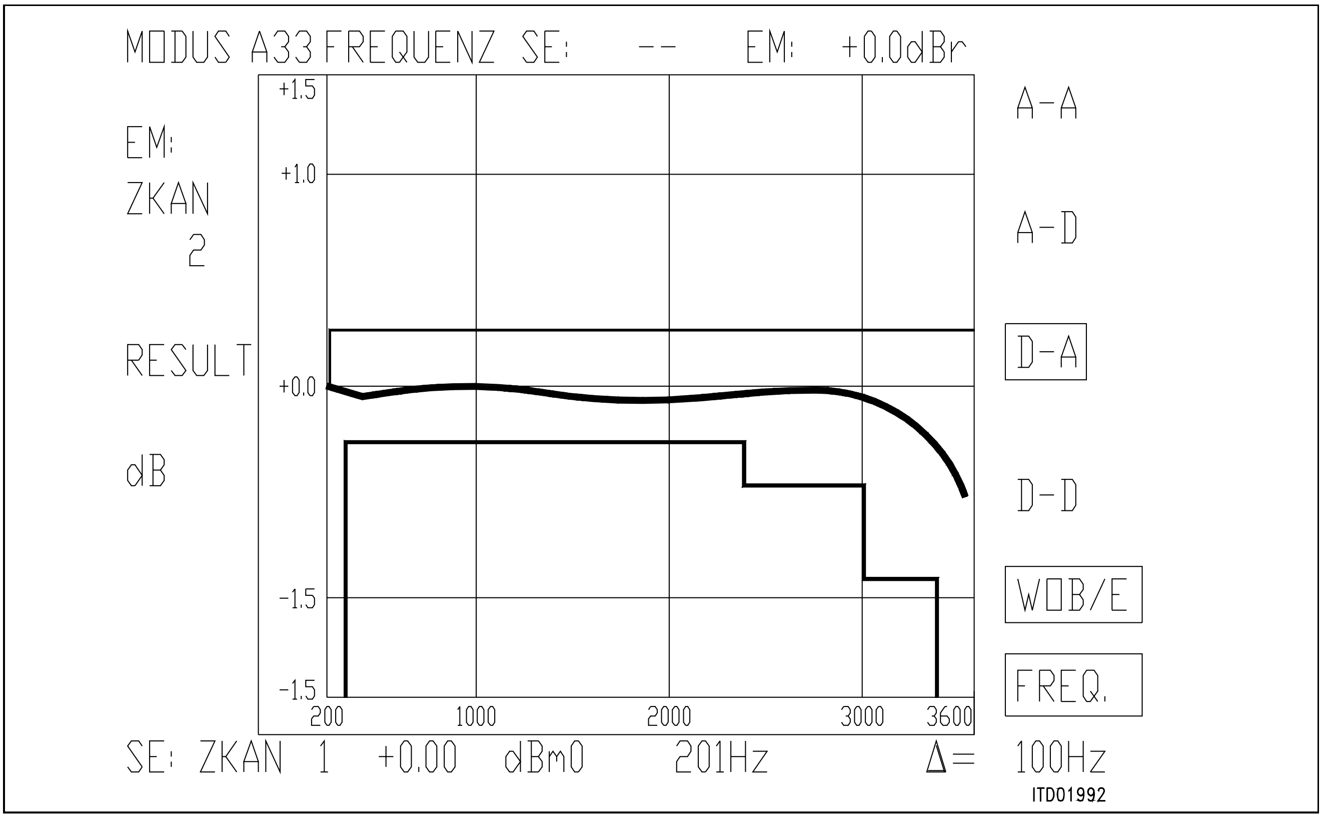


Figure 9

FREQ/Hz	RES/dBm0	FREQ/Hz	RES/dBm0
201	-0.09	2208	-0.15
301	-0.13	2309	-0.14
402	-0.16	2409	-0.13
502	-0.15	2509	-0.12
602	-0.13	2610	-0.12
703	-0.12	2710	-0.12
803	-0.11	2811	-0.12
903	-0.10	2911	-0.13
1004	-0.10	3011	-0.16
1104	-0.10	3112	-0.19
1205	-0.11	3212	-0.24
1305	-0.11	3312	-0.31
1405	-0.12	3413	-0.43
1506	-0.14	3513	-0.61
1606	-0.15		
1706	-0.15		
1807	-0.16		
1907	-0.16		
2008	-0.16		
2108	-0.16		

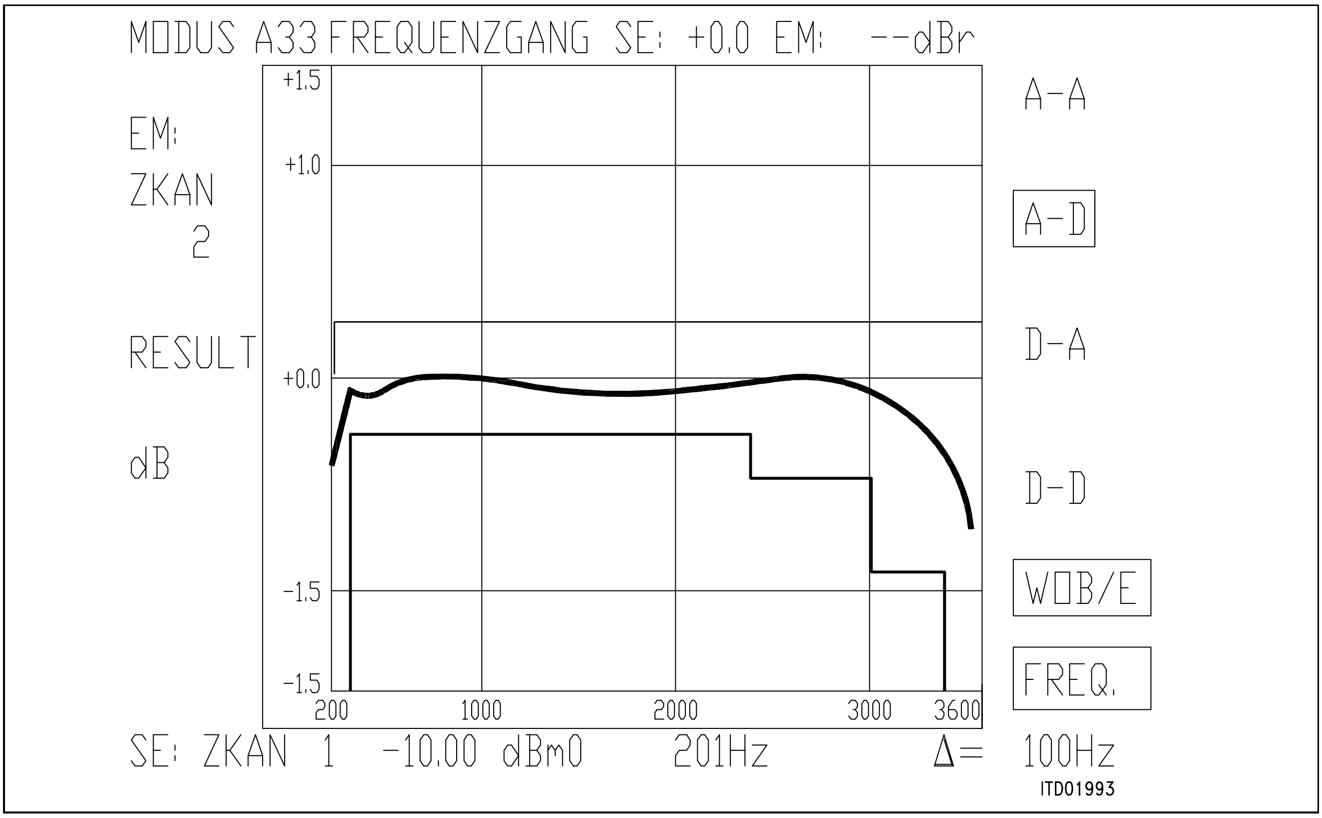


Figure 10

FREQ/Hz	RES/dBm0	1	FREQ/Hz	RES/dBm0
201	-0.68		2208	-0.29
301	-0.30		2309	-0.28
402	-0.32		2409	-0.26
502	-0.30		2509	-0.25
602	-0.28		2610	-0.24
703	-0.27		2710	-0.25
803	-0.26		2811	-0.27
903	-0.25		2911	-0.28
1004	-0.26		3011	-0.32
1104	-0.27		3112	-0.37
1205	-0.28		3212	-0.44
1305	-0.28		3312	-0.58
1405	-0.30		3413	-0.69
1506	-0.31		3513	-0.89
1606	-0.32			
1706	-0.33			
1807	-0.32			
1907	-0.32			
2008	-0.32			
2108	-0.30			

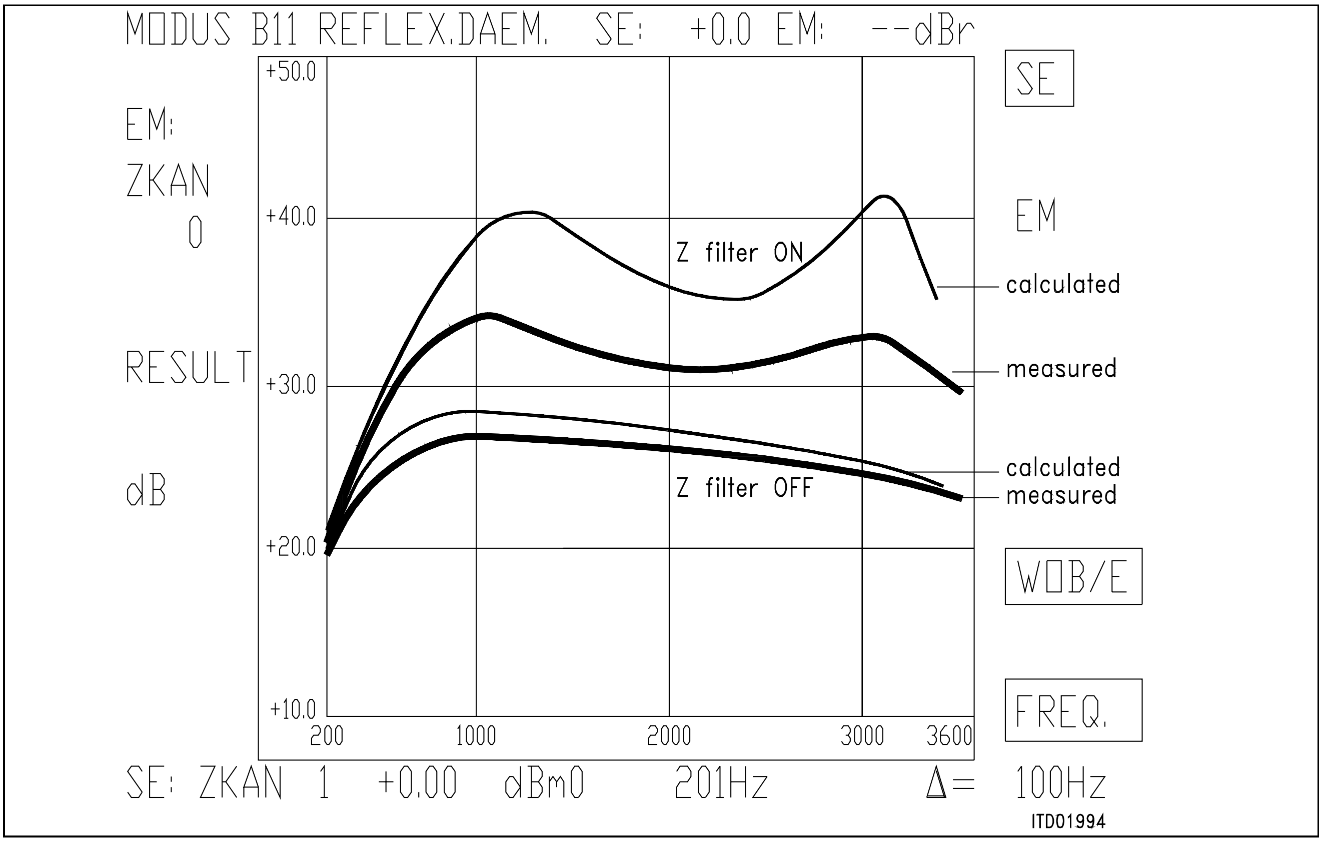


Figure 11

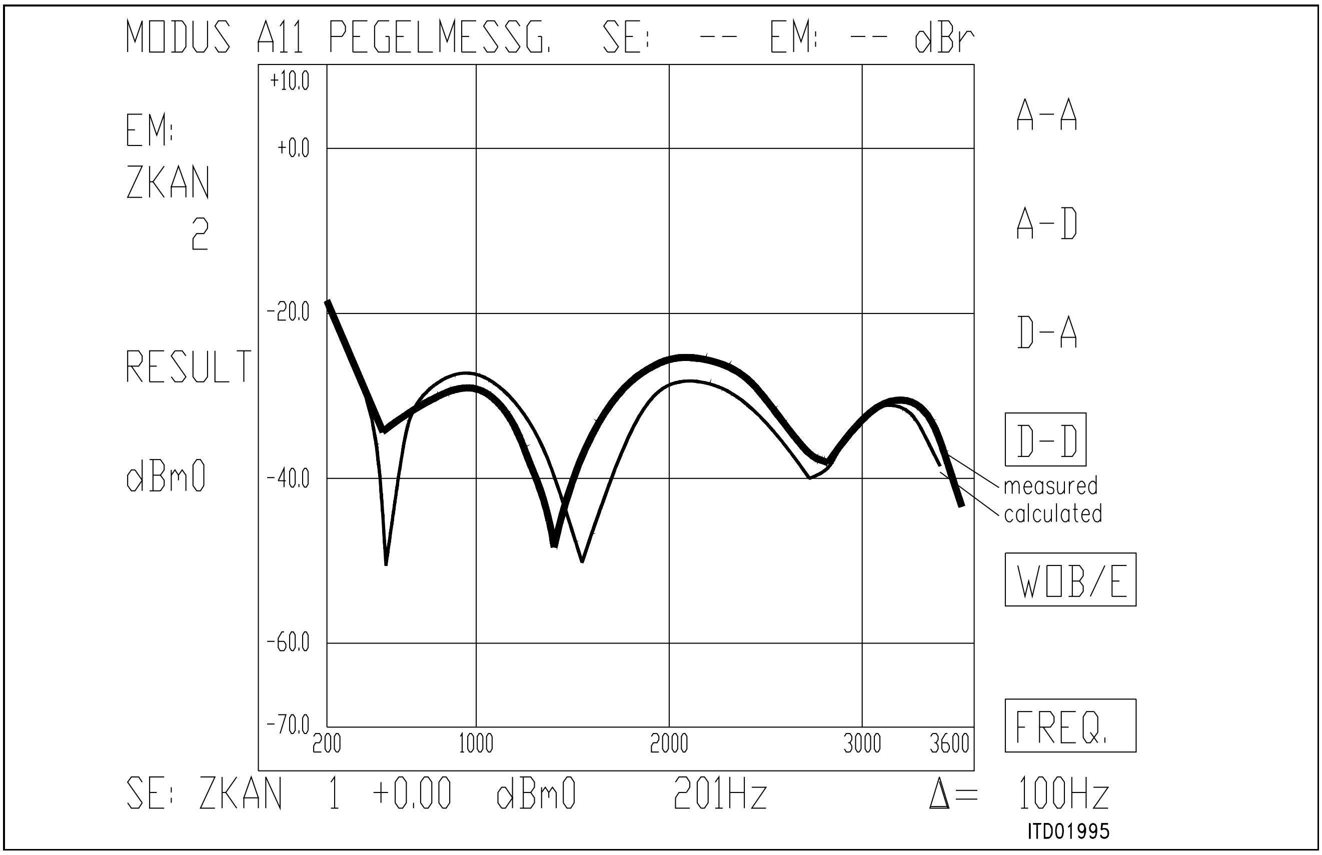


Figure 12

7 Correlation

The same circuit has been tested for correlation between calculated and measured values with and without fuse resistors and with other specifications. We obtained a good correlation between measured results and calculated results.

BRD spec and fuse resistor (Z_f = 20 Ω)
results: BF3.BYT

```
PSR=36
CAM00=41
CAM20=40
CIW0=26,F4,80
CIW0=13,C0,C1,C2,7B,19,2A,D1,2F
CIW0=23,70,CB,97,51,CA,5D,01,45
CIW0=2B,70,D3,AD,4B,25,3A,1D,12
CIW0=03,21,BA,7D,8B,54,4A,AC,B2
CIW0=0B,00,B2,91,CA,12,EC,4B,B9
CIW0=18,19,19,11,19
CIW0=30,A0,CF,10,B2
SIG0=80
CIW0=26,F4,78
```

The circuit as it is fulfills the requirement for Germany of – 7 dB relative level in receive direction only with the version 4 and later of SICOFI (6 dB attenuation are necessary).

USA spec and **no** fuse resistor:
Results: PBL 3762.byt

```
PSR=36
CAM00=41
CAM20=40
CIW0=26,F4,80
CIW0=13,40,BC,FB,6C,12,33,CB,13
CIW0=23,70,29,77,75,19,26,07,36
CIW0=2B,F0,29,8F,7D,E8,E6,01,CE
CIW0=03,32,B1,13,90,2F,E9,A3,B6
CIW0=0B,00,33,AF,63,42,71,B8,EA
CIW0=18,19,19,11,19
CIW0=30,71,C8,00,26
SIG0=80
CIW0=26,F4,78
```

BRD.SPE with Fuse Resistor: BF3.BYT

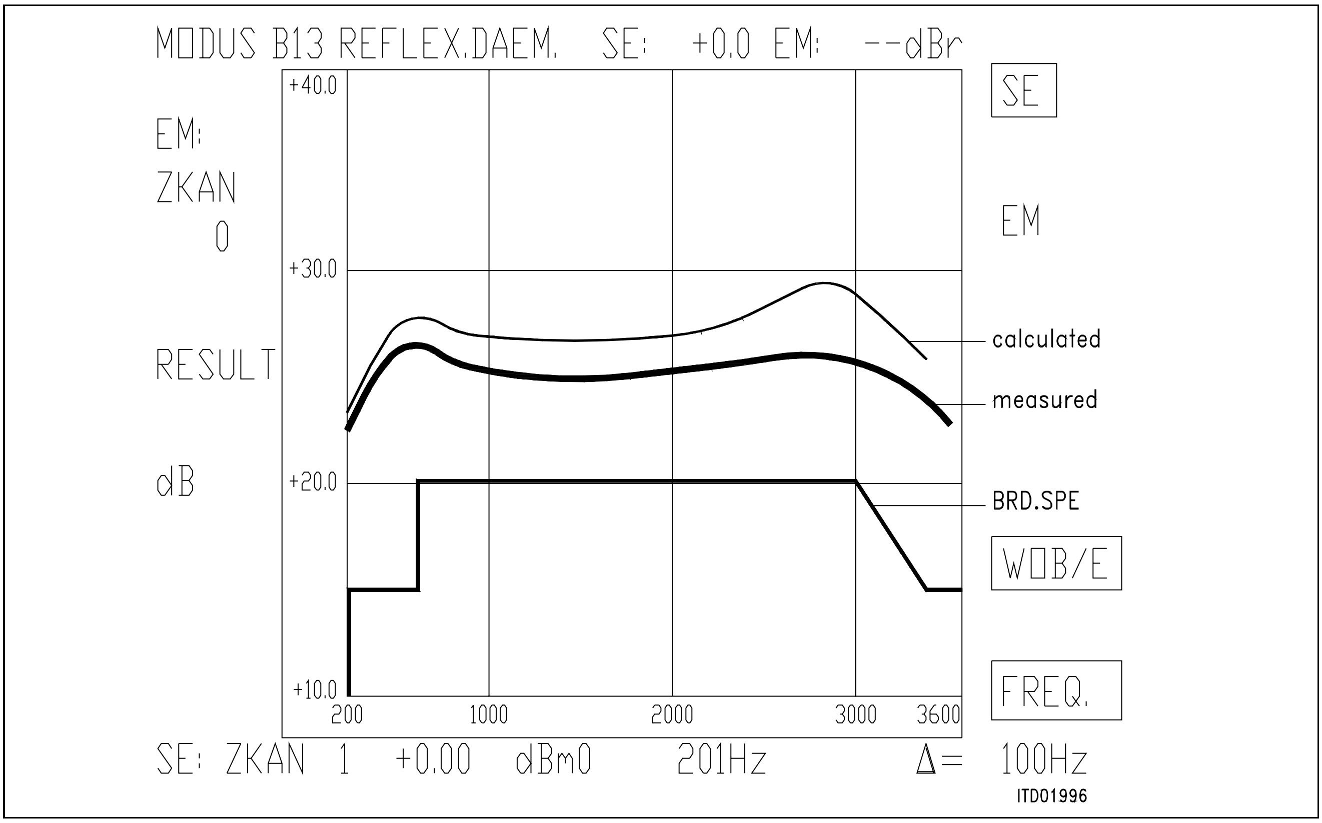


Figure 13

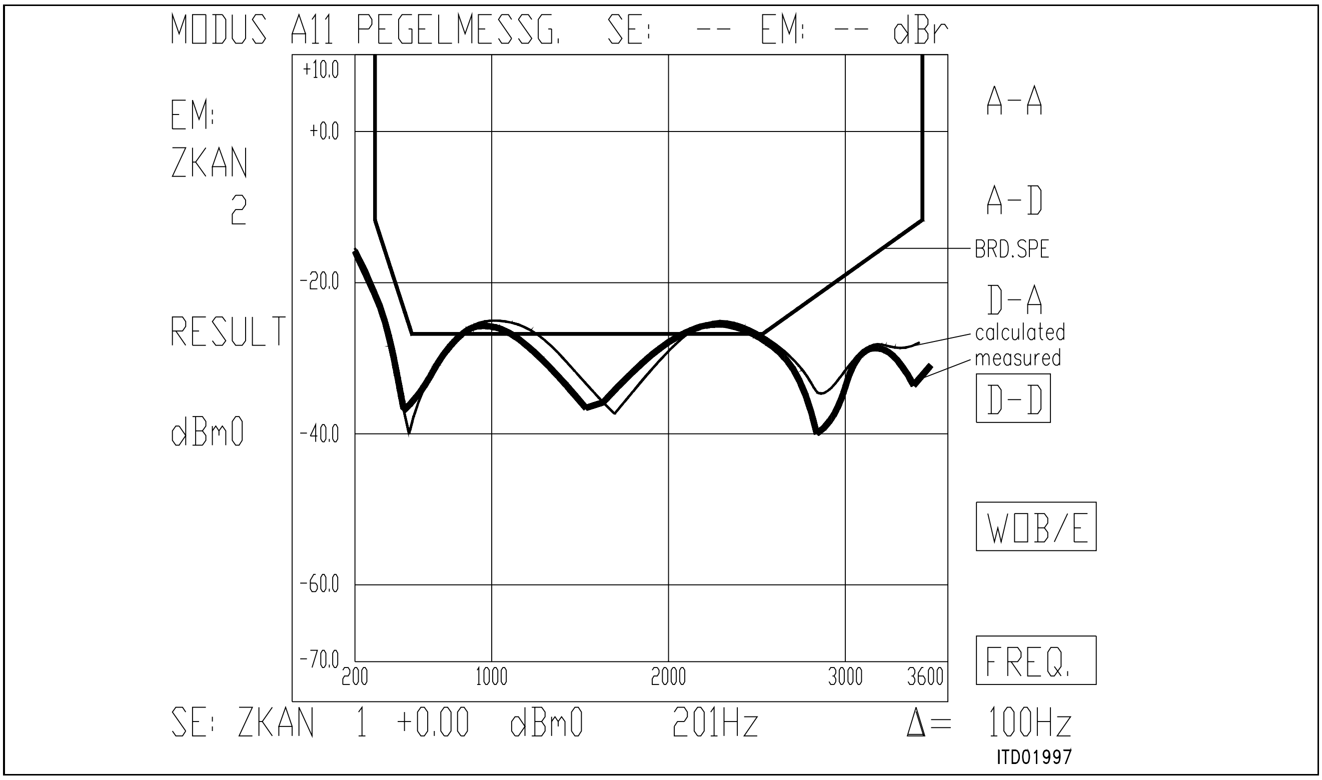


Figure 14

USA.SPE without Fuse Resistor: PBL 3762.BYT

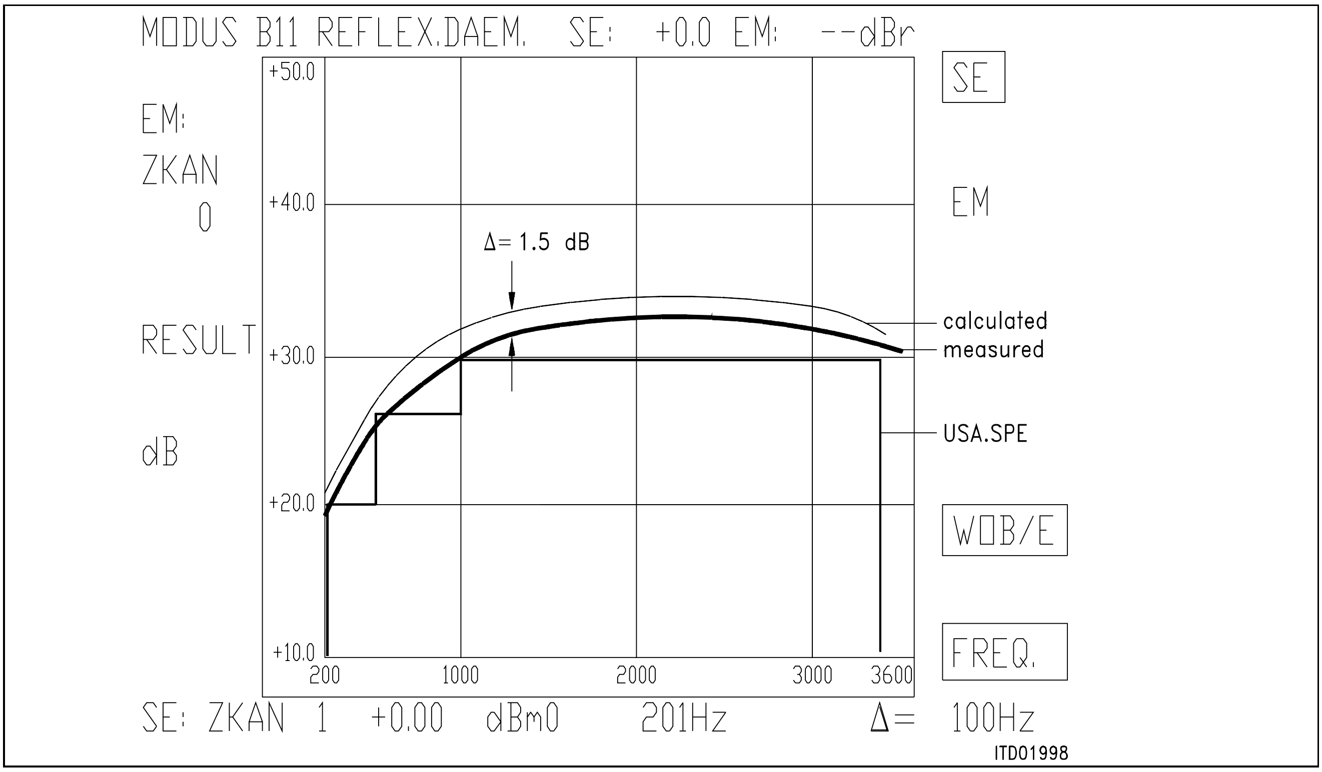


Figure 15

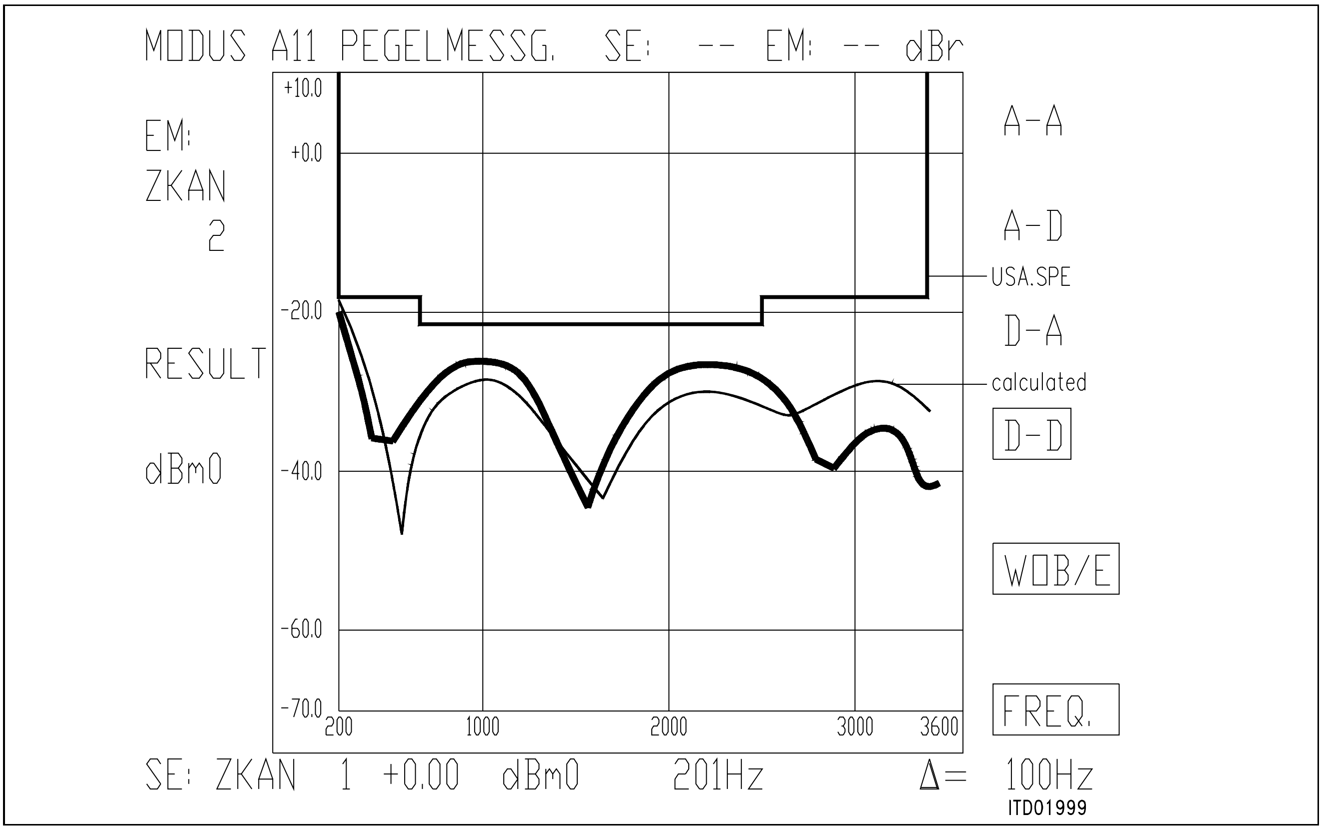


Figure 16

SICOFI® Application Together with ST SLIC L3000/L3030

Contents **Page**

1 Introduction

Due to the various existing technical realizations of the Subscriber Line Interface (SLIC) it is necessary to write a dedicated ’SLIC Program’ for each SLIC type when calculating the SLIC parameters and simulating its transfer characteristics using e.g. the STS 2060 SICOFI Coefficients Program. This ’SLIC Program’ generates an input file for the SICOFI Coefficients Program which in turn calculates the coefficients required for programming the SICOFI PEB 2060 or SICOFI-2 PEB 2260.

This application note refers to the SGS-Thomson SLIC L3030. Besides of some information about operating the SLIC and the SICOFI software, it contains the SLIC program written in FORTRAN. In the appendix the calculated and measured transfer functions according to specifications of the ’Deutsche Bundespost’ are compared.

A SLIC-Babyboard answering these specifications has been designed by the HL IT Application Group of Siemens and is available under the name of STUS 3030. This board is compatible to our SICOFI-Testboard STUT 2060 and SICOFI-2-Board SIPB 5135.

2 Software Principle

The main functions of a Subscriber Line Interface Circuit (SLIC) are to provide the BORSHT functions (Battery feeding, Overvoltage protection, Ringing, Signaling, Hybrid function, Testing). In the case of a SLIC being used in combination with the SICOFI, the hybrid function is splitted into the two-wire to four-wire junction realized by the SLIC, and the impedance matching, hybrid balancing and gain adjustment provided by the internal filters of the SICOFI (**see figure 1**).

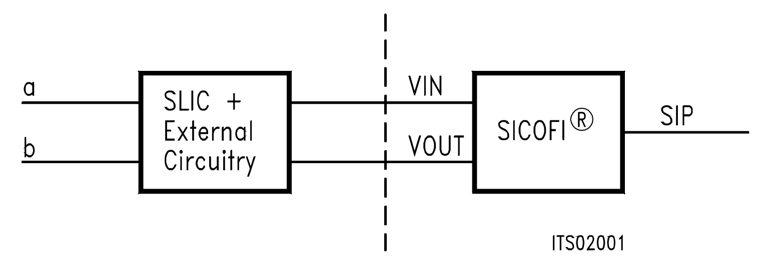


Figure 1

SLIC-SICOFI® Hardware

In a similar way, the software consists of two major sections: The SLIC description file (.SLI file) and the SICOFI program.

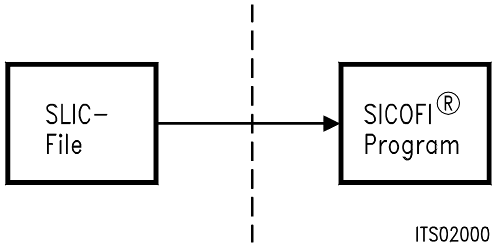


Figure 2

SLIC-SICOFI® Software

The other functions (such as off-hook detection, testing, standby mode, ringing) may also affect the speech signal, but will not be considered in the SLIC example described below.

2.1 SICOFI® Software

For modelling the SLIC, the complete SICOFI software structure is shown in detail in **figure 3**:

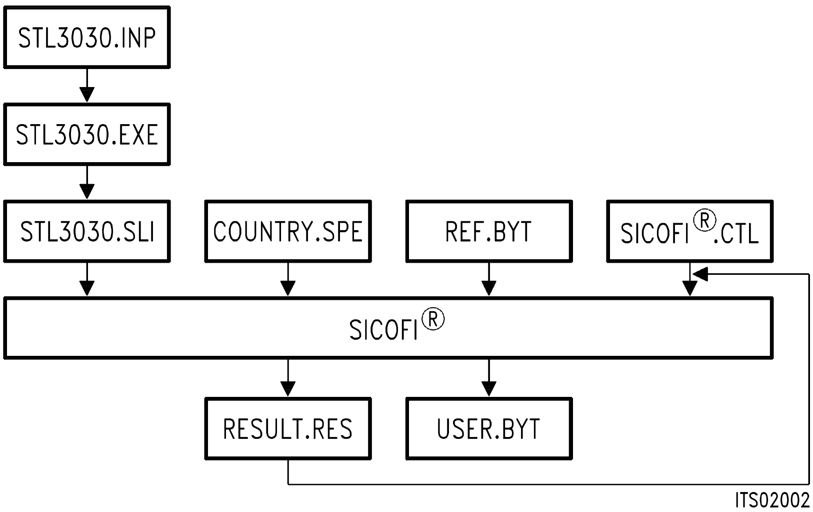


Figure 3

Details of Software Structure

ST L3030.INP

The input file ST L3030.INP contains all data of the external circuitry and, in addition, the worst case loop attenuation at the four-wire SLIC side. Representation of numerical values is left to the user.

ST L3030.EXE

Using the input file ST L3030.INP, the SLIC program ST L3030.EXE calculates the transfer functions of the SLIC. It is written in FORTRAN.

ST L3030.SLI

ST L3030.SLI is the output file of the SLIC program ST L3030.EXE. In the main part it contains a table of the M-parameters of the SLIC calculated in dependence of frequency. At the top of the file the external components and the worst case loop attenuation are included.

Auxiliary Files:

COUNTRY.SPE:

COUNTRY.SPE is an input file to the SICOFI program describing the particular customer specifications (CCITT etc ...) and measurement configuration parameters (e.g. termination impedance).

REF.BYT

REF.BYT is another input file to the SICOFI program defining a frame into which the SICOFI program can write the newly calculated coefficients together with some predefined commands (required for sending the SICOFI coefficients from the Peripheral Board Controller PBC (PEB 2050) to the SICOFI and to store them in a USER.BYT file).

SICOFI.CTL

SICOFI.CTL is the control file of the SICOFI program. It contains the data controlling the optimization and simulation processes.

The SICOFI program SICOFI.BAT generates the SICOFI coefficients and simulates the theoretical transfer functions of the set SLIC + SICOFI.

RESULT.RES

RESULT.RES is the output file of the SICOFI program. It contains the coefficients for programming the SICOFI and a list of the calculated transfer characteristics of the set SLIC + SICOFI such as return loss, frequency response, echo return loss, etc ...

2.2 SLIC Software

According to its functionality the SLIC operates as a three-port. To describe its electrical properties five parameters are used in the SICOFI program: The four Mixed-Matrix-parameters (M-parameters) and the attenuation of the loop Z-filter/SLIC (ZSLI-value).

2.2.1 M - Parameter

The SLIC and its external circuitry may be represented as a three-port (**c.f. figure 4**).

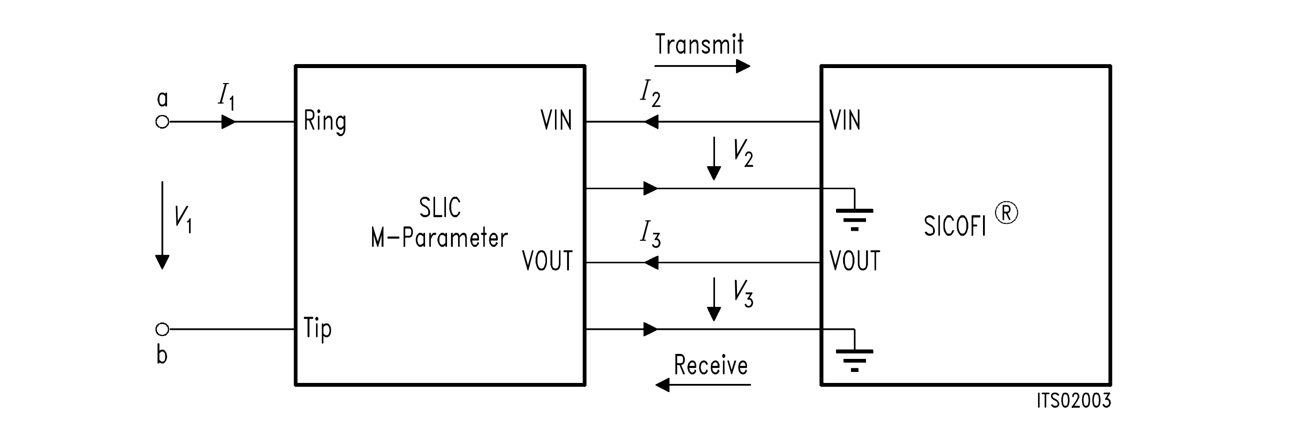


Figure 4

SLIC and its External Circuitry as a Three Port

I_1, I_2 and I_3 are port currents and V_1, V_2 and V_3 are port voltages.
This circuit can be described by the following equation system:

(1) $I_1 = M11 \times V_1 + M12 \times V_3 + M13 \times I_2$
(2) $V_2 = M21 \times V_1 + M22 \times V_3 + M23 \times I_2$
(3) $I_3 = M31 \times V_1 + M32 \times V_3 + M33 \times I_2$

Simplifications:

When the SLIC is connected to the SICOFI, we can assume that:

$I_2 = 0$ because of the high SICOFI input impedance. (In special cases the SICOFI input impedance can be included in the three-port model).

I_3 is not relevant in the following calculations because the SICOFI works as an ideal voltage generator. (The SICOFI output impedance of about 10 Ω may be included in the SLIC model).

According to the above agreements the equation system can be reduced to a pair of equations containing just four M-parameters:

(4) $I_1 = \text{M11} \times V_1 + \text{M12} \times V_3$
(5) $V_2 = \text{M21} \times V_1 + \text{M22} \times V_3$

These parameters M_{11}, M_{12}, M_{21}, M_{22} fully describe the SLIC and its external circuitry. They are defined as **shown in figures 5 through 8**.

→ Please verify that circuits of **figures 5 and 7** and of **figures 6 and 8** respectively are identical!

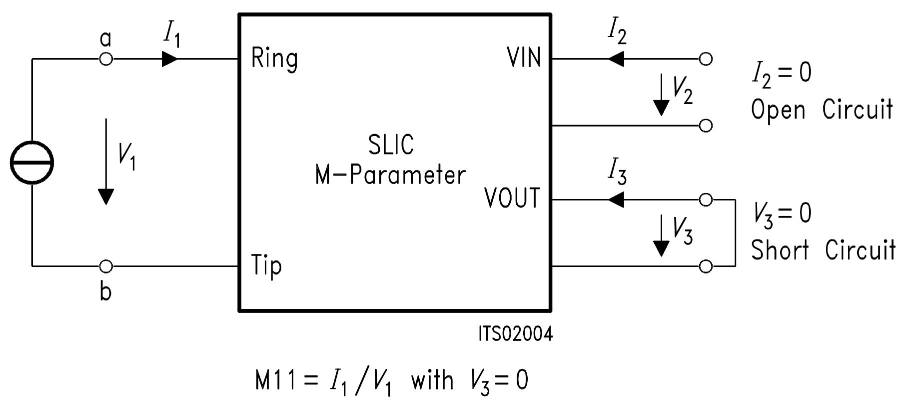


Figure 5

Definition of SLIC M11-Parameter

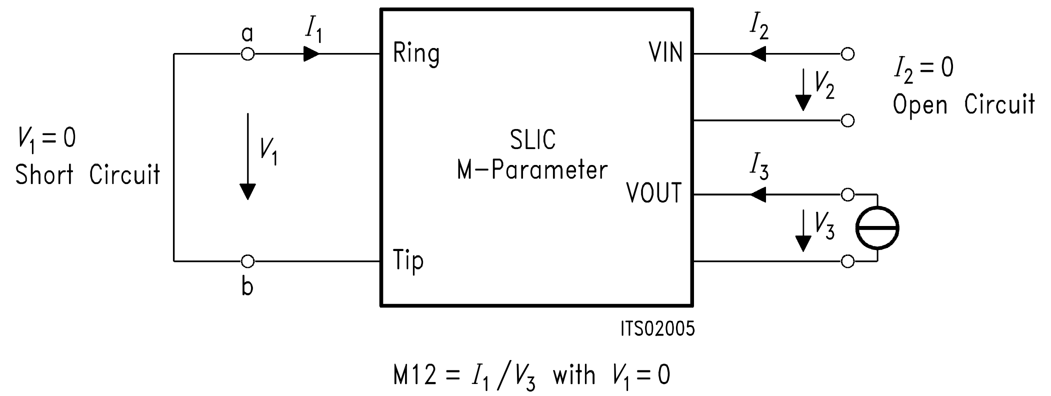


Figure 6

Definition of SLIC M12-Parameter

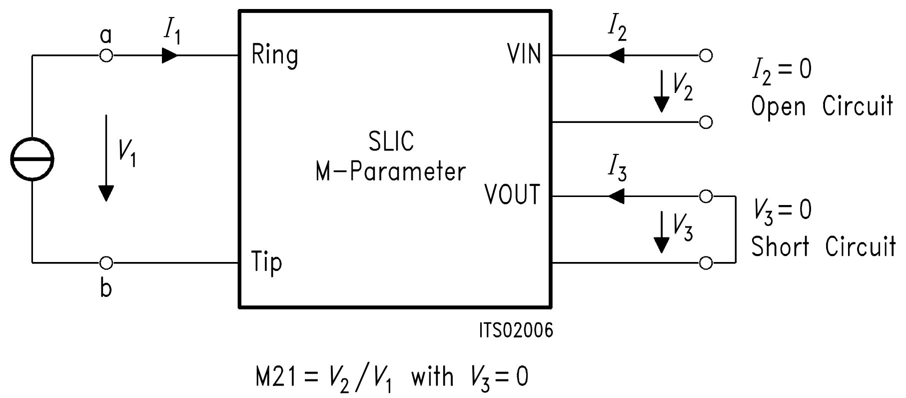


Figure 7

Definition of SLIC M21-Parameter

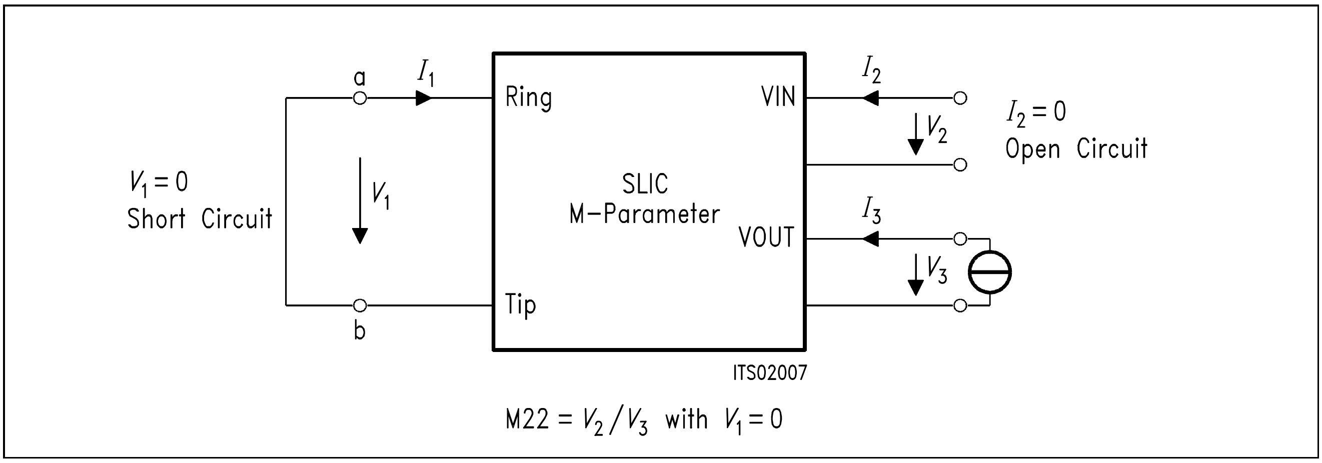


Figure 8

Definition of SLIC M_{22}-Parameter

2.2.2 ZSLI-Value

ZSLI is the **minimal attenuation** (resp. maximal gain) at the SLIC 4-wire side (Z-filter/SLIC loop).

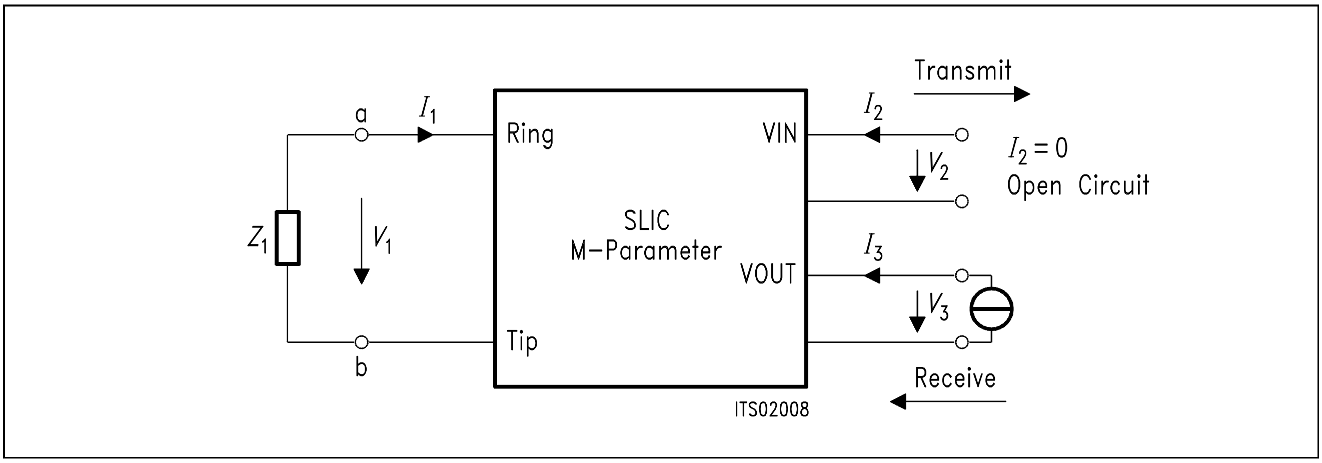


Figure 9

Definition of ZSLI

ZSLI is used by the SICOFI program during automatic calculation of Z-filter coefficients as a reference to check for possible oscillations in the SICOFI Z-filter + SLIC loop.
The value will be given in dB and is expressed as attenuation:

$$ZSLI = -20 \times \log(V_2/V_3)$$

→ Please verify that as V_2 is larger than V_3, ZSLI is a negative quantity.

Note: According to the Nyquist criteria, the attenuation of the closed loop "Z filter - SLIC" must be greater than 1 (gain < 0 dB) in the frequency band 0 – 16 kHz in order to avoid any oscillation.

3 SGS-Thomson SLIC L3030

The SGS-Thomson SLIC connects the SICOFI via the a,b lines to the subscriber. It has the following functions:

– Battery feeding
– Hybrid
– Ringing
– Ground-key detection
– OFF/ON-hook-detection
– Teletex signal injection

The SLIC divides into two parts, a low voltage part (L3030) and a high voltage part (L3000).

3.1 High Voltage Part L3000

The high voltage part is connected to the line. It realizes the battery feeding and switches the ringing and the speech signals in both directions through the SLIC.
The line current is programmable to 4 threshold values (25 mA, 30 mA, 45 mA, and 70 mA). An internal temperature sensing part shuts the line current off, when the temperature threshold is exceeded. The ringing signal is supplied by the battery on a small AC control-voltage (0.285 Vrms) at pin 26. The ringing signal starts and stops when the control signal crosses zero. The control signal is amplified and fed in balanced mode to the line with a superimposed DC voltage of 22 V.

3.1.1 DC Characteristics

In conversation mode the SLIC can work in Normal Battery or Boost Battery mode; with bit 3 of the signaling byte it is also possible to select the polarity of the DC line voltage. These possibilities have no influence on the transfer functions. In all these states the SLIC may operate as current generator, standard feeding system or as low impedance system.

a) Current generator
In this case the impedance of the SLIC is very high (> 20 kΩ) and the SLIC can supply currents of 25 mA, 30 mA, 45 mA, or 70 mA.

b) Standard feeding system
In this case the characteristic is equal to a – 48 V battery in series with two resistors, the values of which are set by external components.

c) Low impedance system
In this case the battery voltage is reduced to 33 V and the series resistors are reduced, too. With 'Boost Battery' this region cannot be reached.

These three working ranges are **shown in figure 10** below; the DC characteristic is selected by the resistor R_{DC}.

$$R_{DC} = 2 \times (R_{FS} - R_{P1}) \text{ with } R_{P1} = R_{P2}$$

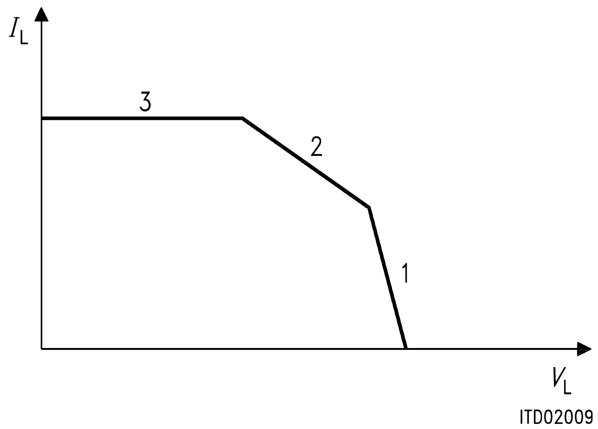


Figure 10

DC Characteristics I_{lim} = 25/30/45/70 mA

The resistor R_{DC} is to be used only in sections 1 and 2, and is infinite in section 3.

The value of R_{DC} influences also the internal block called K ('kernel'). In sections 2 and 3 the value of K equals K = 4/5 and in section 1 K = 5/12. The SLIC program already provides these two values. You only have to put the value of R_{DC} into the input file (**see section 4.1**).

3.1.2 AC Characteristics of the ST-SLIC

The ST-SLIC needs a large capacitance to block the DC from the 4-wire side of the SLIC. To save space and cost, the ST has a built-in capacitance multiplier. Thus the user requires just two small capacitors and a single resistor.

3.1.2.1 Model without Capacitor Multiplier

When not using the capacitor multiplier the customer needs only C_{AC1} and a connection between pins 7 and 14. The value of the (external) capacitor C_{AC1} is 47 µF.

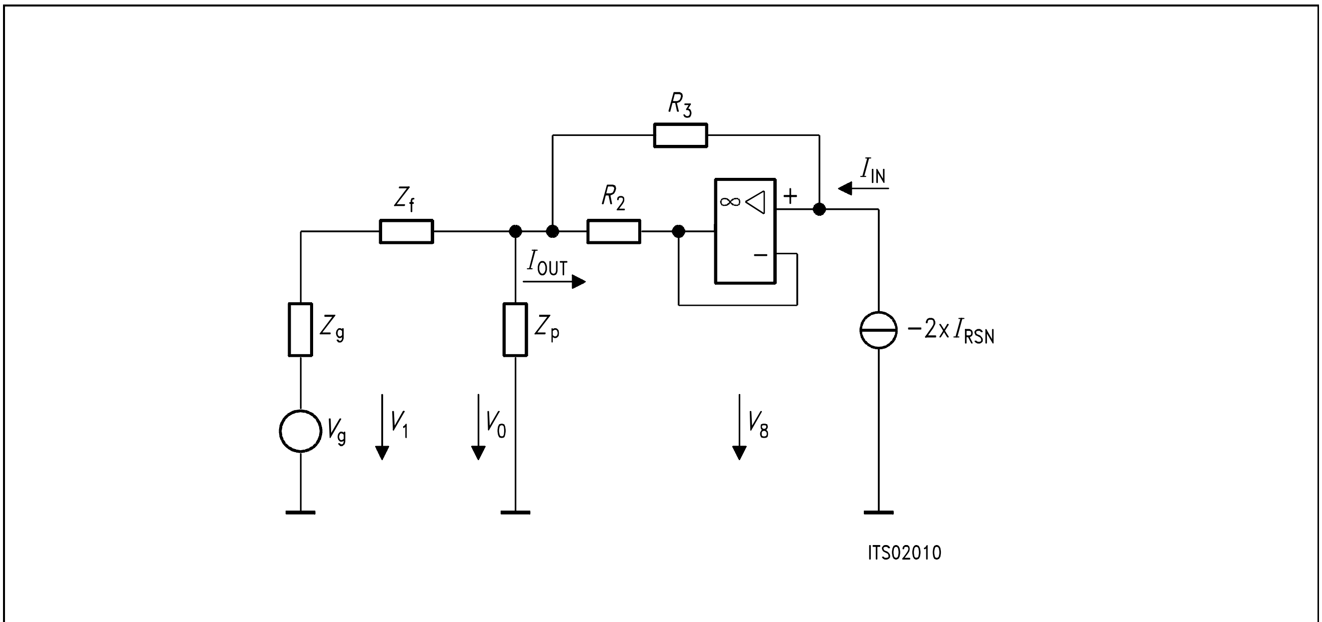


Figure 11

Circuit Diagram of the ST-SLIC

Note: K is dependent on the value R_{DC} (**see section 3.1.1**)

3.1.2.2 Model with Capacitor Multiplier

When using the capacitor multiplier you need C_{AC1}, C_{AC2} and R_R. The connection between pins 7 and 14 is shut off. The values used on the SLIC Babyboard STUS 3030 are:

C_{AC1} = 1 µF
C_{AC2} = 1 µF
R_R = 50 kΩ

With the above values the effective capacitance (to be used by the SLIC program) is 22 µF (see application note of ST-SLIC. – In the SLIC model of **figure 11** no multiplier is used).

3.2 Low Voltage Part L3030

The low voltage part controls the high voltage part L3000 in giving the proper information for setting line feed characteristics and injecting ringing and TTX signals. An on-chip digital interface (see below) allows to control all these operations. The L3030 defines working states of the line interface and also informs the controller via the SLD-bus about the line status.

3.3 Digital Interface

The Digital Interface has 5 pins:

E/Aread/write command

NCSchip select

DIOdata input/output

DCLKclock signal

CIchanging NCS signal from input to output:

in serial mode NCS is an input

in parallel mode NCS is an output

The Digital Interface is connected via a discrete logic to the SLD-interface.

The Digital Interface may work in serial or parallel mode.

The interface works in **serial mode** by connecting pin 21 to ground. Only in this mode all features of the SLIC (power-down, ringing, teletex signal, current setting) are available.

Because the timing of the ST-SLIC is different from that of the SICOFI, these two devices have to be connected via a discrete logic. A 3.3 kΩ resistor is inserted between the SIP-pin of the SICOFI and the SIP-wire, because the SLIC sends its last data when the SICOFI sends data too.

CI of the SLIC must be fixed to ground because NCS is only an input. DIO is connected to the SIP-wire. All other interface pins are connected to the discrete logic.

Figure 12 shows a block diagram of an analog line card supplying 16 subscribers using the ST-SLIC together with SICOFI, PBC and discrete logic. You can find the circuit diagram of the discrete logic in **figure 13**.

The **parallel mode** is chosen when a voltage higher than 4 V is put to pin 21.

The SLIC of the SLIC Babyboard STUS 3030 can work both with the serial interface or with the parallel interface. The serial interface, however, works only in connection with the SICOFI Testboard STUT 2060, because the discrete logic needs a signal 'SIGS' from the PBC. On the other hand, if the SICOFI-2 Board SIPB 5135 is used, the board works only with the parallel interface. It is selected by two jumpers (**not shown in figures 12 and 13**).

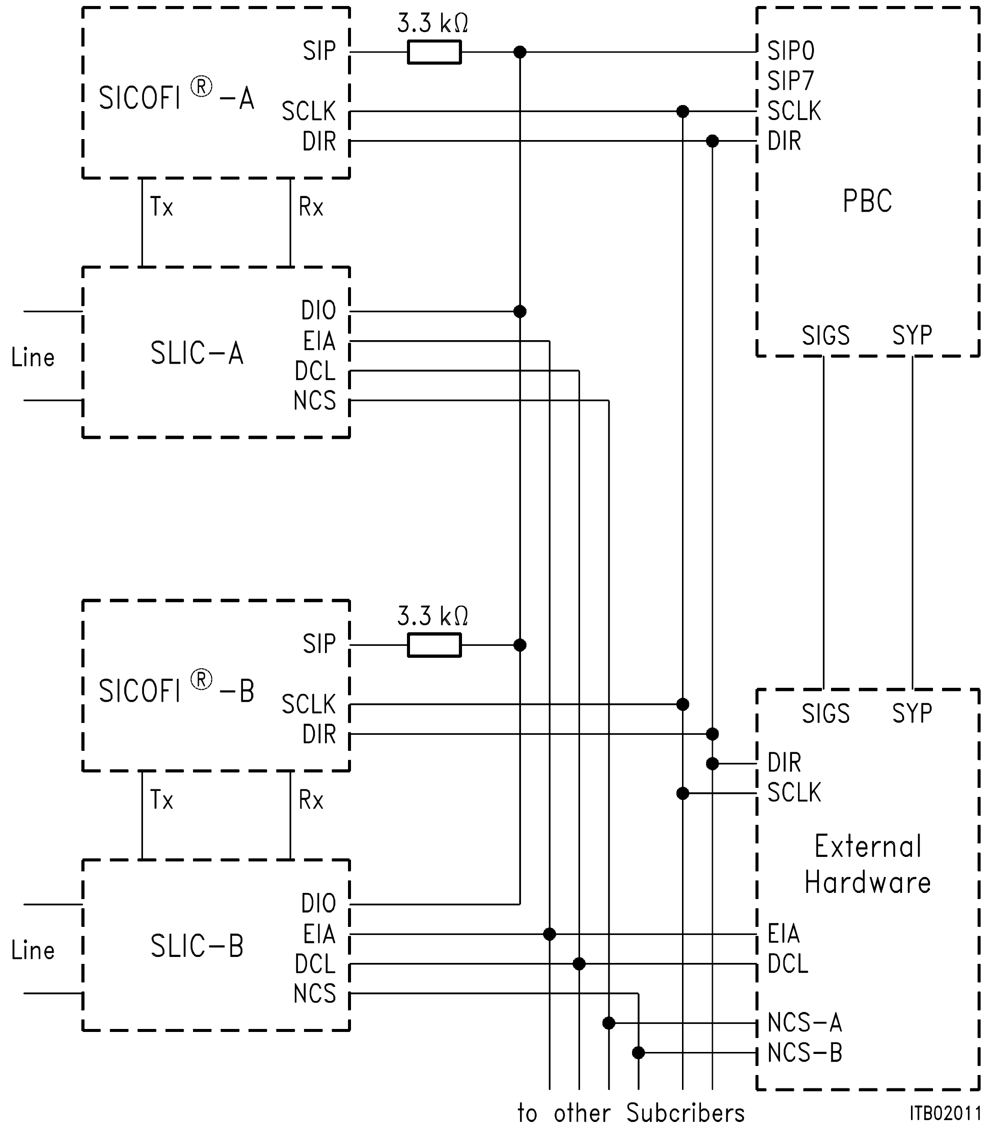


Figure 12

Block Diagram of an Analog Line Card Supplying 16 Subscribers

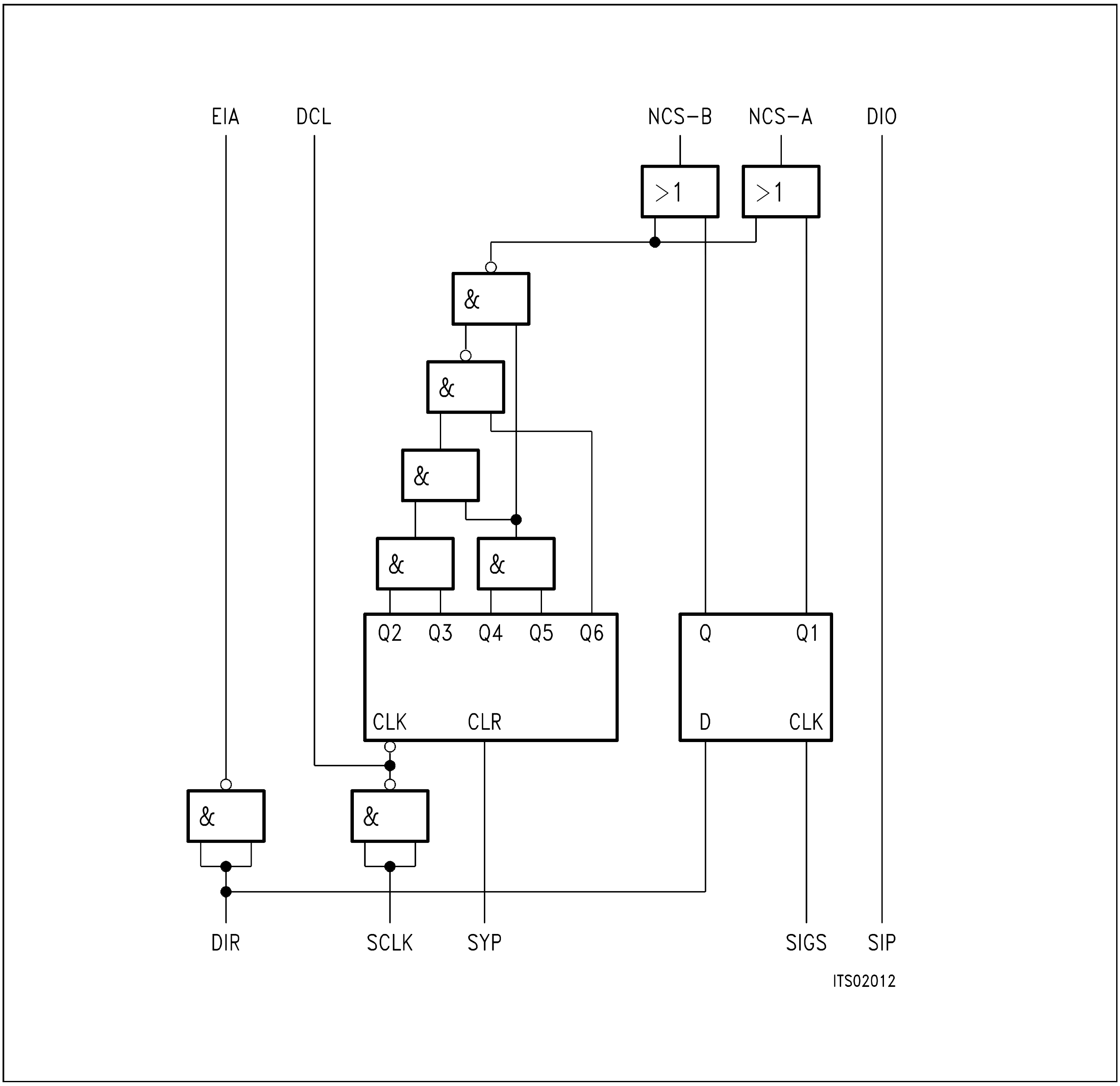


Figure 13

Discrete Logic for 16 Subscribers

3.4 Programming the ST-SLIC

The serial input port of the SLIC is connected to the SIP-lines of the Peripheral Board Controller (PBC) PEB 2050 and SICOFI. The discrete logic generates a chip select signal for the SLIC when the signaling byte is sent on the line. In this case the customer can use the signaling byte to program the SLIC.

Attention: Be aware of rotating the bit sequence of the signaling byte, because the PBC starts sending bit 7 ahead while the SLIC needs at first bit 0.

For example:

SIG0 = 80 power-up and line current I = 25 mA

SIG0 = 81 power-up and line current I = 30 mA

SIG0 = 82 power-up and line current I = 70 mA

SIG0 = 83 power-up and line current I = 45 mA

You have to program the SCR register of the PBC to generate a signal at the SIGS-pin of the PBC. With this signal the discrete logic creates a chip select signal for the particular SLIC:

SLIC-A	SCR = 90
SLIC-B	SCR = 50

Note: With a single PBC just two SLICs are to be controlled.

4 Calculations and Results

4.1 Calculations on the SLIC

The SLIC program requires an input file containing the values of the external circuitry for calculating the M-parameters which are written to a SLIC-file. This serves as an input file to the SICOFI program and thus you are able to calculate the SICOFI coefficients.

In receive direction the SLIC amplifiers the incoming signal and therefore it must be attenuated by the SICOFI. Because the required attenuation (> 12 dB) exceedes the possibilities of the SICOFI at its digital side, you need a voltage divider in receive direction or the analog attenuation of the SICOFI must be preset to 6 dB (AGR = 01).

The ST-SLIC has several external components:

Z_A	SLIC impedance balancing network
Z_B	line impedance balancing network
Z_{AC}, C_{AC1},	) DC feeding system, AC blocking and
R_{DC}, R_{PC}	) impedance matching
R_{REF}	bias resistance
C_{INT}	time constant

You do not need the Z_A-network!! Set Z_B to 10 kΩ and let the B-filter of the SICOFI make the balancing.

The components R_{REF} and C_{INT} do not influence the transfer functions and hence may be neglected. All other components are to be gathered into the input file. The capacitor C_{AC1} is taken with its actual value when the multiplier is not used; when the multiplier is used, a value of 22 µF has to be used in the input file.

The calculated M-parameters are:

$M11 = 1/Z_{ML}$

$M12 = 2 \times AR/Z_{ML}$

$M21 = AX$

$M22 = 2 \times AX + AR \times Z_B / (Z_A + Z_B)$

$Z_{ML} = (R_{DC} + R_{PC}) \times (1 + jw \times C \times R_{DC}) \times ((Z_{AC} \times R_{PC})/(R_{DC} + R_{PC}))/ (1 + jw \times C \times R_{DC})$

4.2 Format of the SICOFI® Input File

The SLIC program writes a table to the output file ST L3030.SLI. This output is the SICOFI input file. An example of this file is listed below:

```
* ST SLIC L3030
* VOR =  .50000      RIR =  .10000E+06  CKR =  .00000
* VOX =  1.0000      RIX =  10000.      CKX =  .10000E-05
* RP1ZA  .00000     RP1A =  .00000     RP1P =  .00000
* RP2ZA  .00000     RP2A =  .00000     RP2B =  .00000
* CP1ZA  .00000     CP1A =  .00000     CP1B =  .00000
* CP2ZA  .00000     CP2A =  .00000     CP2B =  .00000
* RSZAC  500.00     RSA =   .50000E+08 RSB =   100000
* CSZAC  .00000     CSA =   .00000     CSB =   .00000
* RPC =  100.00     RDC =   300.00     CAC =  .22000E-04
* CCOMP  .68000E-07
ZSLI
  1.0000
M11-TABLE
       10.000000000000000    2.265894E-03   -3.723228E-04
       20.000000000000000    1.991187E-03   -4.019077E-04
       30.000000000000000    1.849926E-03   -3.384906E-04
                        .
                        .
                        .
     3980.000000000000000    1.827491E-03    1.151429E-03
     3990.000000000000000    1.828295E-03    1.154225E-03
M12-TABLE
       10.000000000000000    2.265894E-03   -3.723228E-04
       20.000000000000000    1.991187E-03   -4.019077E-04
       30.000000000000000    1.849926E-03   -3.384906E-04
                        .
                        .
                        .
     3980.000000000000000    1.827491E-03    1.151429E-03
     3990.000000000000000    1.828295E-03    1.154225E-03
M21-TABLE
       10.000000000000000    2.830432E-01    4.504772E-01
       20.000000000000000    1.122734E-01    4.872317E-01
       30.000000000000000    1.803674E-01    4.139977E-01
                        .
                        .
                        .
     3980.000000000000000    9.999840E-01    3.998804E-03
     3990.000000000000000    9.999841E-01    3.988782E-03
M22-TABLE
       10.000000000000000    5.659732E-05    9.007743E-05
       20.000000000000000    1.224302E-04    9.742685E-05
       30.000000000000000    1.560423E-04    8.278299E-05
                        .
                        .
                        .
     3980.000000000000000    1.999568E-04    7.996009E-07
     3990.000000000000000    1.999568E-04    7.975970E-07
```

The leading comment lines (beginning with "*") document which SLIC is used. The first column of the M-parameter tables indicates the frequency value, from 10 to 3990 Hz in steps of 10 Hz. The second and the third columns give the real and imaginary part values respectively.

When modifying the .SLIC-file please note that these three values are separated by at least a single space character; every real number must contain a decimal point (FORTRAN "REAL" format).

4.3 Results

The SLIC was calculated using the parameters ’ST L3030.SLI’ of the SLIC program (ST L3030.EXE) in ST L3030.INP, and coefficients were calculated. The result file of the SICOFI program was stored in ’ST L3030.RES’ and the calculated programming bytes in ’ST L3030.BYT’.

With these bytes the SICOFI has been programmed and measurements have been taken with a "PCM4" of Wandel & Goltermann, using the SLIC board pluged into the STUT 2060 test board as shown in appendix D. The measurements comprise the levels in transmit direction (AD) and in receive direction (DA), the attenuation distortion (AD and DA), the transhybrid loss (DD), and the 2-wire impedance return loss.

The plots of measurements can be found in appendix E.

The plot masks correspond to CCITT Recommendations G.712 and G.714.

4.4 Comparison of Measurements and Simulations

Measurements have been taken on a SLIC L3030 including the capacitance multiplier. In general the measurements conform with the calculations within small differences. Only the high attenuation of calculated echo return loss could not be reached experimentally.

Appendix A: Input File ’ST L3030.INP’

```
VOR=
0.5
RIR=
100.E03
CKR=
0.
VOX=
1.0
RIX=
10000.
CKX=
1.0E-06
RP1ZAC=
0.
RP2ZAC=
0.
CP1ZAC=
0.0
CP2ZAC=
0.
RSZAC=
500.
CSZAC=
0.
RP1A=
0.
RP2A=
0.
CP1A=
0.
CP2A=
0.
RSA=
50.E06
CSA=
0.
RP1B=
0.
RP2B=
0.
CP1B=
0.
CP2B=
0.
RSB=
10000.
CSB=
0.
RPC=
100.
```

```
RDC=
300.
CAC=
22.E-06
CCOMP
68.0E-09
ZSLI=
1
```

Appendix B: Program ’ST L3030.FOR’

```
C######################################################################
#
C
      PROGRAM SGS
C     08.06.90  Udo Stueting

C######################################################################
#
      IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
*
      INTEGER IN,OUT,I
      CHARACTER*14 BUFF1,BUFF2*7,BUFF3*7,BUF4*7,BUF5*7
      CHARACTER*7 BUF6,BUF7*7,BUF8*7,BUF9*7,BUF2*12,BUF3*12
       CHARACTER*7 BUF10*7,BUF11*7,BUF12*7,BUF13*7,BUF14*7,BUF15*7
       CHARACTER*7 BUF16*7,BUF17*7,BUF18*7,BUF19*7,BUF20*7,BUF21*7
       CHARACTER*7 BUF22*7,BUF23*7,BUF24*7,BUF25*7,BUF26*7,BUF 27*7
       CHARACTER*7 BUF28*7,BUF29*7,BUF30*7,BUF31*7
      CHARACTER  BUF1*12,FILEOUT*12,ANSW*1,INFILE*12
      REAL*8 FREQ
      REAL*8 VOR,RIR,CKR,VOX,RIX,CKX,PI2,ZSLI
      REAL*8 P1A,RP2A,CP1A,CP2A,RSA,CSA,RP1B,RP2B,CP1B,CP2B,RSB,CSB
      REAL*8 RP1ZAC,RP2ZAC,CP1ZAC,CP2ZAC,RSZAC,CSZAC
      REAL*8 RPC,RDC,CAC,CCOMP,RGTTX
       COMPLEX*8 M11,M12,M21,M22,Z,ZA,ZB,ZAC,ZML,AX,AR,ZM,TTX

*
          COMMON /ARC/ RIR,CKR,VOR
          COMMON /AXC/ RIX,CKX,VOX
          COMMON /PI2C/ PI2
          COMMON /SGSC/ RPC,RDC,CAC,CCOMP
          COMMON /ZACC/RP1ZAC,RP2ZAC,CP1ZAC,CP2ZAC,RSZAC,CSZAC
          COMMON /ZAC/ RP1A,RP2A,CP1A,CP2A,RSA,CSA
          COMMON /ZBC/ RP1B,RP2B,CP1B,CP2B,RSB,CSB
C     ONLY FOR TTX-Filter (PIN 34 of L3030)
          COMMON /TTXC/ RGTTX
C
C*********************************************************************
C      Initialization part

C*********************************************************************
```

```
C
      DATA BUFF1/'* ST SLIC L3030 '/
      DATA BUF2/'* VOR ='/,BUF3/'  RIR ='/,BUF4/'  CKR ='/
      DATA BUF5/'* VOX ='/,BUF6/'  RIX ='/,BUF7/'  CKX ='/
      DATA BUF8/'* RP1ZAC ='/,BUF9/' RP1A ='/BUF10/' RP1B ='/
      DATA BUF11/'* RP2ZAC ='/,BUF12/' RP2A ='/BUF13/' RP2B ='/
      DATA BUF14/'* CP1ZAC ='/,BUF15/' CP1A ='/BUF16/' CP1B ='/
      DATA BUF17/'* CP2ZAC ='/,BUF18/' CP2A ='/BUF19/' CP2B ='/
      DATA BUF20/'* RSZAC ='/,BUF21/' RSA ='/BUF22/' RSB ='/
      DATA BUF28/'* CSZAC ='/,BUF29/' CSA ='/BUF30/' CSB ='/
      DATA BUF23/'* RPC ='/,BUF24/' RDC ='/BUF25/'  CAC ='/
      DATA BUF27/'* CCOMP ='/
C    ONLY FOR TTX-Filter (PIN 34 of L3030)
C      DATA BUF27/'* CCOMP =',BUF31/'RGTTX ='/
      DATA BUF26/' ZSLI ='/
*
        OUT = 6
        IN  = 5
        PI2     = 4.*DASIN(1.D0)
        FILEOUT = ' '
            WRITE(OUT,'(A)')
     &     ' Enter input file name(xxxxxxxx.INP):  '
10          READ (IN,'(A)') INFILE
             IF (INDEX(INFILE,' ').EQ.1
     &         .OR.(INDEX(INFILE,'.INP').EQ.0
     &              .AND.INDEX(INFILE,'.inp').EQ.0)) THEN
                 WRITE (OUT,'(A)') ' Enter correct input file name:
'
                 INFILE=' '
                GOTO 10
             ENDIF
        WRITE (OUT,'(A)') ' Enter output file name (xxxxxxxx.SLI): '
20     READ (IN,'(A)') FILEOUT
        IF (INDEX(FILEOUT,' ').EQ.1) THEN
            WRITE (OUT,'(A)')
     &     'Enter correct output file name (with extention  .SLI): '
            FILEOUT=' '
            GOTO 20
        ENDIF
        OPEN (30, FILE=FILEOUT, ERR=1000, STATUS= 'UNKNOWN')
             OPEN (10, FILE=INFILE, ERR=1100, STATUS= 'OLD')
             READ(10,'(A)')
             WRITE(6,*) 'Reading input file'
             READ(10,*) VOR
             READ(10,'(A)')
             READ(10,*) RIR
             READ(10,'(A)')
             READ(10,*) CKR
             READ(10,'(A)')
             READ(10,*) VOX
             READ(10,'(A)')
             READ(10,*) RIX
             READ(10,'(A)')
             READ(10,*) CKX
             READ(10,'(A)')
             READ(10,*) RP1ZAC
```

```
              READ(10,'(A)')
              READ(10,*) RP2ZAC
              READ(10,'(A)')
              READ(10,*) CP1ZAC
              READ(10,'(A)')
              READ(10,*) CP2ZAC
              READ(10,'(A)')
              READ(10,*) RSZAC
              READ(10,'(A)')
              READ(10,*) CSZAC
              READ(10,'(A)')
              READ(10,*) RP1A
              READ(10,'(A)')
              READ(10,*) RP2A
              READ(10,'(A)')
              READ(10,*) CP1A
              READ(10,'(A)')
              READ(10,*) CP2A
              READ(10,'(A)')
              READ(10,*) RSA
              READ(10,'(A)')
              READ(10,*) CSA
              READ(10,'(A)')
              READ(10,*) RP1B
              READ(10,'(A)')
              READ(10,*) RP2B
              READ(10,'(A)')
              READ(10,*) CP1B
              READ(10,'(A)')
              READ(10,*) CP2B
              READ(10,'(A)')
              READ(10,*) RSB
              READ(10,'(A)')
              READ(10,*) CSB
              READ(10,'(A)')
              READ(10,*) RPC
              READ(10,'(A)')
              READ(10,*) RDC
              READ(10,'(A)')
              READ(10,*) CAC
              READ(10,'(A)')
              READ(10,*) CCOMP
              READ(10,'(A)')
C     ONLY FOR TTX-Filter (PIN 34 of L3030)
C              READ(10,*) RGTTX
C              READ(10,'(A)')
              READ(10,*) ZSLI
              CLOSE (10)
```

```
C
C*******************************************************************
C       Documentation part
C*******************************************************************
C
        WRITE (30,'(A)') BUFF1
        WRITE (BUFF1,'(G12.5)') VOR
        WRITE (BUFF2,'(G12.5)') RIR
        WRITE (BUFF3,'(G12.5)') CKR
        WRITE (30,'(A)') BUF2//BUFF1//BUF3//BUFF2//BUF4//BUFF3
        WRITE (BUFF1,'(G12.5)') VOX
        WRITE (BUFF2,'(G12.5)') RIX
        WRITE (BUFF3,'(G12.5)') CKX
        WRITE (30,'(A)') BUF5//BUFF1//BUF6//BUFF2//BUF7//BUFF3
        WRITE (BUFF1,'(G12.5)') RP1ZAC
        WRITE (BUFF2,'(G12.5)') RP1A
        WRITE (BUFF3,'(G12.5)') RP1B
        WRITE (30,'(A)') BUF8//BUFF1//BUF9//BUFF2//BUF10//BUFF3
        WRITE (BUFF1,'(G12.5)') RP2ZAC
        WRITE (BUFF2,'(G12.5)') RP2A
        WRITE (BUFF3,'(G12.5)') RP2B
        WRITE (30,'(A)') BUF11//BUFF1//BUF12//BUFF2//BUF13//BUFF3
        WRITE (BUFF1,'(G12.5)') CP1ZAC
        WRITE (BUFF2,'(G12.5)') CP1A
        WRITE (BUFF3,'(G12.5)') CP1B
        WRITE (30,'(A)') BUF14//BUFF1//BUF15//BUFF2//BUF16//BUFF3
        WRITE (BUFF1,'(G12.5)') CP2ZAC
        WRITE (BUFF2,'(G12.5)') CP2A
        WRITE (BUFF3,'(G12.5)') CP2B
        WRITE (30,'(A)') BUF17//BUFF1//BUF18//BUFF2//BUF19//BUFF3
        WRITE (BUFF1,'(G12.5)') RSZAC
        WRITE (BUFF2,'(G12.5)') RSA
        WRITE (BUFF3,'(G12.5)') RSB
        WRITE (30,'(A)') BUF20//BUFF1//BUF21//BUFF2//BUF22//BUFF3
        WRITE (BUFF1,'(G12.5)') CSZAC
        WRITE (BUFF2,'(G12.5)') CSA
        WRITE (BUFF3,'(G12.5)') CSB
        WRITE (30,'(A)') BUF28//BUFF1//BUF29//BUFF2//BUF30//BUFF3
        WRITE (BUFF1,'(G12.5)') RPC
        WRITE (BUFF2,'(G12.5)') RDC
        WRITE (BUFF3,'(G12.5)') CAC
        WRITE (30,'(A)') BUF23//BUFF1//BUF24//BUFF2//BUF25//BUFF3
        WRITE (BUFF1,'(G12.5)') CCOMP
        WRITE (30,'(A)') BUF27//BUFF1
C     ONLY FOR TTX-Filter (PIN 34 of L3030)
C        WRITE (BUFF2,'(G12.5)') RGTTX
C        WRITE (30,'(A)') BUF27//BUFF1//BUF31//BUFF2
        WRITE (30,'(A)') 'ZSLI'
        WRITE (30,'(G12.5)') ZSLI
C
```

```
C
C*******************************************************************
C       Calculation part
C*******************************************************************
C
C         M11 = 1. / ZML
C
        ZM = CMPLX(1.,0.)
        WRITE (OUT,*) ' Running M11 calculation...'
        WRITE (30,'(A)') 'M11-TABLE'
        DO 100 I=1,399
             FREQ = DBLE(I*10)
             CALL YZML(FREQ,ZML)
             M11 = ZM / ZML
             WRITE (30,*) FREQ,REAL(M11),AIMAG(M11)
100     CONTINUE
C
C         M12 = 2.0*AR/ZML
C
        WRITE (OUT,*) ' Running M12 calculation...'
        WRITE (30,'(A)') 'M12-TABLE'
        DO 110 I=1,399
               FREQ = DBLE(I*10)
             CALL ARW(FREQ,AR)
             CALL YZML(FREQ,ZML)
             M12 = 2. * AR / ZML
             WRITE (30,*) FREQ,REAL(M12),AIMAG(M12)
110     CONTINUE
C
C         M21 = AX * TTX
C
        WRITE (OUT,*) ' Running M21 calculation...'
        WRITE (30,'(A)') 'M21-TABLE'
        DO 120 I=1,399
             FREQ = DBLE(I*10)
           CALL AXW(FREQ,AX)
           CALL TTXW(FREQ,TTX)
           M21 = AX * TTX
           WRITE (30,*) FREQ,REAL(M21),AIMAG(M21)
120     CONTINUE
C
C       M22 = 2*AX*TTX*AR*(ZB/(ZA+ZB))
C
        WRITE (OUT,*) ' Running M22 calculation...'
        WRITE (30,'(A)') 'M22-TABLE'
        DO 130 I=1,399
            FREQ = DBLE(I*10)
            CALL AXW(FREQ,AX)
            CALL ARW(FREQ,AR)
            CALL YZA(FREQ,ZA)
          CALL YZB(FREQ,ZB)
            CALL TTXW(FREQ,TTX)
            M22 = 2. * AX * AR * TTX
          Z = ZB / (ZA+ZB)
          M22 = M22 * Z
            WRITE (30,*) FREQ,REAL(M22),AIMAG(M22)
```

```
130     CONTINUE
          WRITE(30,'(A1)') ';'
          CLOSE (30)
        WRITE(OUT,'(A)') ' Data written in file: '//FILEOUT
        STOP
1000    WRITE(OUT,'(A)') ' OPEN ERROR AT OUTPUT-FILE: '//FILEOUT
        STOP 1
1100    WRITE(OUT,'(A)') ' OPEN ERROR AT INPUT-FILE: '//INFILE
          STOP 2
        END
```

```
C
C####################################################################
C
      SUBROUTINE ARW(FREQ,AR)
C
C####################################################################
C
C     Name of Subroutine:     ARW
C
C     Formal parameter list:  FREQ,AR
C
C     Input parameters:
C        FREQ    (DOUBLE)
C
C     Output parameters:
C        ARW     (DOUBLE)   ARRAY  2
C
C     Task of this routine: VOR*jwRIR*CKR/(1.+jwRIR*CKR)C
C
C####################################################################
C
          IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
*
          REAL*8 FREQ,RIR,CKR,VOR,OMP,PI2
          COMPLEX AR,V1,V2
*
          COMMON /ARC/ RIR,CKR,VOR
          COMMON /PI2C/ PI2
*
          AR = CMPLX(1.,0.)
        IF (CKR.EQ.0) THEN
         GOTO 10
        ELSE
           OMP = PI2*FREQ*RIR*CKR
           V1 = CMPLX(0.,OMP)
           V2 = CMPLX(1.D0,OMP)
           AR = V1 / V2
          ENDIF
10        AR = AR*VOR
          RETURN
          END
```

```
C
C#################################################################
C
      SUBROUTINE AXW(FREQ,AX)
C
C#################################################################
C
C     Name of Subroutine:     AXW
C
C     Formal parameter list:  FREQ,AX
C
C     Input parameters:
C         FREQ    (DOUBLE)
C
C     Output parameters:
C         AX      (DOUBLE)   ARRAY  2
C
C     Task of this routine:
C
C#################################################################
C
          IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
*
          REAL*8 FREQ,RIX,CKX,VOX,OMP,PI2
        COMPLEX AX,V1,V2
*
          COMMON /AXC/ RIX,CKX,VOX
          COMMON /PI2C/ PI2
*
          AX = CMPLX(1.,0.)
          IF (CKX.EQ.0) THEN
           GOTO 10
          ELSE
           OMP = PI2*FREQ*RIX*CKX
           V1 = CMPLX(0.,OMP)
           V2 = CMPLX(1.D0,OMP)
         AX = V1 / V2
        ENDIF
 10       AX = AX*VOX
          RETURN
          END
```

```
C
C####################################################################
C
      SUBROUTINE YZML(FREQ,ZML)
C
C####################################################################
C
C     Name of Subroutine:     YZML
C
C     Formal parameter list:  FREQ
C
C     Input parameters:
C
C     Output parameters:
C
C     Common blocks:
C
C     Task of this routine:
C
C     Required subroutines:
C
C     Required functions:
C
C     Routine called in the following subroutines or functions:
C
C####################################################################
C
      IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
      REAL*8 FREQ,RPC,CCOMP
      REAL*8 RP1ZAC,RP2ZAC,CP1ZAC,CP2ZAC,RSZAC,CSZAC
      REAL*8 RDC,CAC,PI2
      COMPLEX ZAC,ZML,ZMLZ,ZMLN,ZML1,XC
*
        COMMON /PI2C/ PI2
        COMMON /SGSC/ RPC,RDC,CAC,CCOMP
        COMMON /ZACC/RP1ZAC,RP2ZAC,CP1ZAC,CP2ZAC,RSZAC,CSZAC
*
      CALL IMPED6(RP1ZAC,RP2ZAC,CP1ZAC,CP2ZAC,RSZAC,CSZAC,FREQ,ZAC)
      IF (CCOMP.EQ.0) THEN
       GOTO 10
      ELSE
       XC = CMPLX(0.,( -1./(PI2*FREQ*CCOMP)))
       ZML = ZAC * XC
       ZMLZ= ZAC + XC
       ZAC = ZML / ZMLZ
      END IF
10    ZMLZ = ZAC + RPC
      ZMLN = RPC + RDC
      ZML1 = ZMLZ / ZMLN
      ZML = CMPLX(0.,(PI2 *FREQ*CAC*RDC))
```

```
      ZML = ZML1 * ZML
      ZML = 1 + ZML
      ZMLZ = ZMLN * ZML
      ZMLN = CMPLX(1.,(PI2*FREQ*CAC*RDC))
      ZML = ZMLZ / ZMLN
      RETURN
      END
C
C##############################################################
C
      SUBROUTINE YZA(FREQ,ZA)
C
C##############################################################
C
C     Name of Subroutine:     YZA
C
C     Formal parameter list:  FREQ
C
C     Input parameters:
C
C     Output parameters:
C
C     Common blocks:
C
C     Task of this routine:
C
C     Required subroutines:
C
C     Required functions:
C
C     Routine called in the following subroutines or functions:
C
C##############################################################
C
      IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
      REAL*8 FREQ
      REAL*8 RP1A,RP2A,CP1A,CP2A,RSA,CSA
      COMPLEX ZA
*
      COMMON /ZAC/ RP1A,RP2A,CP1A,CP2A,RSA,CSA
*
      CALL IMPED6(RP1A,RP2A,CP1A,CP2A,RSA,CSA,FREQ,ZA)
      RETURN
      END
```

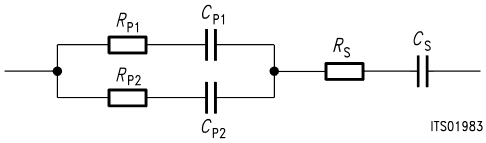
```
C
C#################################################################
C
      SUBROUTINE YZB(FREQ,ZB)
C
C#################################################################
C
C     Name of Subroutine:     YZB
C
C     Formal parameter list:  FREQ
C
C     Input parameters:
C
C     Output parameters:
C
C     Common blocks:
C
C     Task of this routine:
C
C     Required subroutines:
C
C     Required functions:
C
C     Routine called in the following subroutines or functions:
C
C#################################################################
C
      IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
      REAL*8 FREQ
      REAL*8 RP1B,RP2B,CP1B,CP2B,RSB,CSB
      COMPLEX ZB
*
      COMMON /ZBC/RP1B,RP2B,CP1B,CP2B,RSB,CSB
*
      CALL IMPED6(RP1B,RP2B,CP1B,CP2B,RSB,CSB,FREQ,ZB)
      RETURN
      END


C
C#################################################################
C
      SUBROUTINE TTXW(FREQ,TTX)
C
C#################################################################
C
C     Name of Subroutine:     TTXW
C
C     This subroutine calculates the Transfer function of the
C       TTX-filter at pin 34 and pin 35.
C
C     Formal parameter list:  FREQ,TTX
```

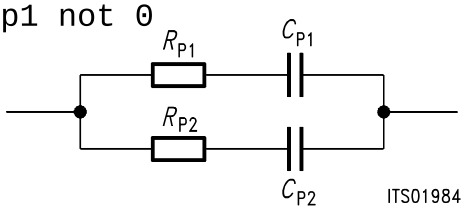
```
C
C     Input parameters:
C        FREQ    (DOUBLE)
C
C     Output parameters:
C        TTX     (COMPLEX)
C
C     Task of this routine:
C
C#############################################################
C
          IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
*
          REAL*8 FREQ,RGTTX,OMP,PI2
          COMPLEX TTX
*
          COMMON /TTXC/ RGTTX
          COMMON /PI2C/ PI2
*
        OMP = FREQ * PI2
          TTX = CMPLX(1.,0.)
          RETURN
          END
C

C############################################################C
C###                                                      ###C
      SUBROUTINE IMPED6(RP1,RP2,CP1,CP2,RS,CS,FREQ,Zeq)
C###                                                      ###C
C###  Modification Klaus Kliese 27.08.89                  ###C
C###                                                      ###C
C###  Note: when a parameter is set to 0 then the         ###C
C###  corresponding resistor or capacitance does not      ###C
C###  exist                                               ###C
C###                                                      ###C
C###  Formal parameter list:RP1,RP2,CP1,CP2,RS,CS,FREQ,Zeq ###C
C###                                                      ###C
C###  Input parameters:                                   ###C
C###      RS     [ REAL ]   ; series resistance           ###C
C###      CS     [ REAL ]   ; series capacitance          ###C
C###      RP1    [ REAL ]   ; parallel resistance         ###C
C###      RP2    [ REAL ]   ; parallel resistance         ###C
C###      CP1    [ REAL ]   ; parallel capacitance        ###C
C###      CP2    [ REAL ]   ; parallel capacitance        ###C
C###      FREQ   [ REAL ]   ; frequency                   ###C
```

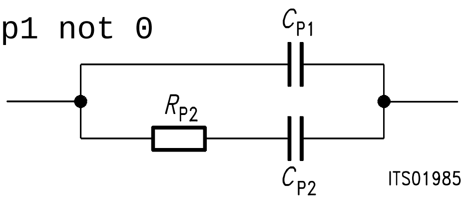
```
C###  Output parameters:                                        ###C
C###      Zeq     [ COMPLEX ]                                   ###C
C###                                                            ###C
C###  Common blocks:  QPI2                                       ###C
C###                                                            ###C
C###  Task of this routine: Equivalent impedance of:            ###C
C###                                                            ##
```



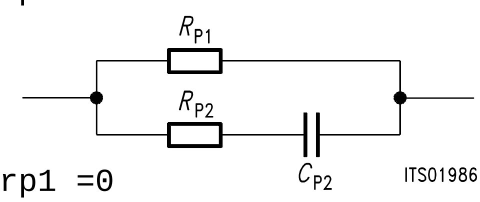

```
C###                                                           ###C
C### SPECIAL CASES:                                             ###C
C###          A. SYSTEM Parallel                                ###C
C###             1. CP1 not 0                                   ###C
C###                1.1 rp1 not 0                               ##
```



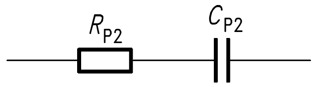

```
C###                1.2 rp1 not 0                               ##
```




```
c###                                                           ###C
C###             2. CP1 =0                                      ###C
C###                2.1 rp1  not 0                              ##
```



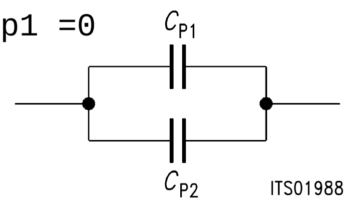

```
C###                2.2 rp1 =0                                  ##
```



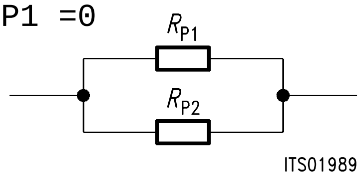

```
C###             3. idem  if CP2  = 0                           ##
```

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```
C###                                                            ##
C###             4. RP2 =0 and rp1 =0                           ##
```

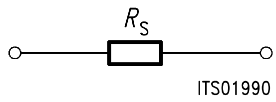



```
C###             5. CP2 =0 and CP1 =0                           ##
```

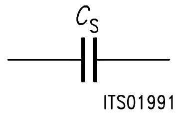



```
C###                                                           ###C
```

```
C###             B.System Series                                ###C
C###               1. CS = 0                                    ###C
C###                                                            ###C
```




```
C###               1. RS = 0                                    ###C
C###                                                            ###C
C###                idem  system A                              ###C
```




```
C###                                                            ###C
C###             C.Conclusion: Zeq = sum of the two             ###C
C###                           systems in any case              ###C
C###                                                            ###C
C##############################################################
#C
      REAL*8 CP1,CP2,RP1,RP2
      REAL*8 CS,RS,N,UL
      REAL*8 FREQ,PI2,OMEGA
      COMPLEX D,C,Zeq,ZA,ZB
*
      COMMON /PI2C/ PI2
*
      OMEGA = PI2*FREQ
      IF (CP1.EQ.0) THEN
         C=CMPLX(RP1,0.)
      ELSE
CKL 26.7.89   C = RP1 + 1 / j*OMEGA*CP1
         C = RP1 + (1. / CMPLX(0.,OMEGA*CP1))
      ENDIF
      IF (CP2.EQ.0) THEN
         D=CMPLX(RP2,0.)
      ELSE
CKL 26.7.89   D = RP2 + 1 / j*OMEGA*CP2
         D = RP2 + (1. / CMPLX(0.,OMEGA*CP2))
      ENDIF
      N  = CABS(C)
      UL = CABS(D)
* if one of them is 0 then no parallel calculation
      IF ((N.EQ.0).OR.(UL.EQ.0)) then
           ZA=C+D
      ELSE
*  ZA = C & D in parallel
           ZA=C*D/(C+D)
      ENDIF
C System series
      IF (CS .EQ.0) THEN
         ZB=CMPLX(RS,0.)
      ELSE
         ZB = RS +( 1. / CMPLX(0.,OMEGA*CS))
      ENDIF
c both
       Zeq=ZA+ZB
       RETURN
       END
C
C##############################################################C
```

Appendix C: Spec File 'ST L3030.SPE'

This specification file contains the specifications of the 'Deutsche Bundespost'.

```
FREF = 1014.0    LAW = A
VREF= 0.9480  RLX = 0.    RLR =  -7.0
ABIMP  = ZI
ZLRP1= 820.      ZLCP1= 0.    ZLRP2= 0.    ZLCP2= 0.115E-06
ZLRS = 220.      ZLCS = 0.
ZIRP1= 820.      ZICP1= 0.    ZIRP2= 0.    ZICP2= 0.115E-06
ZIRS = 220.      ZICS = 0.
Z3RP1= 820.      Z3CP1= 0.    Z3RP2= 0.    Z3CP2= 0.115E-06
Z3RS = 220.      Z3CS = 0.
ZRRP1= 820.      ZRCP1= 0.    ZRRP2= 0.    ZRCP2= 0.115E-06

ZRRS = 220.      ZRCS = 0.
ZRE
FR           300        500       3k       3.4k
AT-          0          20        20         16
AT+         16         20        20          0

ZMIR
FR            4k        12k
AT-          30         3
AT+          30         3

DA,UPPER
FR         300    500    2.7k     3k      3.4k
AT-       100    .75    .25       .35       .75
AT+        .75    .25    .35       .75     100

DA,LOWER
FR         300         3.4k
AT-        0           -.25
AT+        -.25         0

DA,DELAY
FR           500        600       1k       2.6k   2.8k
GD-         10k       .420       .150      .085      .150
GD+         .420        .150       .085       .150    10k

AD,UPPER
FR         300    500    2.7k     3k      3.4k
AT-       100    .75    .25       .35       .75
AT+        .75    .25    .35       .75     100

AD,LOWER
FR         300         3.4k
AT-        0           -.25
AT+        -.25         0
```

```
AD,DELAY
FR             500          600         1k         2.6k     2.8k
GD-           10k         .420         .150        .085        .150
GD+           .420          .150         .085        .150    10k
DD
FR             300          500        2.5k        3.4k
AT-          0            27            27            23
AT+           23            27            27           0
```

Appendix D: Result File 'ST L3030.RES'

```
Input file name: ST L3030.CTL         Date:  08.06.90 14:18
SPEC = L3030.SPE                      SLIC = ST L3030.SLI
BYTE =REF.BYT                         CHNR =  0,A
PLQ  = N
ON = ALL              VERSION = 4.4              SHORT = N
OPT =  Z+X+R+B        ZXRB =  NNNN                 REL = Y
ZAUTO = Y              ZREP = N     ZSIGN =  1
FZ =     300.00       3400.0       ZLIM =  2.00
FR =     300.00       3200.0
RDISP = Y             RREFQ = N    RREF =  3.1501
FX =     300.00       3400.0
XDISP = Y             XREFQ = N    XREF = -.50486
BAUTO = Y             BREP = N     BSIGN =  1
FB =     300.00       3400.0       BLIM =  2.00    BDF =  1
APRE = .00     DPRE = .00     APOF = .00     DPOF = .00
AGX  = 00        AGR  = 00        TM3  = 000
XZQ =  -.39062500E+00  -.17639160E-01   .93505860E-01
        .38574220E-01  -.11328130E+00
XRQ =   .81250000E+00  -.19140630E-00  -.41503910E-02
       -.85449220E-02   .48828130E-02
XXQ =   .10317380E+01   .33691410E-01  -.48828130E-02
       -.61035160E-02   .12207030E-03
XBQ =  -.13671880E+00  -.32812500E+00  -.32031250E+00
        .69580080E-02   .44921880E-01
       -.11132810E+00  -.17333980E-01   .92773440E-01
       -.95703130E-01   .44921880E-01
XGQ =   .52001950E+00   .16406250E+01
;

Bytes for Z-Filter (13):          B0,1C,25,4C,F1,3E,95,BA
Bytes for R-Filter (2B):          70,1A,4F,F1,C9,AA,0C,1B
Bytes for X-Filter (23):          70,E8,AF,FB,1A,45,02,65
Bytes for Gain-factors (30):      51,32,10,32
2nd part of bytes B-Filter (0B):  00,15,BB,CA,14,ED,B3,BB
1st part of bytes B-Filter (03):  5B,B1,B7,AB,32,2A,B2,14
Bytes for B-filter delay (18):    19,19,11,19

* ST SLIC L3030
* VOR =  .50000      RIR =  .10000E+06  CKR =  .00000
* VOX =  1.0000      RIX =  10000.      CKX =  .10000E-05
* RP1ZA  .00000     RP1A =  .00000     RP1B =  .00000
* RP2ZA  .00000     RP2A =  .00000     RP2B =  .00000
* CP1ZA  .00000     CP1A =  .00000     CP1B =  .00000
* CP2ZA  .00000     CP2A =  .00000     CP2B =  .00000
* RSZAC  500.00     RSA =   .50000E+08 RSB =   10000.
* CSZAC  .00000     CSA =   .00000     CSB =   .00000
* RPC =  100.00     RDC =   300.00      CAC =  .22000E-04
* CCOMP  .68000E-07
```

```
 Run #     2

 Z-Filter calculation results
   Reference impedance for optimization:
 ZIRP1= 820.   ZICP1= .000     ZIRP2= 0.  ZICP2= .115E-06
 ZIRS = 220.   ZICS = .000

   Calculated and quantized coefficients:

 XZ  =    -.39571   -.01763    .09355    .03834   -.11305
 XZQ =    -.39063   -.01764    .09351    .03857   -.11328
 Bytes for Z-Filter (13):    B0,1C,25,4C,F1,3E,95,BA

RETURN LOSS

  FREQ        loss                          FREQ        loss
  (Hz)        (dB)                           (Hz)        (dB)
   100.      20.369                         2000.      32.299
   200.      25.997                         2100.      33.062
   300.      28.913                         2200.      33.919
   400.      30.415                         2300.      34.819
   500.      31.014                         2400.      35.642
   600.      31.082                         2500.      36.164
   700.      30.892                         2600.      36.116
   800.      30.612                         2700.      35.400
   900.      30.333                         2800.      34.186
  1000.      30.099                         2900.      32.743
  1100.      29.932                         3000.      31.265
  1200.      29.841                         3100.      29.845
  1300.      29.832                         3200.      28.519
  1400.      29.906                         3300.      27.295
  1500.      30.067                         3400.      26.168
  1600.      30.316                         3500.      25.131
  1700.      30.659                         3600.      24.175
  1800.      31.100                         3700.      23.292
  1900.      31.645                         3800.      22.476

Min. Z-loop reserve:          6.834 dB at frequency:  7500.0 Hz
Min. Z-loop mirror reserve:  10.725 dB at frequency:  7000.0 Hz
Run #    2


X-FILTER calculation results

  Reference impedance for optimization:
ZIRP1=  820.  ZICP1= .000    ZIRP2= 0.  ZICP2= .115E-06
ZIRS =  220.  ZICS = .000

  Calculated and quantized coefficients:

XX  =    1.03178    .03370   -.00468   -.00613    .00014
XXQ =    1.03174    .03369   -.00488   -.00610    .00012
```

```
Bytes for X-Filter (23):    70,E8,AF,FB,1A,45,02,65
X-filter attenuation function (in dB),(always absolute values)
```

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
100.	-.462	.001	2000.	-.320	.001
200.	-.465	.001	2100.	-.285	.001
300.	-.470	.001	2200.	-.250	-.000
400.	-.476	.002	2300.	-.215	-.001
500.	-.482	.002	2400.	-.181	-.002
600.	-.489	.003	2500.	-.149	-.003
700.	-.495	.003	2600.	-.119	-.003
800.	-.501	.003	2700.	-.093	-.004
900.	-.504	.004	2800.	-.069	-.004
1000.	-.505	.004	2900.	-.049	-.004
1100.	-.503	.005	3000.	-.033	-.005
1200.	-.498	.005	3100.	-.020	-.005
1300.	-.488	.005	3200.	-.010	-.005
1400.	-.475	.005	3300.	-.003	-.004
1500.	-.458	.004	3400.	.001	-.004
1600.	-.437	.004	3500.	.004	-.004
1700.	-.412	.004	3600.	.005	-.004
1800.	-.384	.003	3700.	.006	-.003
1900.	-.353	.002	3800.	.006	-.003

```
GX results:
All attenuation values (in dB) refer to FREF =  1014. Hz

 RLX   SLIC+Z   AGX   VREF/VSIC  XREF  TM3       GX
 .00 -  .24  -  .00  -  4.41  -  -.50  -   .00  = -4.33  ideal
 .03 =  .24  +  .00  +  4.41  +  -.50  +   .00  + -4.30  quant

Second byte for Gain:      ,10,32
Calculation of transmit transfer function (AD)
All attenuation values (in dB) refer to FREF = 1014.0 Hz

TGREFCA =    .252 ms      TGREFCB =    .265 ms
```

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
100.	14.050	2.857	2000.	.030	.010
200.	.387	1.873	2100.	.037	.015
300.	.025	.625	2200.	.044	.020
400.	.040	.306	2300.	.050	.027
500.	.035	.175	2400.	.056	.035
600.	.026	.108	2500.	.060	.044
700.	.017	.069	2600.	.063	.055
800.	.009	.044	2700.	.066	.067
900.	.004	.028	2800.	.069	.083
1000.	-.001	.017	2900.	.074	.101
1100.	-.004	.010	3000.	.084	.123

1200.	-.005	.005	3100.	.101	.150
1300.	-.005	.002	3200.	.131	.184
1400.	-.003	.001	3300.	.184	.227
1500.	-.001	.000	3400.	.275	.285
1600.	.004	.000	3500.	.434	.366
1700.	.009	.002	3600.	.726	.486
1800.	.015	.004	3700.	1.327	.682
1900.	.023	.007	3800.	2.793	1.018

Run # 1

R-Filter calculation results
Reference impedance for optimization:
ZIRP1= 820. ZICP1= .000 ZIRP2= 0. ZICP2= .115E-06
ZIRS = 220. ZICS = .000

Calculated and quantized coefficients:

XR =	.82771	-.19100	-.00410	-.00853	.00477
XRQ =	.81250	-.19141	-.00415	-.00854	.00488

Bytes for R-Filter (2B): 70,1A,4F,F1,C9,AA,0C,1B

R-filter attenuation function (in dB),(always absolute values)

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
100.	4.235	-.042	2000.	1.497	.009
200.	4.199	-.041	2100.	1.376	.010
300.	4.139	-.040	2200.	1.261	.010
400.	4.057	-.038	2300.	1.154	.011
500.	3.952	-.035	2400.	1.051	.011
600.	3.828	-.033	2500.	.951	.011
700.	3.685	-.029	2600.	.854	.012
800.	3.527	-.026	2700.	.758	.012
900.	3.356	-.022	2800.	.663	.013
1000.	3.176	-.018	2900.	.568	.014
1100.	2.990	-.014	3000.	.474	.016
1200.	2.801	-.010	3100.	.382	.017
1300.	2.613	-.006	3200.	.292	.019
1400.	2.429	-.002	3300.	.208	.021
1500.	2.251	.001	3400.	.130	.022
1600.	2.081	.003	3500.	.060	.024
1700.	1.920	.005	3600.	-.000	.025
1800.	1.769	.007	3700.	-.049	.027
1900.	1.628	.008	3800.	-.085	.027

GR results:
All attenuation values (in dB) refer to FREF= 1014. Hz

-RLR		SLIC+Z		AGR		VSIC/VREF		RREF		GR	
7.00	-	2.58	-	.00	-	-4.41	-	3.15	=	5.68	ideal
7.00	=	2.58	+	.00	+	-4.41	+	3.15	+	5.68	quant

First byte for Gain (30): 51,32

Calculation of receive transfer function (DA)

All attenuation values (in dB) refer to FREF = 1014.0 Hz

TGREF CA = .198 ms TGREF CB = .181 ms

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
100.	.001	.021	2000.	-.047	.044
200.	.007	.004	2100.	-.038	.050
300.	.012	.001	2200.	-.028	.056
400.	.018	.000	2300.	-.018	.063
500.	.023	.000	2400.	-.009	.072
600.	.026	.000	2500.	-.002	.082
700.	.026	.001	2600.	.002	.093
800.	.023	.002	2700.	.003	.107
900.	.017	.004	2800.	.003	.123
1000.	.007	.006	2900.	.004	.142
1100.	-.004	.009	3000.	.006	.166
1200.	-.017	.012	3100.	.017	.194
1300.	-.029	.015	3200.	.041	.230
1400.	-.041	.019	3300.	.090	.274
1500.	-.050	.022	3400.	.181	.334
1600.	-.056	.026	3500.	.344	.416
1700.	-.059	.030	3600.	.648	.537
1800.	-.058	.034	3700.	1.269	.734
1900.	-.054	.039	3800.	2.763	1.071

Run # 1

B-Filter calculation results

Reference impedance for optimization:

ZLRP1= 820. ZLCP1= .000 ZLRP2= 0. ZLCP2=.115E-06

ZLRS = 220. ZLCS = .000

Calculated and quantized coefficients:

XB =	-.13494	-.33311	-.31893	.00704	.04508
	-.11252	-.01736	.09255	-.09495	.04363
XBQ =	-.13672	-.32813	-.32031	.00696	.04492
	-.11133	-.01733	.09277	-.09570	.04492

2nd part of bytes B-Filter (0B): 00,15,BB,CA,14,ED,B3,BB

1st part of bytes B-Filter (03): 5B,B1,B7,AB,32,2A,B2,14

TRANS HYBRID LOSS

FREQ (Hz)	loss (dB)	FREQ (Hz)	loss (dB)
100.	36.403	2000.	40.457
200.	30.116	2100.	39.753
300.	35.631	2200.	39.660
400.	42.346	2300.	40.188
500.	51.099	2400.	41.450
600.	47.859	2500.	43.748
700.	43.555	2600.	47.934
800.	41.444	2700.	57.305
900.	40.490	2800.	52.729
1000.	40.317	2900.	45.637
1100.	40.812	3000.	42.064
1200.	42.009	3100.	40.071
1300.	44.100	3200.	39.144
1400.	47.594	3300.	39.136
1500.	53.580	3400.	39.925
1600.	54.406	3500.	40.684
1700.	48.018	3600.	39.299
1800.	44.185	3700.	36.517
1900.	41.856	3800.	35.495

Additional B-filter delay (in seconds): .625E-04
Bytes for B-filter delay (18): 19,19,11,19

Appendix E:

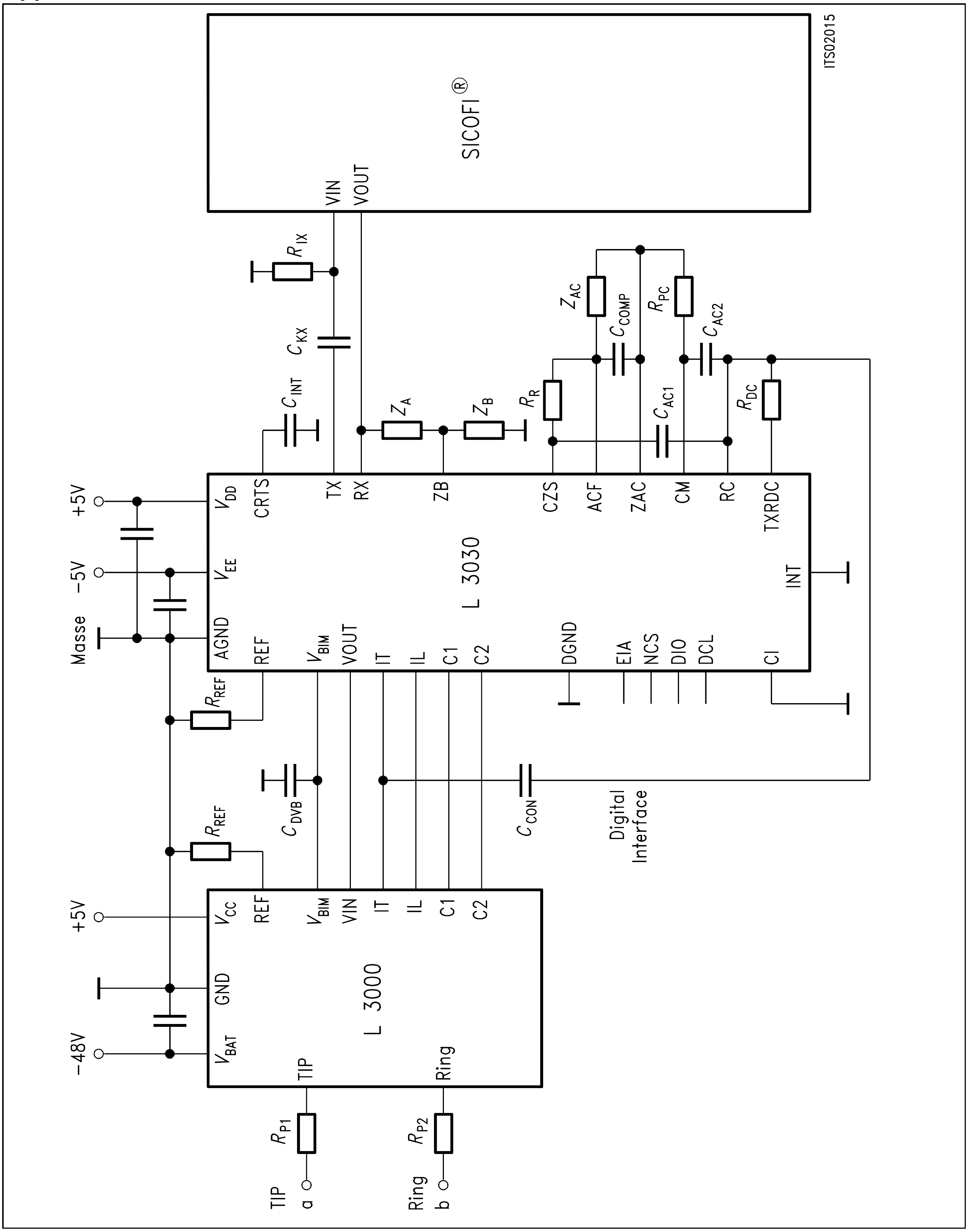


Figure 14

ST-SLIC Circuitry With and Without the Multiplier

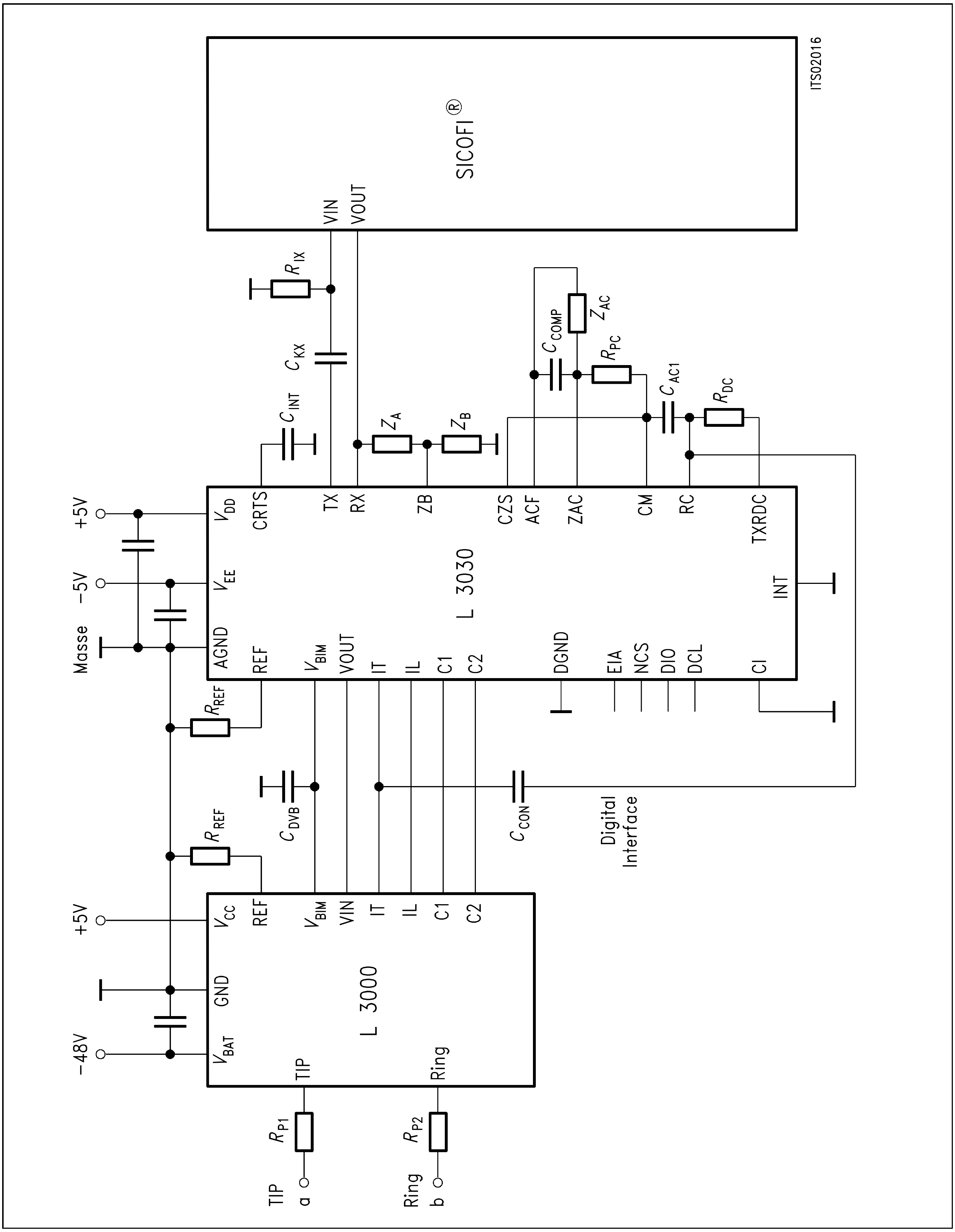


Figure 15
SICOFI® and ST-SLIC Connection Without Multiplier Used

Appendix F:

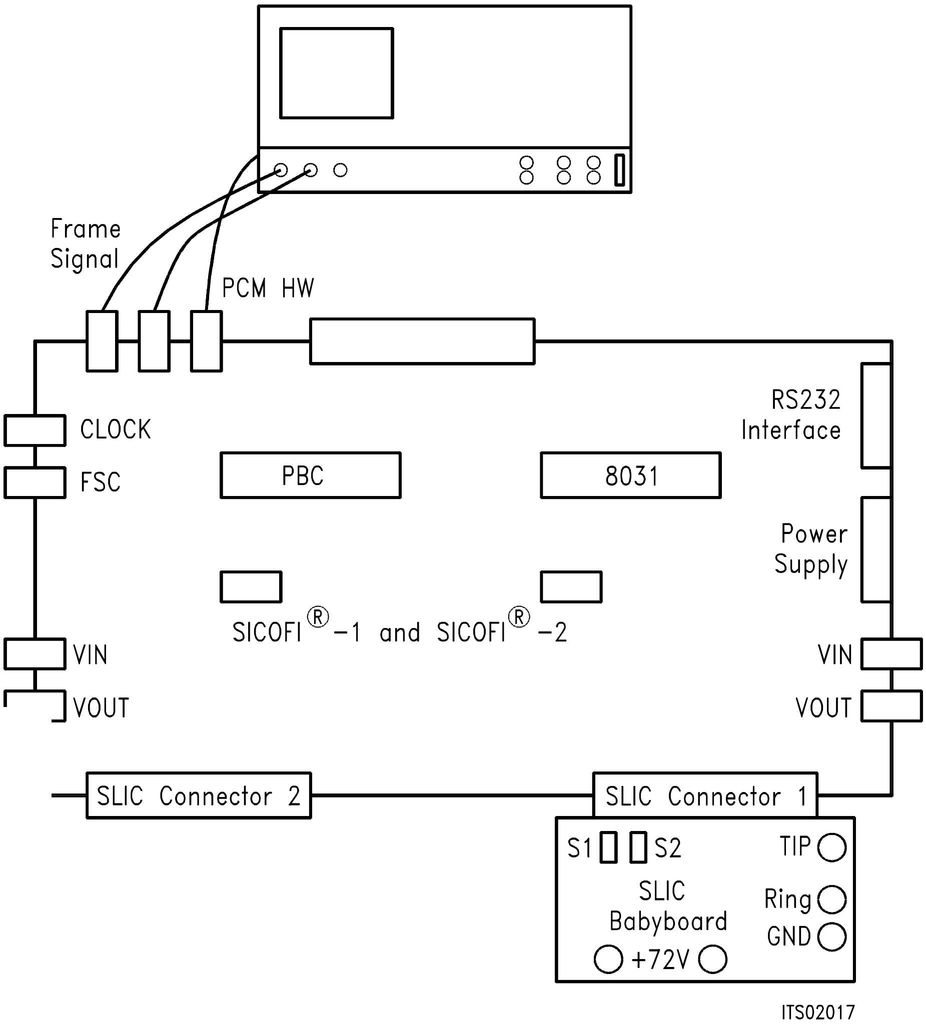


Figure 16
Diagram of the Measurement System

Appendix G:

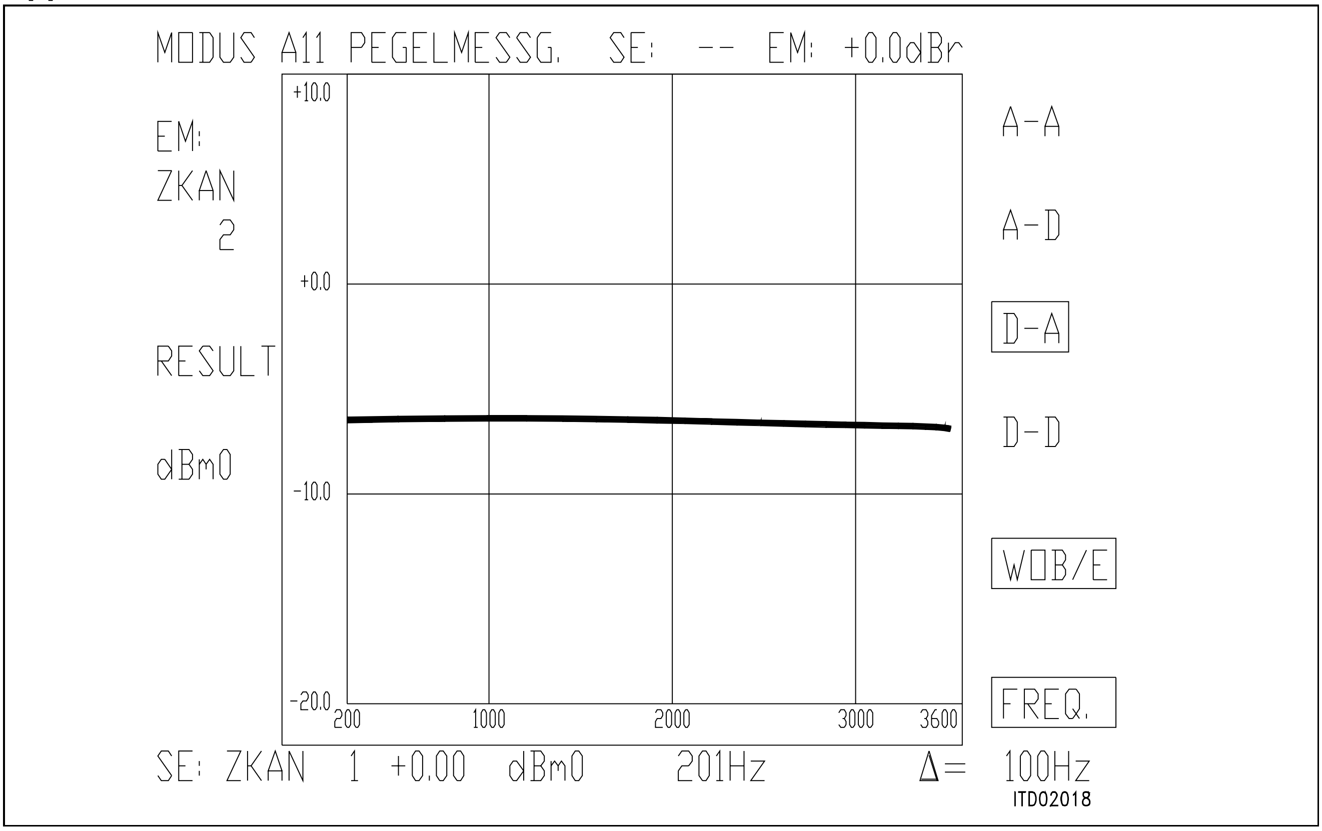


Figure 17

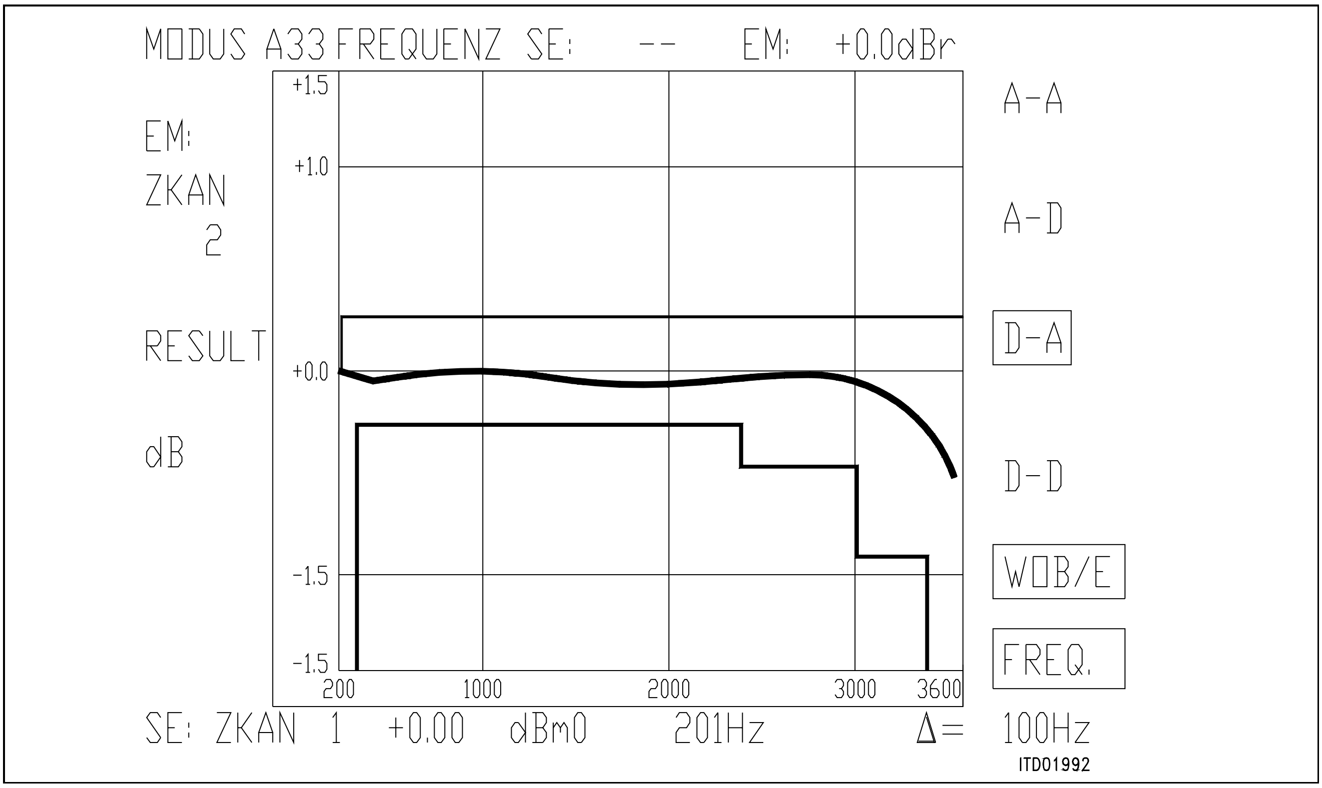


Figure 18

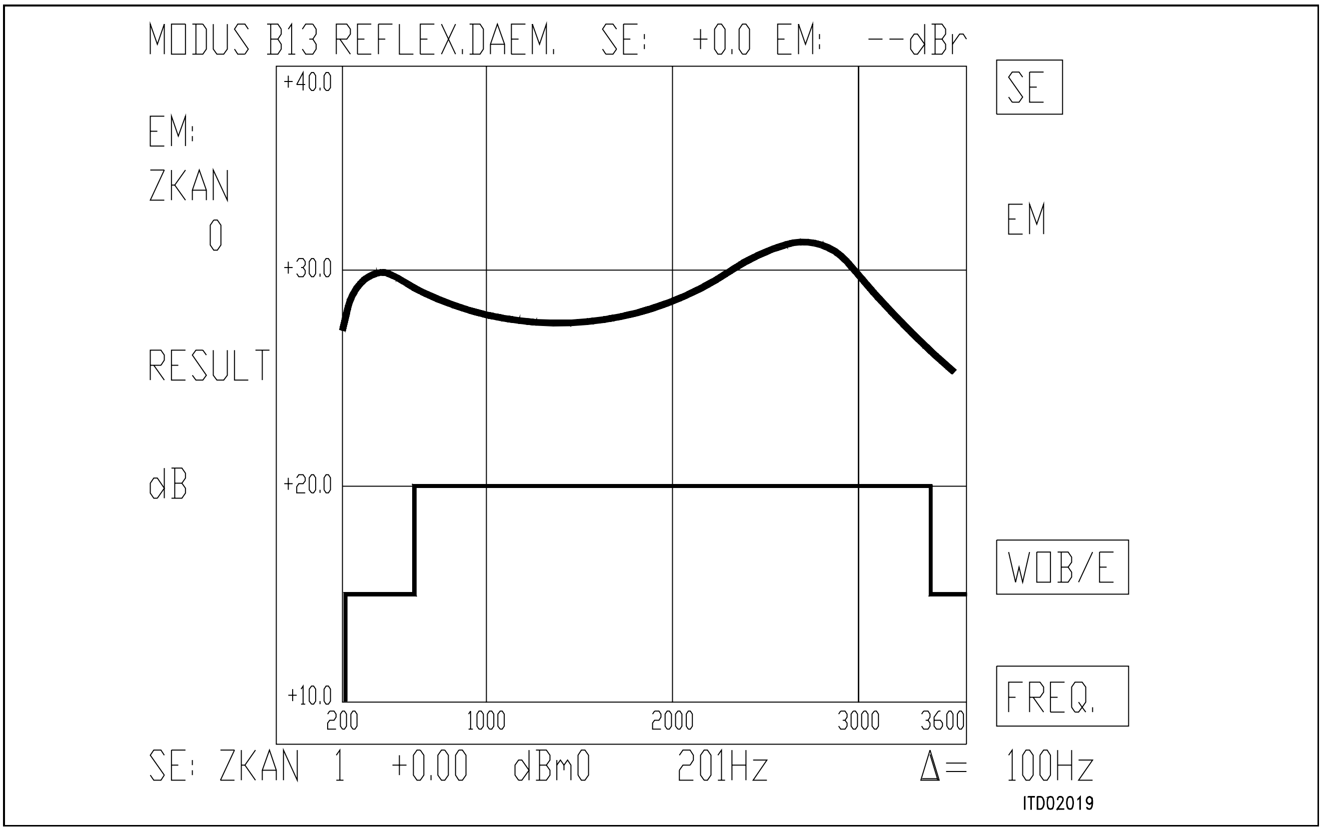


Figure 19

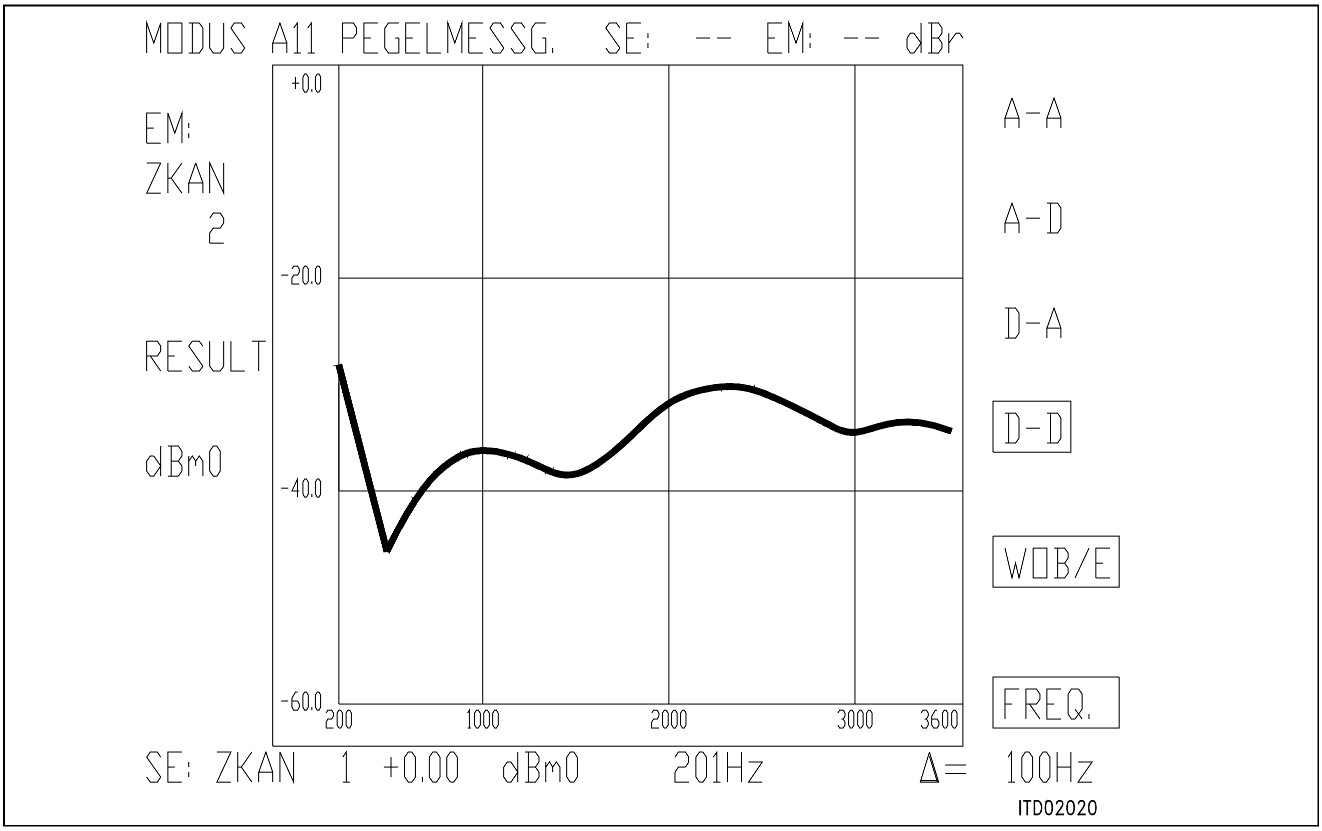


Figure 20

SICOFI® Application Together with STM-SLIC L3000/L3090

Contents **Page**

1 Introduction

This application note describes the combination of a codec filter device (SICOFI) with an electronic SLIC(ST L3090/L3000) as it can be used on a line card for the connection of analog subscribers.

This note consists of:

– A general description of the ST-SLIC L3090/L3000
– A proposal for the interconnection of SICOFI and SLIC
– A description of the model for the SLIC's function
– A listing of FORTRAN program to calculate SLIC transfer function
– Result of calculation and measurements generated for the requirements of the 'Deutsche Bundespost'.

2 Hardware SICOFI® and ST-SLIC L3090/L3000

2.1 ST-SLIC L3090/L3000

The SGS-THOMSON-SLIC (ST L3090/L3000) connects the SICOFI with the a,b lines to the subscriber. It has the following functions:

– Battery feeding
– Hybrid
– Ringing
– Ground key detection
– OFF/ON-hook

The SLIC is divided into two parts, a low voltage part (L3090) and a high voltage part (L3000).

The High Voltage Part
The high voltage part is connected with the line. It realizes the battery feeding through the SLIC and switches the ringing signal and the speech signal in both directions.

An internal temperature detection part switches the line current off, when the temperature gets to high.

The high voltage part is connected to the low voltage part using 6 wires.

The Low Voltage Part
The low voltage part synthesizes the DC characteristic, the AC output impedance performs the echo cancellation. Some of these functions may be realized by the SICOFI and therefore it is possible to reduce the number of external components.

The L3090 has a digital parallel interface with 5 pins. There are two output pins (NGDK and ONHK). These two pins detect ground-key and off-hook. The other three pins are chip select (NCS) and two input pins (PWON and RNG). The input pins can be configured to operate in four modes:

Power-Down The SLIC presents a high impedance to the line and does not supply current.

Standby The SLIC is able to supply current to the line (limited to 12 mA) and to recognize the off-hook condition.

Conversation The SLIC supplies the line and is able to detect both the off-hook and ground key conditions. The DC characteristic shown to the line is divided into two regions:

- current limiting region; the limiting level can be choosen between 4 and 62 mA applying a logical level at pin 24 of L3090 (Note that this pin is not latched by NCS-signal)
- standard feeding region; the characteristic region is equivalent to a voltage generator with a series resistance, the value of which is defind by an external component.

Ringing The SLIC injects a balanced ringing signal to the line with an amplitude of 60 Vrms with a superimposed DC voltage of 22 V. The ringing signal is produced by the battery and a small AC-voltage (1.5 Vrms) at pin 14 of L3090 (connected via a capacitor 1 µF to SICOFI VOUT). The ringing signal starts and stops when the signal crosses zero.

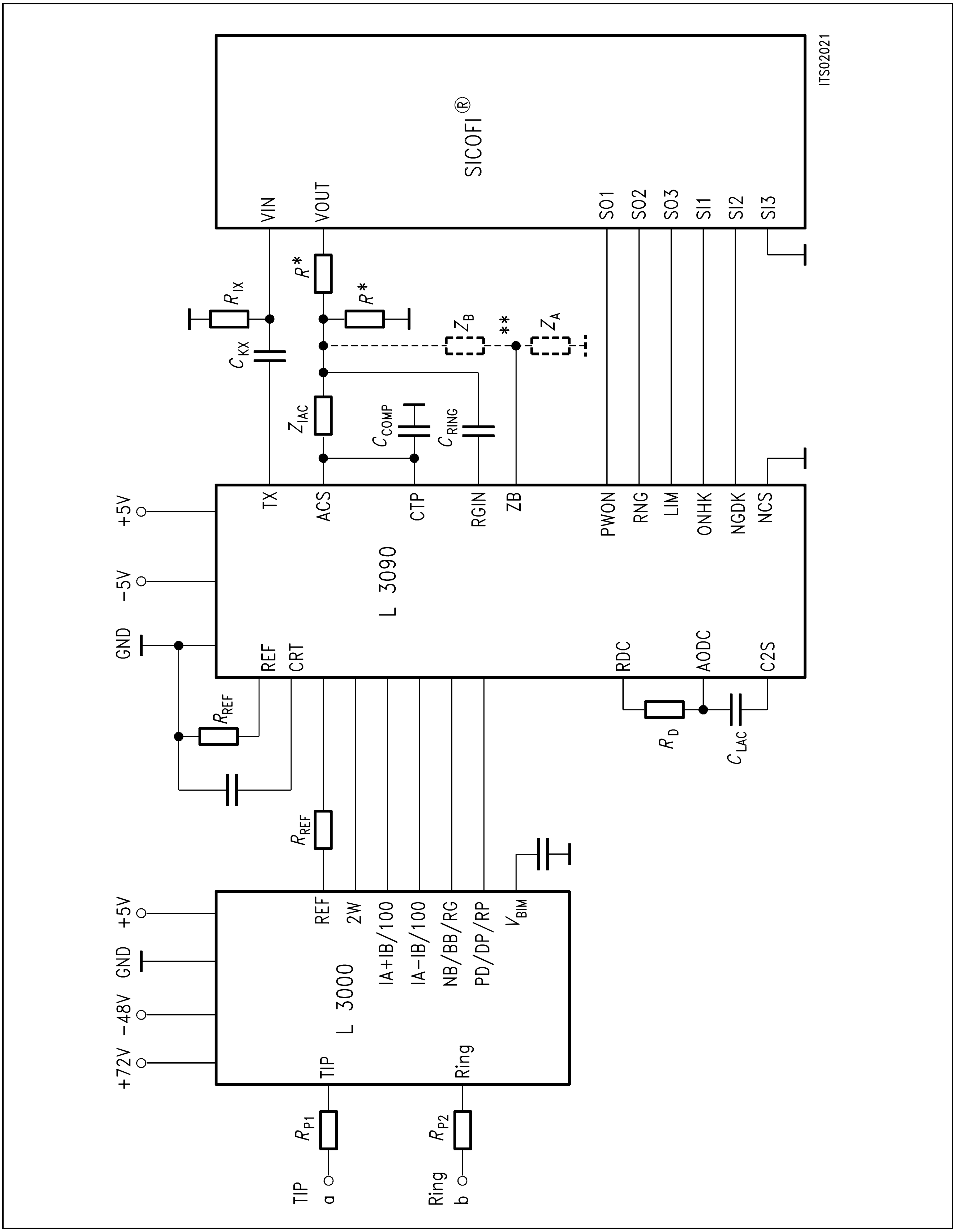


Figure 1

SICOFI® and ST SLIC L3090/L3000

2.2 Programming the PBC, SICOFI® and ST-SLIC L3090/L3000

The ST-SLIC L3090/L3000 can be controlled through the SICOFI (**see figure 1**), setting properly its parallel interface.

For example:

SIG0 = A0 Conversation with I_{lim} = 42 mA
SIG0 = 40 Power down

The line status (off-hook/ground-key) can be read through the SICOFI (**see figure 1**).

For example:

SIG0: 40 off-hook
SIG0: 80 ground-key

2.3 Model of the ST-SLIC L3090/L3000

The ST-SLIC has some external components:

Z_A SLIC impedance balancing network
Z_B line impedance balancing network
Z_{IAC}
C_{LAC} DC feeding system and AC
R_D impedance adjustment
R_{PC}

The value of R_D depends on the DC characteristic region.

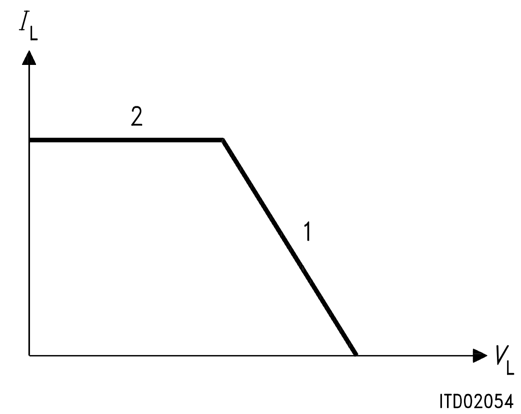


Figure 2

R_D is only used in part 1 infinite in part 2

The value of the impedance R_D has to be written into the input file.

3 Software for ST-SLIC L3090/L3000

3.1 General SLIC-Parameters

To calculate the coefficients we need the mixed matrix parameters:

Objectives:
– Calculation of the mixed matrix parameters using a simplified three port model.

Method:
– A SLIC is a circuit with a number of elements accessible through three ports:

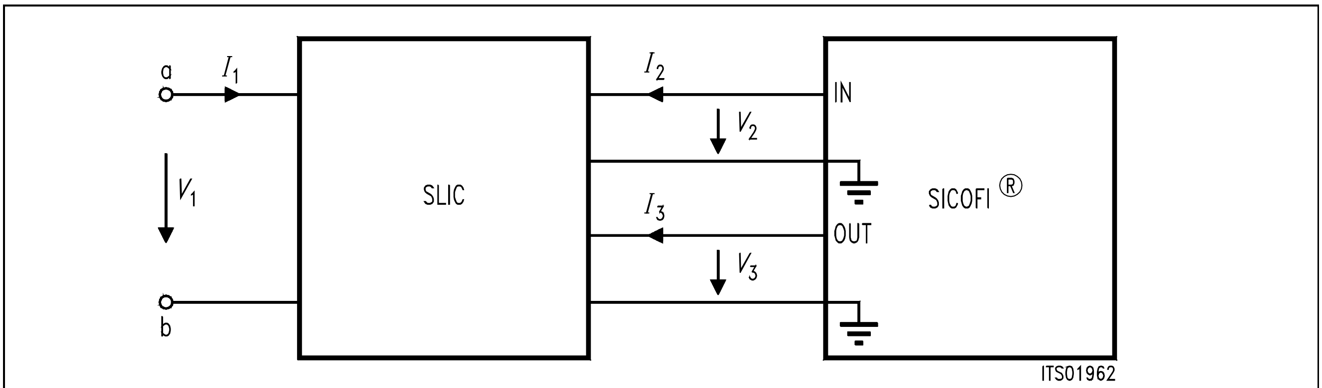
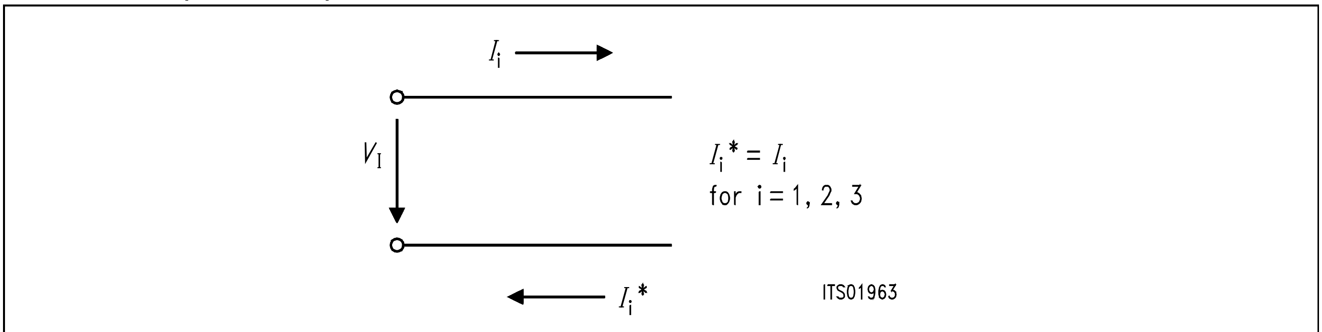


Figure 3

I_1, I_2 and I_3 are port currents
V_1, V_2 and V_3 are port voltages

I_1 = M11 × V_1 + M12 × V_3 + M13 × I_2 (1)
V_2 = M21 × V_1 + M22 × V_3 + M23 × I_2 (2)
I_3 = M31 × V_1 + M32 × V_3 + M33 × I_2 (3)

Note: Description of a port:



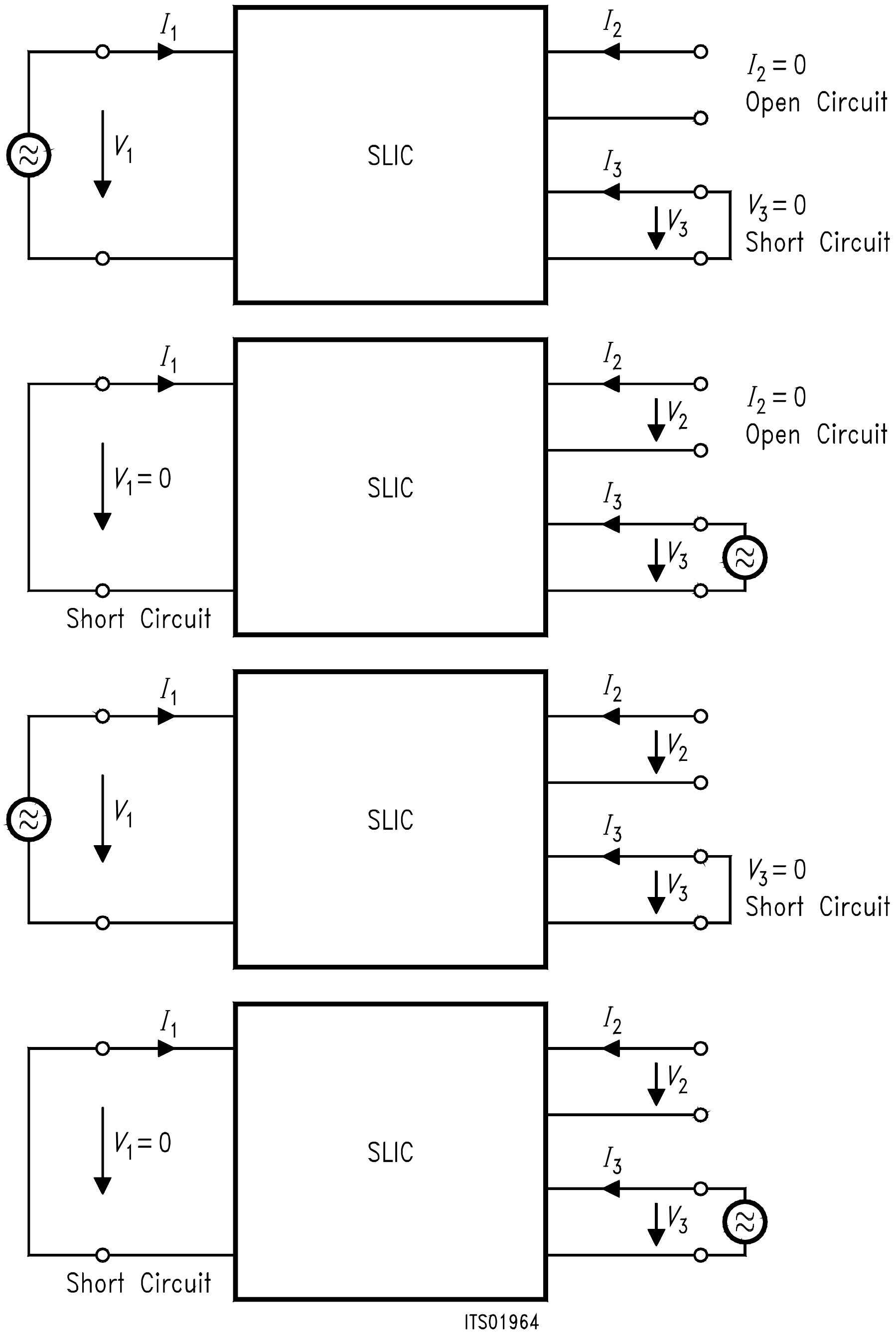
Simplification of the Three Port Model

When the SLIC is connected to the SICOFI, we can assume that:

– I_2 = 0 because the input impedance of SICOFI can be included in the three part model
– I_3 is not relevant in the following calculations because the equation (3) is not used in the SICOFI program.

I_1 = M11 × V_1 + M12 × V_3 (4)
V_2 = M21 × V_1 + M22 × V_3 (5)

The parameters M11, M12, M21 and M22 are determined as follows:



$$M11 = \frac{I_1}{V_1} \text{ for } V_3 = 0 \quad (6)$$

$$M12 = \frac{I_1}{V_3} \text{ for } V_1 = 0 \quad (7)$$

$$M21 = \frac{V_2}{V_1} \text{ for } V_3 = 0 \quad (8)$$

$$M22 = \frac{V_2}{V_3} \text{ for } V_1 = 0 \quad (9)$$

Figure 4

3.2 ST-SLIC Parameter

The mixed matrix parameters are:

Re [M11] (10 – 400 Hz) = $(A + 4 \times \pi \times \pi \times f \times f \times C \times B \times B) / (A \times A + 4 \times \pi \times \pi \times f \times f \times C \times C \times B \times B)$

Re [M11] (400 – 4 kHz) = $(E + 4 \times \pi \times \pi \times f \times f \times D \times D \times R_{PP}) / (E \times E + \$ \times \pi \times \pi \times f \times f \times D \times D \times R_{PP} \times R_{PP})$

Im [M11] (10 – 400 Hz) = $(2 \times \pi \times f \times B \times (A - C)) / (A \times A + 4 \times \pi \times \pi \times f \times f \times C \times C \times B \times B)$

Im [M11] (400 – 4 kHz) = $(2 \times \pi \times f \times D \times (E - R_{PP})) / (E \times E + 4 \times \pi \times \pi \times f \times f \times R_{PP} \times R_{PP} \times D \times D)$

Re [M12] (10 – 4 kHz) = $2 \times (A + 4 \times \pi \times \pi \times f \times f \times C \times B \times B) / (A \times A + \$ \times \pi \times \pi \times f \times f \times C \times C \times B \times B)$

Im [M12] (10 – 4 kHz) = $2 \times (2 \times \pi \times f \times B \times (A - C)) / (A \times A + 4 \times \pi \times \pi \times f \times f \times C \times C \times B \times B)$

Re [M21] (10 – 3 kHz) = $-(4 \times \pi \times \pi \times f \times f \times B \times B \times L \times C) / (A \times A + 4 \times \pi \times \pi \times f \times f \times C \times C \times B \times B)$

Re [M21] (3 – 4 kHz) = $-(L \times E) / (E \times E + 4 \times \pi \times \pi \times f \times f \times H \times H)$

Im [M21] (10 – 3 kHz) = $-(2 \times \pi \times f \times B \times L \times A) / (A \times A + 4 \times \pi \times \pi \times f \times f \times C \times C \times B \times B)$

Im [M21] (3 – 4 kHz) = $(2 \times \pi \times f \times L \times H) / (E \times E + 4 \times \pi \times \pi \times f \times f \times H \times H)$

Re [M22] (10 – 4 kHz) = $2 \times (A \times A + 4 \times \pi \times \pi \times f \times f \times B \times B \times C \times M) / (A \times A + 4 \times \pi \times \pi \times f \times B \times B \times C \times C) - N)$

Im [M22] (10 – 4 kHz) = $2 \times (2 \times \pi \times f \times B \times A \times (M - C)) / (A \times A + 4 \times \pi \times \pi \times f \times f \times B \times B \times C \times C)$

where:

A = $R_D + R_{PP}$

B = $R_D \times C_D$

C = $R_{AC} / 25 + R_{PP}$

D = $(R_{AC} + R_{PC}) \times C_C$

E = $R_{AC} / 25 + R_{PP}$

G = $C_C \times R_{PC}$

H = $C_C \times R_{PP} \times (R_{AC} + R_{PC})$

L = $(R_{AC} + R_{PC}) / 25$

M = $R_{PP} - R_{PC} / 25$

N = $R_A / (R_A + R_B)$

3.3 Calculation

The SLIC has a 0 dB gain in the receive direction and therefore the SICOFI must attenuate the incoming signal in order to match the German specs (GR = – 7 dB). Because of the attenuation being too high (> 12 dB) for the SICOFI, either a voltage divider in receive direction is needed or the AGR of the SICOFI has to be programmed to 6 dB analog attenuation. The SLIC-program is written in FORTRAN and the user may modify this for his own SLIC. The program needs an input file with the values of the external circuit, and then it calculates the mixed matrix parameters and writes them into a SLIC-file. Together with the SICOFI-program you are able to calculate the SICOFI coefficients. It should be noted that the two impedances Z_A and Z_B, used by the SLIC in order to perform the echo cancellation, can be avoided because the SICOFI is able to perform such a function (in this case Z_B is open and Z_A is shorted to ground. In special cases (very high signal levels) it could be necessary to introduce two resistors as Z_A and Z_B to avoid that the TX-SLIC-amplifier saturates (max. TX peak voltage = 3 V).

If you have no Z_A and Z_B than you are not allowed to switch a capacitor between SLIC and SICOFI in the receive direction because the SLIC input need a connection to ground.

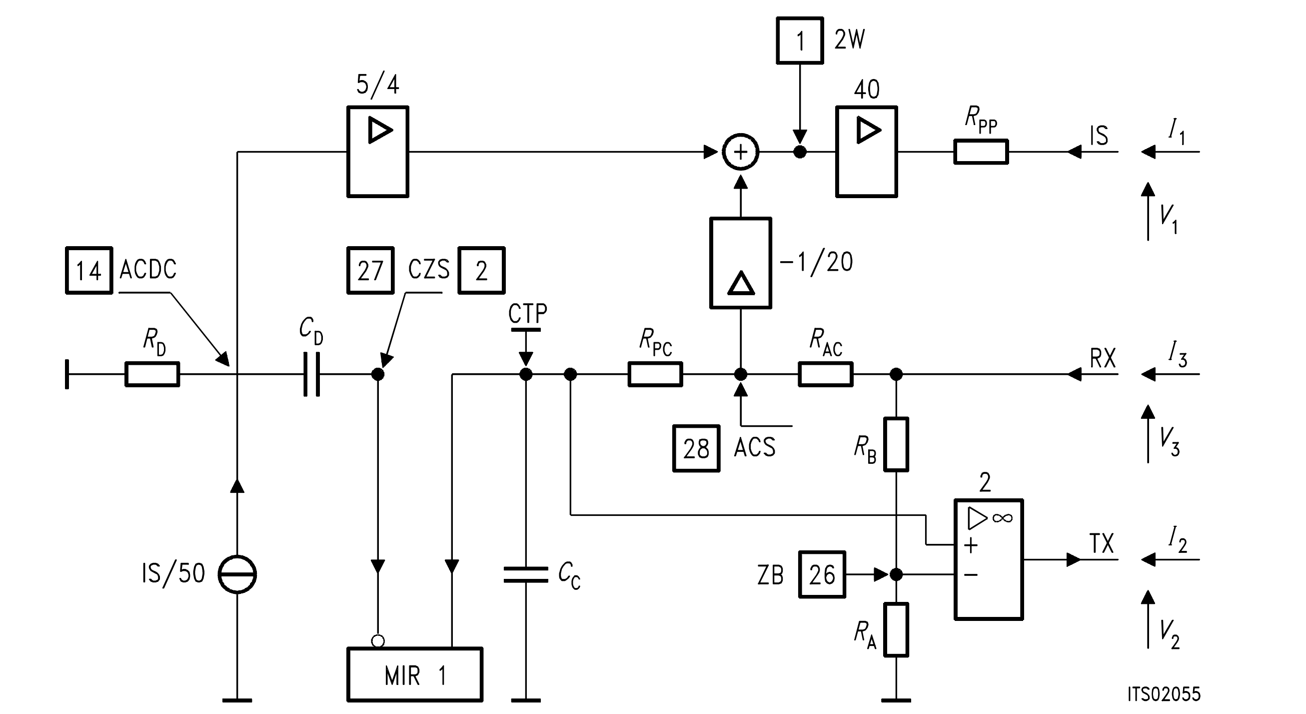


Figure 5
L3090/L3000 Model

Note: For an easier representation some components names were changed in respect to the names on the data sheet; in particular:

R_{PP} correspond to $2 \times R_P$
R_D correspond to R_{DC}
R_{AC} correspond to Z_{IAC}
R_{PC} correspond to R_{PC}
R_A correspond to Z_L
R_B correspond to Z_B
C_D correspond to C_{LAC}
C_C correspond to C_{COMP}

4 Comparison between Calculation and Measurement

The values of the measurement conformed with the calculation. The difference between both are very small (see results of calculation and measurement in the appendix). Only the high attenuation of calculated echo return loss (> 35 dB) cannot be reached by measurement.

5 Appendix

On the next pages you will find the following details:

- SGS-THOMSON-SLIC L3090/L3000 FORTRAN program listing
- Calculated SICOFI-ST-SLIC transfer functions for the ST-SLIC model. The values of the external ST-SLIC components are listed on bottom at page...

Note: R = 300 Ω
Input impedance of SLIC: 34750 Ω parallel with ring input. In this case: V_{OR} = 0.47

- Measured SICOFI-ST-SLIC transfer functions.

Listing of FORTRAN program 'STL 3090.FOR'

```
C**************************** TOP *********************************
C##################################################################
C
      PROGRAM SGS
C     17.05.88  Udo Stueting / Klaus Kliese /Walter Rossi  L 3090
C##################################################################
        IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
*
        INTEGER IN,OUT,I
        CHARACTER*14 BUF1,BUF2*7,BUF3*7,BUF4*7,BUF5*7
        CHARACTER*7 BUF6,BUF7*7,BUF8*7,BUF9*7,BUFF2*12,BUFF3*12
        CHARACTER*7 BUF10*7,BUF11*7,BUF12*7,BUF13*7,BUF14*7,BUF15*7
        CHARACTER*7 BUF16*7
        CHARACTER  BUFF1*12,FILEOUT*12,ANSW*1,INFILE*12
        REAL*8 M11(2),M12(2),M21(2),M22(2),FREQ,AR(2),AX(2)
        REAL*8 VOR,RIR,CKR,VOX,RIX,CKX,PI2,ZSLI
        REAL*8 RPP,RD,RAC,RPC,RA,RB,CD,CC
        REAL*8 NA,NB,NC,ND,NE,NG,NH,NL,NM,NN
*
          COMMON /ARC/ RIR,CKR,VOR
          COMMON /AXC/ RIX,CKX,VOX
          COMMON /NSGSC/ NA,NB,NC,ND,NE,NG,NH,NL,NM,NN
          COMMON /RSGSC/ RPP,RD,RAC,RPC,RA,RB,CD,CC
          COMMON /PI2C/ PI2

C*****************************************************************
C       Initialisation part
C*****************************************************************
C
      DATA BUF1/'* SGS SLIC '/
      DATA BUF2/'* VOR ='/,BUF3/'  RIR ='/,BUF4/'  CKR ='/
      DATA BUF5/'* VOX ='/,BUF6/'  RIX ='/,BUF7/'  CKX ='/
      DATA BUF8/'* RPP ='/,BUF9/' RD ='/BUF10/' RAC ='/
      DATA BUF11/'* RPC ='/,BUF12/' RA ='/BUF13/' RB ='/
      DATA BUF14/'* CD ='/,BUF15/' CC ='/
      DATA BUF16/' ZSLI ='/
*
        OUT = 6
        IN  = 5
        PI2     = 4.*DASIN(1.D0)
        FILEOUT = ' '
            WRITE(OUT,'(A)')
     &     ' Enter input file name(xxxxxxxx.INP):  '
10          READ (IN,'(A)') INFILE
             IF (INDEX(INFILE,' ').EQ.1
```

```
     &         .OR.(INDEX(INFILE,'.INP').EQ.0
     &              .AND.INDEX(INFILE,'.inp').EQ.0)) THEN
                 WRITE (OUT,'(A)') ' Enter correct input file name:  '
                 INFILE=' '
                GOTO 10
             ENDIF
        WRITE (OUT,'(A)') ' Enter output file name (xxxxxxxx.SLI): '
20     READ (IN,'(A)') FILEOUT
        IF (INDEX(FILEOUT,' ').EQ.1) THEN
            WRITE (OUT,' (A)')
     &    ' Enter correct output file name (with extention  .SLI): '
            FILEOUT=' '
            GOTO 20
        ENDIF
        OPEN (30, FILE=FILEOUT, ERR=1000, STATUS= 'UNKNOWN')
             OPEN (10, FILE=INFILE, ERR=1100, STATUS= 'OLD')
             READ(10,'(A)')
             WRITE(6,*) 'Reading input file'
             READ(10,*) VOR
             READ(10,'(A)')
             READ(10,*) RIR
             READ(10,'(A)')
             READ(10,*) CKR
             READ(10,'(A)')
             READ(10,*) VOX
             READ(10,'(A)')
             READ(10,*) RIX
             READ(10,'(A)')
             READ(10,*) CKX
             READ(10,'(A)')
             READ(10,*) RPP
             READ(10,'(A)')
             READ(10,*) RD
             READ(10,'(A)')
             READ(10,*) RAC
             READ(10,'(A)')
             READ(10,*) RPC
             READ(10,'(A)')
             READ(10,*) RA
             READ(10,'(A)')
             READ(10,*) RB
             READ(10,'(A)')
             READ(10,*) CD
             READ(10,'(A)')
             READ(10,*) CC
             READ(10,'(A)')
             READ(10,*) ZSLI
             CLOSE (10)
```

```
C
C*****************************************************************
C      Documentation part
C*****************************************************************
C
        WRITE (30,'(A)') BUF1
        WRITE (BUFF1,'(G12.5)') VOR
        WRITE (BUFF2,'(G12.5)') RIR
        WRITE (BUFF3,'(G12.5)') CKR
        WRITE (30,'(A)') BUF2//BUFF1//BUF3//BUFF2//BUF4//BUFF3
        WRITE (BUFF1,'(G12.5)') VOX
        WRITE (BUFF2,'(G12.5)') RIX
        WRITE (BUFF3,'(G12.5)') CKX
        WRITE (30,'(A)') BUF5//BUFF1//BUF6//BUFF2//BUF7//BUFF3
        WRITE (BUFF1,'(G12.5)') RPP
        WRITE (BUFF2,'(G12.5)') RD
        WRITE (BUFF3,'(G12.5)') RAC
        WRITE (30,'(A)') BUF8//BUFF1//BUF9//BUFF2//BUF10//BUFF3
        WRITE (BUFF1,'(G12.5)') RPC
        WRITE (BUFF2,'(G12.5)') RA
        WRITE (BUFF3,'(G12.5)') RB
        WRITE (30,'(A)') BUF11//BUFF1//BUF12//BUFF2//BUF13//BUFF3
        WRITE (BUFF1,'(G12.5)') CD
        WRITE (BUFF2,'(G12.5)') CC
        WRITE (30,'(A)') BUF14//BUFF1//BUF15//BUFF2
        WRITE (30,'(A)') 'ZSLI'
        WRITE (30,'(G12.5)') ZSLI

C
C****************************************************************
C     Definition L3090
C****************************************************************
C
        NA = RD +RPP
        NB = RD * CD
        NC = (RAC / 25.) + RPP
        ND = (RAC + RPC) * CC
        NE = (RAC / 25) + RPP
        NG =  CC * RPC
        NH = CC * RPP * (RAC + RPC)
        NL = (RAC + RPC) / 25.
        NM = RPP - (RPC/ 25.)
        NN = RA / (RA + RB)
```

```
C
C***************************************************************
C      Calculation part
C***************************************************************
C      L3090
C
        WRITE (OUT,*) ' Running M11 calculation...'
        WRITE (30,'(A)') 'M11-TABLE'
        DO 100 I=1,40
             FREQ = DBLE(I*10)
             CALL PM11L(FREQ,M11)
             WRITE (30,*) FREQ,M11(1),M11(2)
100     CONTINUE
        DO 101 I=41,399
             FREQ = DBLE(I*10)
             CALL PM11H(FREQ,M11)
             WRITE (30,*) FREQ,M11(1),M11(2)
101     CONTINUE
C
C        M12 =
C
        WRITE (OUT,*) ' Running M12 calculation...'
        WRITE (30,'(A)') 'M12-TABLE'
        DO 110 I=1,399
             FREQ = DBLE(I*10)
             CALL ARW(FREQ,AR)
             CALL PM12L(FREQ,M12)
             CALL CMUL(AR,M12,M12)
             WRITE (30,*) FREQ,M12(1),M12(2)
110     CONTINUE
C
C        M21 =
C
        WRITE (OUT,*) ' Running M21 calculation...'
        WRITE (30,'(A)') 'M21-TABLE'
        DO 120 I=1,300
             FREQ = DBLE(I*10)
             CALL AXW(FREQ,AX)
             CALL PM21L(FREQ,M21)
             CALL CMUL(AX,M21,M21)
             WRITE (30,*) FREQ,M21(1),M21(2)
120     CONTINUE
        DO 121 I=301,399
             FREQ = DBLE(I*10)
             CALL AXW(FREQ,AX)
             CALL PM21H(FREQ,M21)
             CALL CMUL(AX,M21,M21)
             WRITE (30,*) FREQ,M21(1),M21(2)
121     CONTINUE
```

```
C
C       M22 =
C
        WRITE (OUT,*) ' Running M22 calculation...'
        WRITE (30,'(A)') 'M22-TABLE'
        DO 130 I=1,399
              FREQ = DBLE(I*10)
              CALL AXW(FREQ,AX)
              CALL ARW(FREQ,AR)
              CALL PM22L(FREQ,M22)
              CALL CMUL(AR,M22,M22)
              CALL CMUL(AX,M22,M22)
              WRITE (30,*) FREQ,M22(1),M22(2)
130     CONTINUE
          WRITE(30,'(A1)') ';'
          CLOSE (30)
        WRITE(OUT,'(A)') ' Data written in file: '//FILEOUT
        STOP
1000    WRITE(OUT,'(A)') ' OPEN ERROR AT OUTPUT-FILE: '//FILEOUT
        STOP 1
1100    WRITE(OUT,'(A)') ' OPEN ERROR AT INPUT-FILE: '//INFILE
          STOP 2
        END
C
C###################################################################
C
      SUBROUTINE ARW(FREQ,AR)
C
C###################################################################
C
C     Name of Subroutine:     ARW
C
C     Formal parameter list:  FREQ,AR
C
C     Input parameters:
C        FREQ    (DOUBLE)
C
C     Output parameters:
C        ARW     (DOUBLE)   ARRAY  2
C
C     Task of this routine: VOR*jwRIR*CKR/(1.+jwRIR*CKR)C
C
C###################################################################
C
          IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
*
          REAL*8 AR(2),FREQ,RIR,CKR,VOR,OMP,PI2,V1(2),V2(2)
*
          COMMON /ARC/ RIR,CKR,VOR
          COMMON /PI2C/ PI2
*
          IF(CKR.EQ.0) THEN
```

```
            AR(1) = 1.
            AR(2) = 0.
          ELSE

           OMP = PI2*FREQ*RIR*CKR
           V1(1) = 0
           V1(2) = OMP
           V2(1) = 1.D0
           V2(2) = OMP
           CALL CDIV(V1,V2,AR)
          END IF
          AR(1) = VOR * AR(1)
          AR(2) = VOR * AR(2)
          RETURN
          END

C
C####################################################################
C
      SUBROUTINE AXW(FREQ,AX)
C
C####################################################################
C
C     Name of Subroutine:     AXW
C
C     Formal parameter list:  FREQ,AX
C
C     Input parameters:
C         FREQ    (DOUBLE)
C
C     Output parameters:
C         AX      (DOUBLE)   ARRAY 2
C
C     Task of this routine:
C
C####################################################################
C
          IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
*
          REAL*8 AX(2),FREQ,RIX,CKX,VOX,OMP,PI2,V1(2),V2(2)
*
          COMMON /AXC/ RIX,CKX,VOX
          COMMON /PI2C/ PI2
*
          IF(CKX.EQ.0) THEN
           AX(1) = 1.
           AX(2) = 0.
          ELSE
           OMP   = PI2*FREQ*RIX*CKX
           V1(1) = 0.
           V1(2) = OMP
           V2(1) = 1.D0
```

```
           V2(2) = OMP
           CALL CDIV(V1,V2,AX)
          END IF
          AX(1) = AX(1)*VOX
          AX(2) = AX(2)*VOX
          RETURN
          END

C
C###################################################################
C
      SUBROUTINE CMUL(C,D,E)
C
C###################################################################
C
C     Name of Subroutine:     CMUL
C
C     Formal parameter list:  C,D,P
C
C     Input parameters:
C         C       (DOUBLE)   ARRAY [2]
C         D       (DOUBLE)   ARRAY [2]
C
C     Output parameters:
C         E       (DOUBLE)   ARRAY [2]
C
C     Task of this routine:
C         SUBROUTINE COMPLEX MULTIPLICATION
C
C###################################################################
C
      IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
*
      REAL*8 C(2),D(2),P(2),E(2)
*
      P(1)=C(1)*D(1)-C(2)*D(2)
      P(2)=C(2)*D(1)+C(1)*D(2)
      E(1)=P(1)
      E(2)=P(2)
      RETURN
      END

C
C###################################################################
C
      SUBROUTINE CDIV(C,D,E)
C
C###################################################################
C
C     Name of Subroutine:     CDIV
C
C     Formal parameter list:  C,D,P
```

```
C
C     Input parameters:
C         C       (DOUBLE)   ARRAY [2]
C         D       (DOUBLE)   ARRAY [2]
C
C     Output parameters:
C         E       (DOUBLE)   ARRAY [2]
C
C     Task of this routine:
C         SUBROUTINE COMPLEX DIVISION
C
C###################################################################
C
      IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
*
      REAL*8 C(2),D(2),P(3),E(2)
*
      P(2)= D(1)*D(1)+D(2)*D(2)
      P(1)= C(1)*D(1)+C(2)*D(2)
      P(3)= C(2)*D(1)-C(1)*D(2)
*
      E(1)=P(1)/P(2)
      E(2)=P(3)/P(2)
      RETURN
      END
C
C###################################################################
C
      SUBROUTINE PM11L(FREQ,M11)
C
C###################################################################
C
C     Name of Subroutine:  PM11L
C
C     Formal parameter list:  FREQ
C
C     Input parameters:  FREQ
C
C     Output parameters:  M11
C
C     Task of this routine:  Re [M11] (10-400Hz)
C                            Im [M11] (10-400Hz)
C
C###################################################################
C
      IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
      REAL*8 PI2,FREQ,M11(2),NA,NB,NC,ND,NE,NG,NH,NL,NM,NN
*
        COMMON /PI2C/ PI2
        COMMON /NSGSC/ NA,NB,NC,ND,NE,NG,NH,NL,NM,NN
*
        M11(1) =(NA + PI2*PI2*FREQ*FREQ*NC*NB*NB) /
```

```
     &                 (NA*NA +PI2*PI2*FREQ*FREQ*NC*NC*NB*NB)
        M11(2) = (PI2*FREQ*NB*(NA-NC)) /
     &                 (NA*NA +PI2*PI2*FREQ*FREQ*NC*NC*NB*NB)
        RETURN
        END

C####################################################################
C
      SUBROUTINE PM11H(FREQ,M11)
C
C####################################################################
C
C     Name of Subroutine:  PM11H
C
C     Formal parameter list:  FREQ
C
C     Input parameters:  FREQ
C
C     Output parameters: M11
C
C     Task of this routine:  Re [M11] (410-3990Hz)
C                            Im [M11] (410-3990Hz)
C
C####################################################################
C
      IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
      REAL*8 PI2,FREQ,M11(2),NA,NB,NC,ND,NE,NG,NH,NL,NM,NN
      REAL*8 RPP,RD,RAC,RPC,RA,RB,CD,CC
*
        COMMON /PI2C/ PI2
        COMMON /NSGSC/ NA,NB,NC,ND,NE,NG,NH,NL,NM,NN
        COMMON /RSGSC/ RPP,RD,RAC,RPC,RA,RB,CD,CC

*
        M11(1) =(NE + PI2*PI2*FREQ*FREQ*ND*ND+RPP) /
     &                 (NE*NE +PI2*PI2*FREQ*FREQ*RPP*RPP*ND*ND)
        M11(2) = (PI2*FREQ*ND*(NE-RPP)) /
     &                 (NE*NE +PI2*PI2*FREQ*FREQ*RPP*RPP*ND*ND)
        RETURN
        END

C####################################################################
C
      SUBROUTINE PM12HL(FREQ,M12)
C
C####################################################################
C
C     Name of Subroutine:  PM12HL
C
C     Formal parameter list:  FREQ
C
C     Input parameters:  FREQ
C
```

```
C     Output parameters:  M12
C
C     Task of this routine:  Re [M12] (10-3990Hz)
C                            Im [M12] (10-3990Hz)
C
C####################################################################
C
      IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
      REAL*8 PI2,FREQ,M12(2),NA,NB,NC,ND,NE,NG,NH,NL,NM,NN
*
        COMMON /PI2C/ PI2
        COMMON /NSGSC/ NA,NB,NC,ND,NE,NG,NH,NL,NM,NN
*
        M12(1) = 2. * (NA + PI2*PI2*FREQ*FREQ*NC*NB*NB) /
     &                 (NA*NA +PI2*PI2*FREQ*FREQ*NC*NC*NB*NB)
        M12(2) = 2. * (PI2*FREQ*NB*(NA-NC)) /
     &                 (NA*NA +PI2*PI2*FREQ*FREQ*NC*NC*NB*NB)
        RETURN
        END

C####################################################################
C
      SUBROUTINE PM12H(FREQ,M12)
C
C####################################################################
C
C     Name of Subroutine:  PM12H
C
C     Formal parameter list:  FREQ
C
C     Input parameters:  FREQ
C
C     Output parameters:  M12
C
C     Task of this routine:  not used
C
C
C####################################################################
C
      IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
      REAL*8 PI2,FREQ,M12(2),NA,NB,NC,ND,NE,NG,NH,NL,NM,NN
      REAL*8 RPP,RD,RAC,RPC,RA,RB,CD,CC
*
        COMMON /PI2C/ PI2
        COMMON /NSGSC/ NA,NB,NC,ND,NE,NG,NH,NL,NM,NN
        COMMON /RSGSC/ RPP,RD,RAC,RPC,RA,RB,CD,CC

*
        M12(1) = 2. * (NE + PI2*PI2*FREQ*FREQ*NH*NG) /
     &                 (NE*NE +PI2*PI2*FREQ*FREQ*NH*NH)
        M12(2) = 2. * (PI2*FREQ*(NH-(NE*NG))) /
     &                 (NE*NE +PI2*PI2*FREQ*FREQ*NH*NH)
        RETURN
        END
```

```
C######################################################################
C
      SUBROUTINE PM21L(FREQ,M21)
C
C######################################################################
C
C     Name of Subroutine:  PM21L
C
C     Formal parameter list:  FREQ
C
C     Input parameters:  FREQ
C
C     Output parameters:  M21
C
C     Task of this routine:  Re [M21] (10-3000Hz)
C                            Im [M21] (10-3000Hz)
C
C######################################################################
C
      IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
      REAL*8 PI2,FREQ,M21(2),NA,NB,NC,ND,NE,NG,NH,NL,NM,NN
*
        COMMON /PI2C/ PI2
        COMMON /NSGSC/ NA,NB,NC,ND,NE,NG,NH,NL,NM,NN
*
        M21(1) = - (PI2*PI2*FREQ*FREQ*NB*NB*NL*NC) /
     &                 (NA*NA +PI2*PI2*FREQ*FREQ*NC*NC*NB*NB)
        M21(2) = - (PI2*FREQ*NB*NL*NA) /
     &                 (NA*NA +PI2*PI2*FREQ*FREQ*NC*NC*NB*NB)
        RETURN
        END
```

```
C###################################################################
C
      SUBROUTINE PM21H(FREQ,M21)
C
C###################################################################
C
C     Name of Subroutine:  PM21H
C
C     Formal parameter list:  FREQ
C
C     Input parameters:  FREQ
C
C     Output parameters:  M21
C
C     Task of this routine:  Re [M21] (3010-3990Hz)
C                            Im [M21] (3010-3990Hz)
C
C###################################################################
C
      IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
      REAL*8 PI2,FREQ,M21(2),NA,NB,NC,ND,NE,NG,NH,NL,NM,NN
      REAL*8 RPP,RD,RAC,RPC,RA,RB,CD,CC
*
        COMMON /PI2C/ PI2
        COMMON /NSGSC/ NA,NB,NC,ND,NE,NG,NH,NL,NM,NN
        COMMON /RSGSC/ RPP,RD,RAC,RPC,RA,RB,CD,CC

*
        M21(1) = - (NL * NE) /
     &                 (NE*NE +PI2*PI2*FREQ*FREQ*NH*NH)
        M21(2) = (PI2*FREQ*NL*NH) /
     &                 (NE*NE +PI2*PI2*FREQ*FREQ*NH*NH)
        RETURN
        END

C###################################################################
C
      SUBROUTINE PM22L(FREQ,M22)
C
C###################################################################
C
C     Name of Subroutine:  PM22L
C
C     Formal parameter list:  FREQ
C
C     Input parameters:  FREQ
C
C     Output parameters:  M22
C
C     Task of this routine:  Re [M22] (10-3990Hz)
C                            Im [M22] (10-3990Hz)
C
```

```
C######################################################################
C
      IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
      REAL*8 PI2,FREQ,M22(2),NA,NB,NC,ND,NE,NG,NH,NL,NM,NN
*
        COMMON /PI2C/ PI2
        COMMON /NSGSC/ NA,NB,NC,ND,NE,NG,NH,NL,NM,NN
*
        M22(1) = (-2.*NN)+2.*((NA*NA*PI2*PI2*FREQ*FREQ*NB*NB*NC*NM)/
     &                   (NA*NA+PI2*PI2*FREQ*FREQ*NC*NC*NB*NB))
        M22(2) = 2. * (PI2*FREQ*NB*NA*(NM-NC)) /
     &                   (NA*NA +PI2*PI2*FREQ*FREQ*NC*NC*NB*NB)
       RETURN
       END

C######################################################################
C
      SUBROUTINE PM22H(FREQ,M22)
C
C######################################################################
C
C     Name of Subroutine:  PM22H
C
C     Formal parameter list:  FREQ
C
C     Input parameters:  FREQ
C
C     Output parameters:  M22
C
C     Task of this routine:  not used
C
C
C######################################################################
C
      IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
      REAL*8 PI2,FREQ,M22(2),NA,NB,NC,ND,NE,NG,NH,NL,NM,NN
      REAL*8 RPP,RD,RAC,RPC,RA,RB,CD,CC
*
        COMMON /PI2C/ PI2
        COMMON /NSGSC/ NA,NB,NC,ND,NE,NG,NH,NL,NM,NN
        COMMON /RSGSC/ RPP,RD,RAC,RPC,RA,RB,CD,CC

*
        M22(1) = (-2.*NN) + 2. * (NM*NC) /
     &                   (NC*NC +PI2*PI2*FREQ*FREQ*NH*NH)
        M22(2) = 2. *(PI2*FREQ*NM*NH) /
     &                   (NC*NC +PI2*PI2*FREQ*FREQ*NH*NH)
        RETURN
        END
```

```
C######################################################################
C
      SUBROUTINE IMPED1(RSER,RPAR,CSER,CPAR,FREQ,ZI)
C
C######################################################################
C
C     Name of Subroutine:     IMPED1
C
C     Formal parameter list:  RSER,RPAR,CSER,CPAR,FREQ,ZI
C
C     Input parameters:
C         RSER   (DOUBLE)   ; series resistance
C         RPAR   (DOUBLE)   ; parallel resistance
C         CSER   (DOUBLE)   ; series capacitance
C         CPAR   (DOUBLE)   ; parallel capacitance
C         FREQ   (DOUBLE)   ; frequency
C
C     Output parameters:
C         ZI     (DOUBLE)   ARRAY [2]
C
C  Task of this routine:  CALCULATION OF COMPLEX IMPEDANCE
C
C######################################################################
C
      IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
*
      REAL*8 V1(2),V2(2)ZI(2)CSER,CPAR,FREQ,PI2,RPAR,RSER
*
      COMMON /QP2/ PI2
*
      V1(1) = 1.D0
      V1(2) = PI2*FREQ*CPAR*RPAR
      V2(1) = RPAR
      V2(2) = 0.
      CALL CDIV(V2,V1,ZI)
      ZI(1) = ZI(1)+RSER
      ZI(2) = ZI(2)+0.
      RETURN
      END

C######################################################################
C
      SUBROUTINE IMPED2(RSER,RPAR,CSER,CPAR,FREQ,ZI)
C
C######################################################################
C
C     Name of Subroutine:     IMPED2
C
C     Formal parameter list:  RSER,RPAR,CSER,CPAR,FREQ,ZI
C
C     Input parameters:
C         RSER   (DOUBLE)   ; series resistance
```

```
C         RPAR   (DOUBLE)   ; parallel resistance
C         CSER   (DOUBLE)   ; series capacitance
C         CPAR   (DOUBLE)   ; parallel capacitance
C         FREQ   (DOUBLE)   ; frequency
C
C     Output parameters:
C         ZI     (DOUBLE)   ARRAY [2]
C
C  Task of this routine:  CALCULATION OF COMPLEX IMPEDANCE
C
C###################################################################
C
      IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
*
      REAL*8 V1(2),V2(2),ZI(2),CSER,CPAR,FREQ,PI2,RPAR,RSER,C(2)
      REAL*8 OMEGA
*
      COMMON /QP2/ PI2
*
      OMEGA = PI2*FREQ
      V1(1) = 1.D0
      V1(2) = OMEGA*CPAR*RPAR
      V2(1) = RPAR
      V2(2) = 0.
      CALL CDIV(V2,V1,ZI)
      V2(1) = 0.
      V2(2) = OMEGA*CSER
      V1(1) = 1.D0
      V1(2) = V2(2)*RSER
      CALL CDIV(V1,V2,C)
      ZI(1)=ZI(1)+C(1)
      ZI(2)=ZI(2)+C(2)
      RETURN
      END


C###################################################################
C
      SUBROUTINE IMPED3(RSER,RPAR,CSER,CPAR,FREQ,ZL)
C
C###################################################################
C
C     Name of Subroutine:     IMPED3
C
C     Formal parameter list:  RSER,RPAR,CSER,CPAR,FREQ,ZI
C
C     Input parameters:
C         RSER   (DOUBLE)   ; series resistance
C         RPAR   (DOUBLE)   ; parallel resistance
C         CSER   (DOUBLE)   ; series capacitance
C         CPAR   (DOUBLE)   ; parallel capacitance
C         FREQ   (DOUBLE)   ; frequency
```

```
C
C     Output parameters:
C         ZI     (DOUBLE)   ARRAY [2]
C
C  Task of this routine:  CALCULATION OF COMPLEX IMPEDANCE
C
C####################################################################
C
      IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
*
      REAL*8 ZL(2),CSER,CPAR,FREQ,RPAR,RSER,PI2,OMEGA,A(2),B(2)
*
      COMMON  /QP2/ PI2
*
      OMEGA = PI2*FREQ
      IF (RPAR.EQ.0) THEN
          A(1) = 1.D0
          A(2) = OMEGA*CSER*RSER
          B(1) = 0
          B(2) = OMEGA*CSER
          CALL CDIV(A,B,ZL)
      ELSE
          A(1) = RPAR
          A(2) = OMEGA*CSER*RSER*RPAR
          B(1) = 1.D0
          B(2) = OMEGA*CSER*(RSER+RPAR)
          CALL CDIV(A,B,ZL)
      END IF
      RETURN
      END
```

Listing of SICOFI® Result File 'STL 3090.RES'

```
Input_file_name: L3090.CTL              Date: 20.05.88  11:25
SPEC = L3090.SPE                            SLIC = L3090.SLI
BYTE = L3090.BYT    CHNR = 0,A
PLQ  = N
ON = ALL                    REL  =  Y                   SHORT = N
OPT =  Z+X+R+B              ZXRB =  NNNN
   FZ =  300.00       3400.0       ZLIM =  2.00
ZREP  =Y                         ZSIGN =  1
  FR =   400.00       3300.0
RFIL =  Y             RREFQ = N       RREF =  5.6550
  FX =   400.00       3300.0
XFIL =  Y             XREFQ = N       XREF =-0.76499E-01
  FB =   300.00       3400.0       BLIM =  2.00 TBM =  1
BREP = N                         BSIGN =  1
```

```
APOF =  0.10     DPOF =  0.00E+00 APRE =  0.00E+00 DPRE =  0.00E+00
XZQ =   0.27734375000000000E+00   0.50000000000000000E+00
        0.44921875000000000E-01  -0.45312500000000000E+00
        0.16406250000000000E+00
XRQ =  0.6875000000 -0.2832031250  0.0654296875 -0.0205078125
0.0039062500

XXQ =  1.0468750000 -0.0527343750  0.0302734375 -0.0019531250
0.0019531250

XBQ =   0.45898437500000000E-01   0.39062500000000000E+00
        0.25976562500000000E+00   0.11523437500000000E+00
        0.72265625000000000E-01
        0.12207031250000000E-01   0.53710937500000000E-02
        0.41015625000000000E-01  -0.30754089355468750E-01
        0.19042968750000000E-01
XGQ =  0.6718750000  1.6562500000

;

Bytes for Z-Filter (13):              30,22,B9,5A,B1,F1,28,B3
Bytes for R-Filter (2B):              40,C8,2E,42,A4,3A,14,12
Bytes for X-Filter (23):              50,C8,8D,5C,9C,BC,02,A4
Bytes for Gain-factors (30):          21,A1,10,22
2nd part of bytes B-Filter (0B):      00,26,DB,6E,25,72,2A,A6
1st part of bytes B-Filter (03):      4B,23,C3,22,25,A1,5B,C1
Bytes for B-Filter delay (18):        19,19,11,19

* SGS SLIC
* VOR = 0.47000      RIR =  34750.      CKR = 0.00000E+00
* VOX =  1.0000      RIX = 0.10000E+06  CKX = 0.22000E-04
* RPP =  60.000     RD =    750.00     RAC =   13500.
* RPC = 0.00000E+00 RA =   0.00000E+00 RB =   0.10000E+11
* CD =  0.23500E-04 CC =   0.33000E-09
```

```
Run #    1

Z-FILTER calculation results
  Generator impedance  ZI at a,b line!
  Calculated and quantized coefficients:

XZ  =    0.27720   0.49984   0.04498  -0.45004   0.16550
XZQ =    0.27734   0.50000   0.04492  -0.45312   0.16406
Bytes for Z-Filter (13):    30,22,B9,5A,B1,F1,28,B3

RETURN LOSS

  FREQ        loss                          FREQ       loss
  (Hz)        (dB)                          (Hz)       (dB)
   100.      26.962                         1800.     25.069
   200.      26.741                         1900.     25.314
   300.      26.271                         2000.     25.599
   400.      25.716                         2100.     25.919
   500.      25.724                         2200.     26.267
   600.      25.483                         2300.     26.631
   700.      25.247                         2400.     26.993
   800.      25.031                         2500.     27.330
   900.      24.845                         2600.     27.607
  1000.      24.696                         2700.     27.786
  1100.      24.588                         2800.     27.829
  1200.      24.523                         2900.     27.705
  1300.      24.501                         3000.     27.405
  1400.      24.525                         3100.     26.821
  1500.      24.594                         3200.     26.159
  1600.      24.708                         3300.     25.427
  1700.      24.866                         3400.     24.657

Min. Z-loop reserve:      1.443 dB
       at frequency:     7000.0 Hz
Min. Z-loop mirror signal reserve:      5.092 dB
                     at frequency:     6500.0 Hz


Warning! SICOFI specs (noise, gain tracking ...) not guaranteed
Increase SLIC attenuation in receive path at least by      1.13 dB
Run #    1

X-FILTER calculation results
  Calculated and quantized coefficients:

XX  =    1.03976  -0.05284   0.03052  -0.00288   0.00233
XXQ =    1.04687  -0.05273   0.03027  -0.00195   0.00195
Bytes for X-Filter (23):    50,C8,8D,5C,9C,BC,02,A4
X-filter attenuation function (in dB), (always absolute values)
```

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
300.	-0.191	0.000	1900.	-0.140	-0.007
400.	-0.178	0.000	2000.	-0.170	-0.006
500.	-0.162	-0.001	2100.	-0.206	-0.006
600.	-0.144	-0.002	2200.	-0.246	-0.005
700.	-0.126	-0.003	2300.	-0.290	-0.004
800.	-0.109	-0.004	2400.	-0.338	-0.004
900.	-0.092	-0.004	2500.	-0.391	-0.003
1000.	-0.078	-0.005	2600.	-0.447	-0.002
1100.	-0.067	-0.006	2700.	-0.506	0.000
1200.	-0.060	-0.006	2800.	-0.567	0.001
1300.	-0.057	-0.007	2900.	-0.630	0.002
1400.	-0.058	-0.007	3000.	-0.693	0.004
1500.	-0.065	-0.007	3100.	-0.755	0.005
1600.	-0.076	-0.007	3200.	-0.816	0.007
1700.	-0.093	-0.007	3300.	-0.874	0.008
1800.	-0.114	-0.007	3400.	-0.927	0.010
1900.	-0.140	-0.007	3500.	0.000	0.000
2000.	-0.170	-0.006	3600.	0.000	1.113

GX results:
All attenuation values (in dB) refer to FREF = 1014. Hz

RLX		SLIC+Z		VREF/VSICOFI		–XREF		GX	
0.00	-	0.03	-	4.42	-	-0.08	=	-4.37	ideal
-0.02	=	0.03	+	4.42	+	-0.08	+	-4.38	quant

Second byte for Gain: ,10,22
Calculation of transmit transfer function (AD)
All attenuation values (in dB) refer to FREF = 1014.0 Hz
Generator impedance ZI at a,b line!

TGREF CA = 0.273 ms TGREF CB = 0.287 ms

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
100.	13.827	2.618	2000.	0.005	0.013
200.	0.316	1.808	2100.	0.002	0.018
300.	-0.022	0.595	2200.	0.000	0.024
400.	-0.002	0.325	2300.	-0.003	0.031
500.	-0.005	0.170	2400.	-0.005	0.039
600.	0.002	0.105	2500.	-0.006	0.049
700.	0.000	0.067	2600.	-0.005	0.060
800.	0.000	0.043	2700.	-0.002	0.073
900.	0.002	0.027	2800.	0.004	0.089
1000.	0.004	0.017	2900.	0.016	0.107
1100.	0.007	0.009	3000.	0.037	0.307
1200.	0.009	0.005	3100.	0.093	0.157
1300.	0.011	0.002	3200.	0.142	0.191
1400.	0.013	0.000	3300.	0.218	0.234
1500.	0.013	0.000	3400.	0.336	0.291
1600.	0.012	0.001	3500.	0.525	0.371
1700.	0.011	0.003	3600.	0.853	0.491
1800.	0.010	0.005	3700.	1.493	1.022
1900.	0.007	0.009	3800.	3.002	1.022

Run # 1

R-FILTER calculation results
Calculated and quantized coefficients:

```
XR  =    0.68422  -0.28458   0.06639  -0.01965   0.00512
XRQ =    0.68750  -0.28320   0.06543  -0.02051   0.00391
Bytes for R-Filter (2B):    40,C8,2E,42,A4,3A,14,12
```

R-filter attenuation function (in dB), (always absolute values)

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
300.	6.755	-0.052	1900.	3.612	-0.006
400.	6.662	-0.050	2000.	3.364	-0.004
500.	6.546	-0.048	2100.	3.112	-0.001
600.	6.408	-0.045	2200.	2.855	0.002
700.	6.251	-0.042	2300.	2.594	0.005
800.	6.075	-0.039	2400.	2.331	0.009
900.	5.886	-0.035	2500.	2.065	0.013
1000.	5.684	-0.032	2600.	1.799	0.017
1100.	5.473	-0.028	2700.	1.536	0.021
1200.	5.254	-0.025	2800.	1.278	0.026
1300.	5.030	-0.022	2900.	1.027	0.030
1400.	4.801	-0.019	3000.	0.787	0.034
1500.	4.569	-0.016	3100.	0.560	0.038
1600.	4.335	-0.014	3200.	0.349	0.042
1700.	4.097	-0.011	3300.	0.157	0.046
1800.	3.857	-0.009	3400.	-0.014	0.049
1900.	3.612	-0.006	3500.	-0.052	0.000
2000.	3.364	-0.004	3600.	-0.050	1.002

GR results:
All attenuation values (in dB) refer to FREF= 1014. Hz

```
   -RLR    SLIC+Z    VSICOFI/VREF    RREF          GR
   7.00 -   2.28  -      -4.42    -   5.65    =      3.48  ideal
   6.98 =   2.28  +      -4.42    +   5.65    +      3.45  quant
```

First byte for Gain (30): 21,A1
Calculation of receive transfer function (DA)
All attenuation values (in dB) refer to FREF = 1014.0 Hz
Terminating impedance ZI at a,b line!

TGREF CA = 0.223 ms TGREF CB = 0.205 ms

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
100.	0.049	0.000	2000.	0.083	0.069
200.	0.050	0.014	2100.	0.088	0.075
300.	0.042	0.017	2200.	0.089	0.083
400.	0.031	0.055	2300.	0.086	0.092

500.	0.029	0.026	2400.	0.081	0.102
600.	0.023	0.027	2500.	0.075	0.114
700.	0.017	0.028	2600.	0.069	0.127
800.	0.012	0.030	2700.	0.066	0.143
900.	0.008	0.032	2800.	0.070	0.160
1000.	0.005	0.034	2900.	0.084	0.181
1100.	0.005	0.036	3000.	0.112	0.184
1200.	0.007	0.039	3100.	0.185	0.234
1300.	0.012	0.041	3200.	0.260	0.270
1400.	0.019	0.044	3300.	0.374	0.315
1500.	0.029	0.047	3400.	0.541	0.373
1600.	0.041	0.050	3500.	0.794	0.454
1700.	0.053	0.054	3600.	1.199	0.575
1800.	0.065	0.058	3700.	1.931	0.770
1900.	0.075	0.063	3800.	3.545	1.106

```
Run #     1

B-FILTER calculation results
  Terminating impedance ZL at a,b line!

Calculated and quantized coefficients:

XB  =    0.04525   0.39813   0.25930   0.11590   0.07329
         0.01268   0.00503   0.04196  -0.03075   0.01917
XBQ =    0.04590   0.39062   0.25977   0.11523   0.07227
         0.01221   0.00537   0.04102  -0.03075   0.01904
2nd part of bytes B-Filter (0B):    00,26,DB,6E,25,72,2A,A6
1st part of bytes B-Filter (03):    4B,23,C3,22,25,A1,5B,C1
```

TRANS HYBRID LOSS

FREQ (Hz)	loss (dB)	FREQ (Hz)	loss (dB)
100.	43.346	1800.	46.773
200.	37.367	1900.	47.239
300.	43.283	2000.	46.862
400.	47.865	2100.	45.857
500.	47.354	2200.	44.669
600.	46.009	2300.	43.587
700.	44.625	2400.	42.735
800.	43.525	2500.	42.148
900.	42.736	2600.	41.833
1000.	42.233	2700.	41.784
1100.	41.998	2800.	41.989
1200.	42.018	2900.	42.404
1300.	42.292	3000.	42.903
1400.	42.821	3100.	49.840
1500.	43.604	3200.	50.346
1600.	44.613	3300.	47.987
1700.	45.754	3400.	44.041

```
Additional B-filter delay (in seconds):  .625E-04
Bytes for B-filter delay (18):  19,19,11,19
```

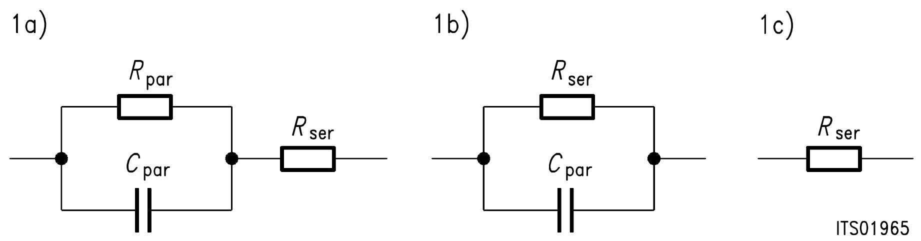


Figure 6

Equivalent Circuit Diagram 1

The configurations 1b) and 1c) can be derived from the equivalent circuit diagram 1a) by zeroing the elements that are not used.

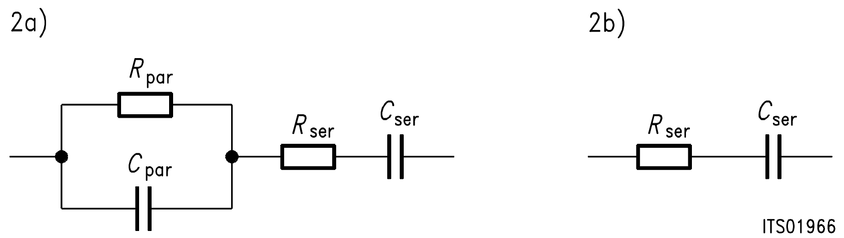


Figure 7

Equivalent Circuit Diagram 2

With R_{par} = 0 the entry of a series impedance 2b) becomes possible with equivalent circuit diagram 2a).

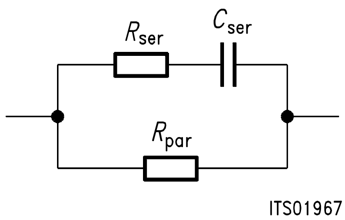


Figure 8

Equivalent Circuit Diagram 3

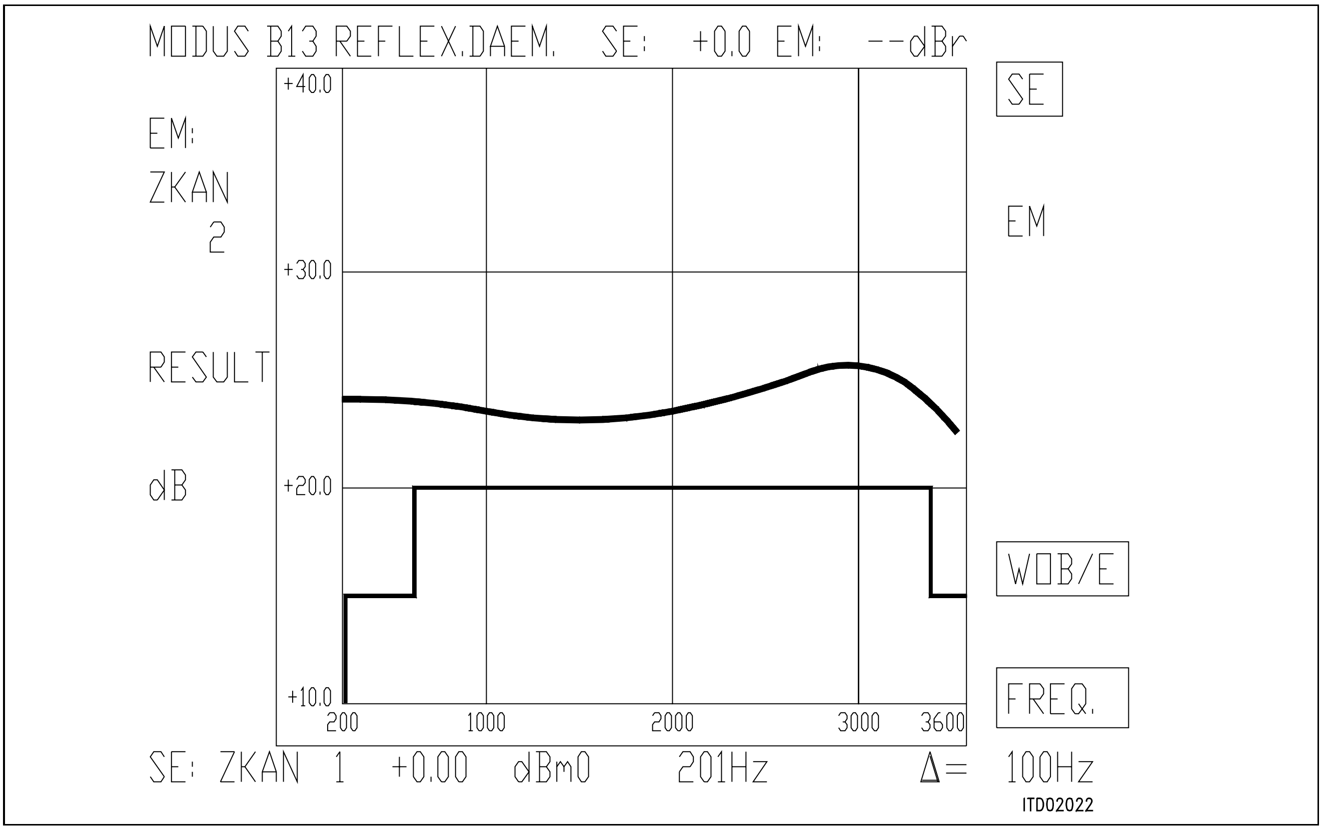


Figure 9

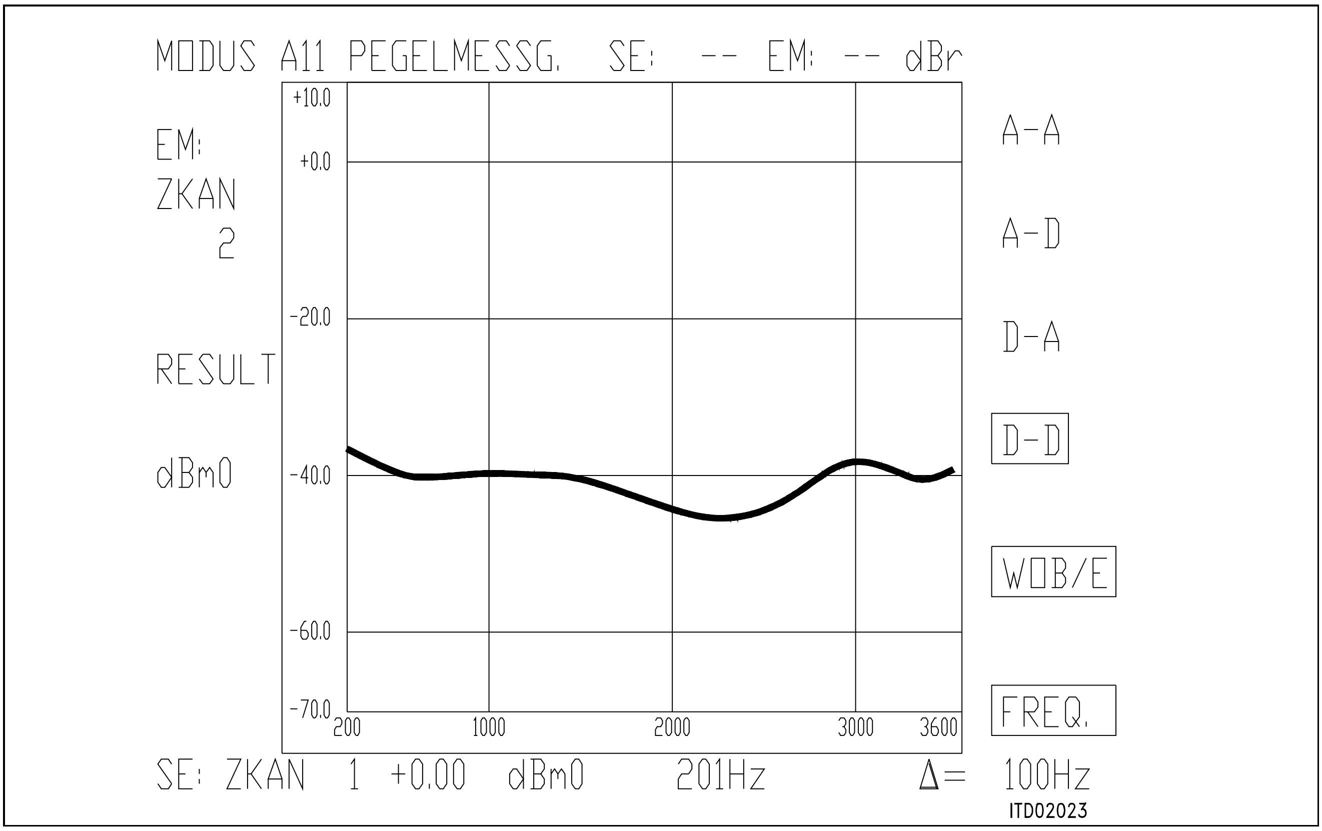


Figure 10

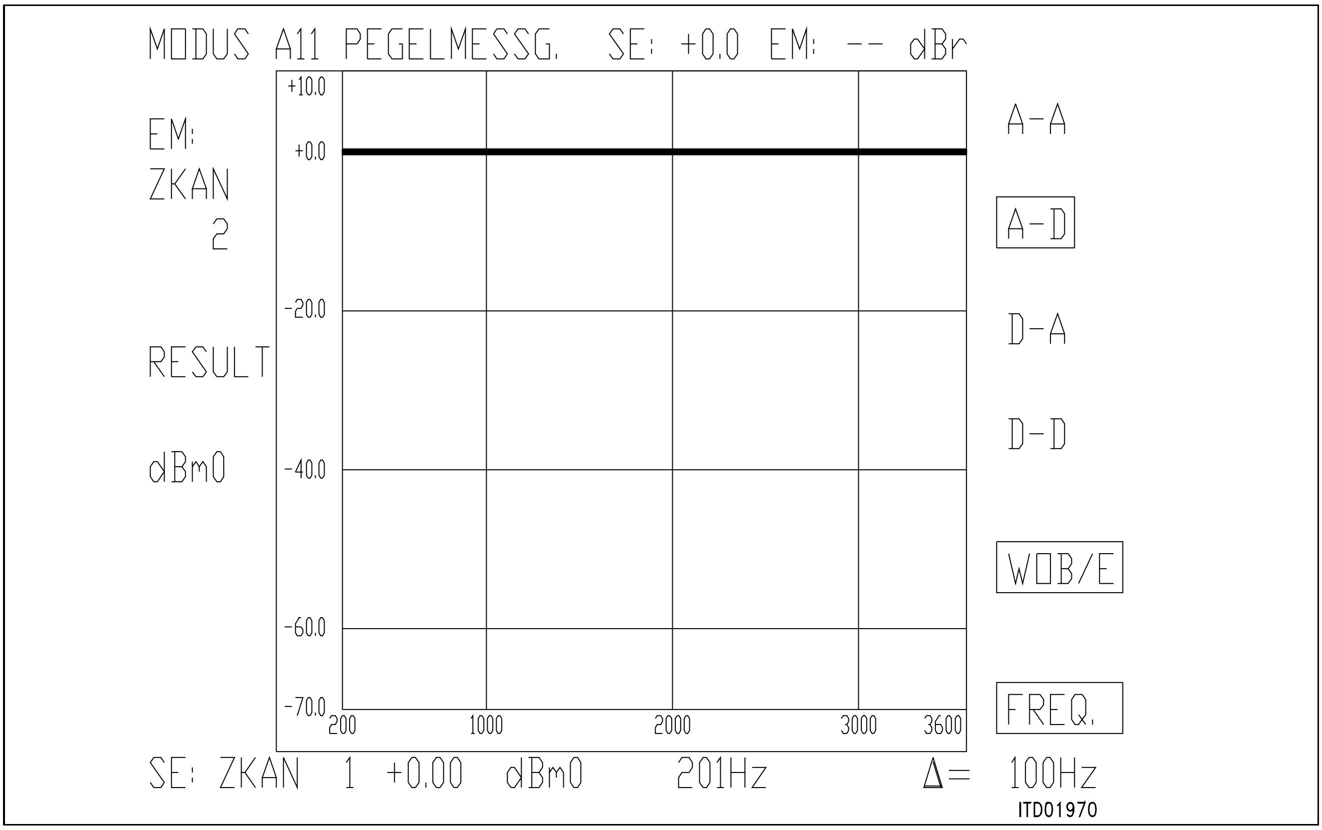


Figure 11

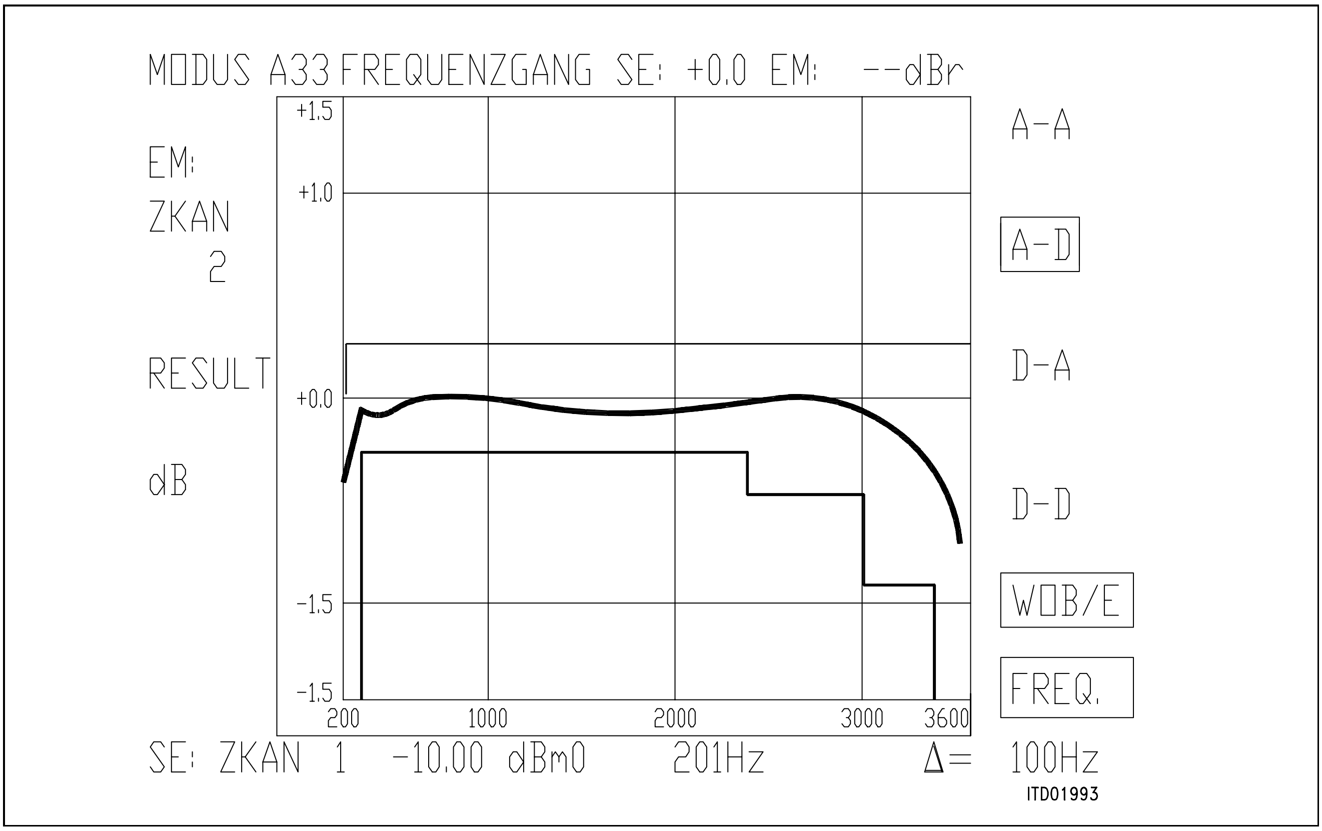


Figure 12

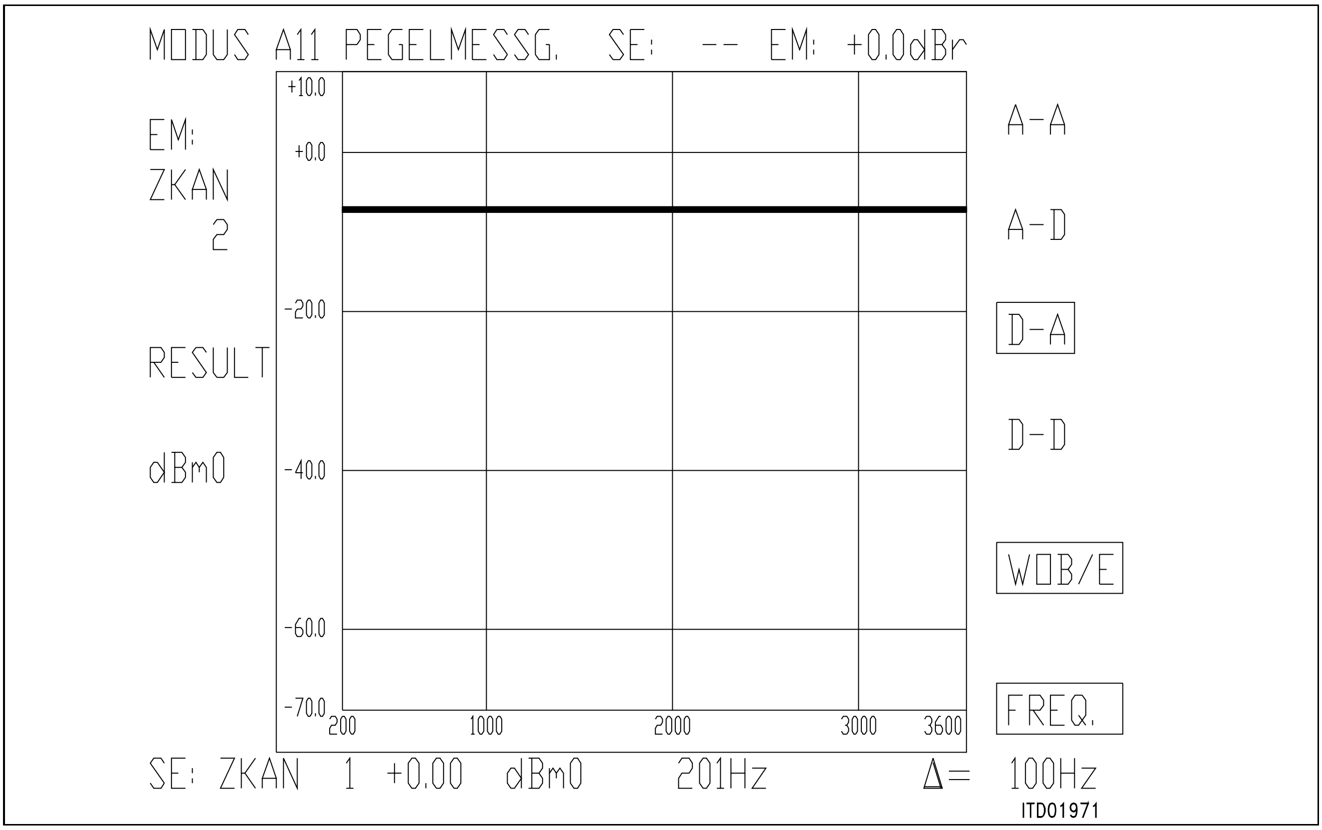


Figure 13

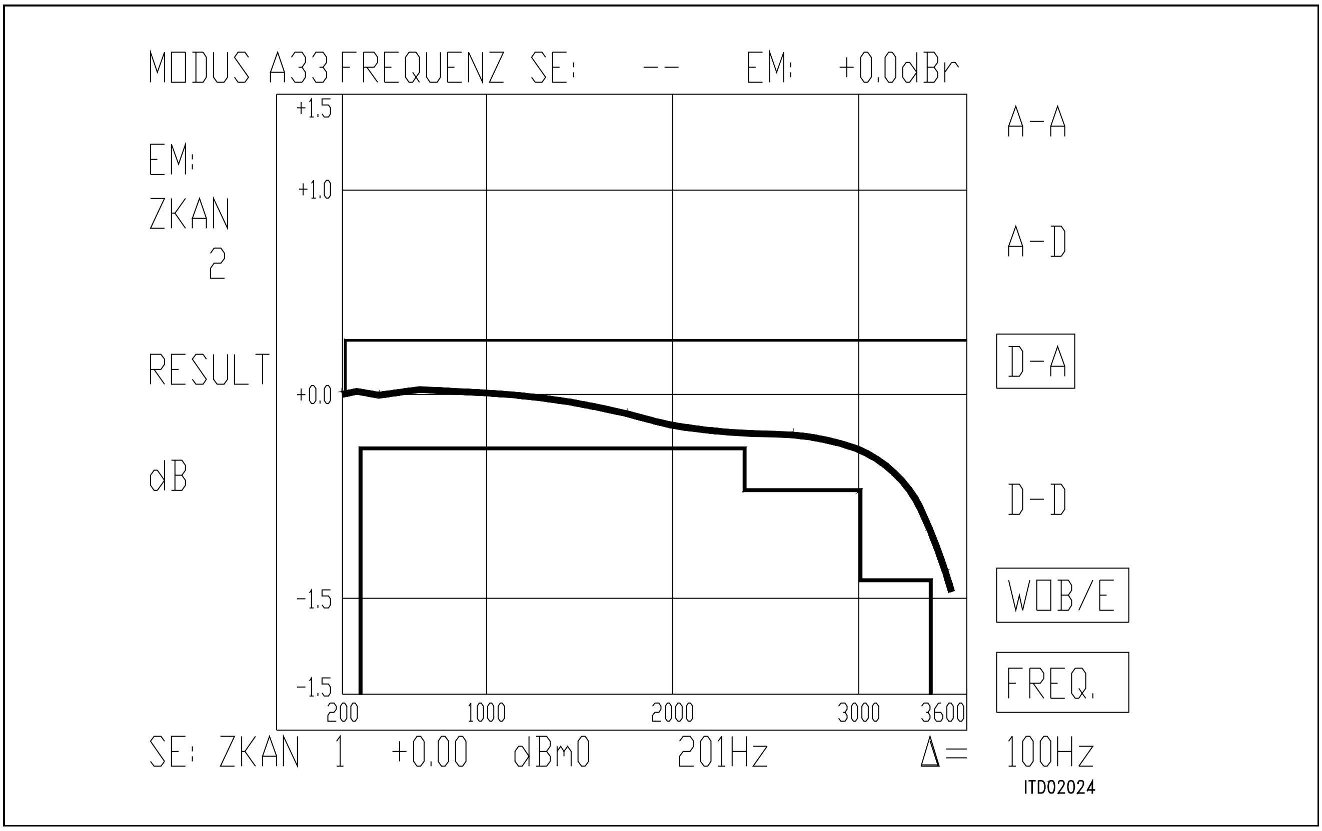


Figure 14

SICOFI® Application Together with Transformer SLIC with Series Feeding

Contents **Page**

1 Introduction

Although the trend in Subscriber Line Interface Circuit design is to integrate as many functions as possible, transformers are still often used in the design of public or private exchange line cards mainly because of their low cost, high reliability and better symetry and galvanic separation.

This note describes an application of the Siemens SIgnal processing COdec FIlter (SICOFI) in a line card equipped with a transformer for the connection of analog subscriber lines. This is intended to be an example from which the user can build his own circuit and program.

Terminology:

In the following, we will call "SLIC" the hardware and software corresponding to the analog components in a Subscriber Line Interface Circuit **excluding** the SICOFI chip.

Overview:

This note begins with generalities about transformers and SLIC functions.

Then comes an example of line card circuitry.

The third part is the calculation of the model for the SLIC.

The corresponding software is then described and used in combination with the SICOFI coefficient program.

Measurements show the fulfilement of the German Post specifications.

Next comes a word about possible strategies.

A listing of the TRAFOS SLIC FORTRAN program can be printed by the user from the source file.

2 General

2.1 SLIC Functions

The main functions of the SLIC are to provide the BORSHT functions (Battery feeding, Overvoltage protection, Ringing, Signaling, Hybrid function, Testing).

In the case of a SLIC circuit in combination with the SICOFI, the hybrid function is splitted into the two-wire to four-wire conversion realized by the SLIC and the hybrid balancing provided by the internal B-filter of the SICOFI.

The other functions (such as off-hook detection, metering, standby mode, ringing) do not affect the speech signal.

Therefore we will not consider these in the scope of this paper.

The signal on a telephone line can be considered as comprising of two parts:

- A DC voltage to feed the subscriber terminal.
- An AC voltage (the speech signal) which has to be transferred in both directions: PABX-line (TRANSMIT) and line-PABX (RECEIVE) with the right attenuation and without distortion.

To separate AC and DC correctly, the circuit has to present a high pass at low frequencies and a specified input impedance (matching impedance) in regard to the AC signal.

A flat frequency response is also required.

2.2 Principles

Schematic: A simple SLIC circuit can be schematized as follows:

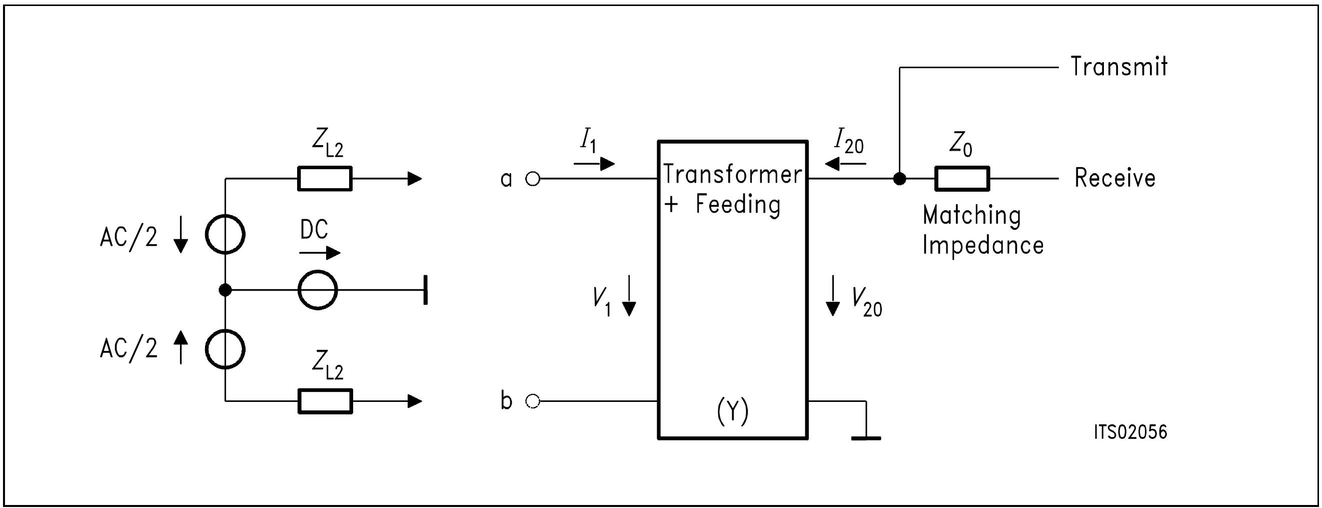


Figure 1

The feeding can be of different kind:

- Series feeding

Transformer: Generally iron core

Advantages:
The high frequency current is stopped by the coils of the transformer itself.

Drawbacks:
It is difficult to dimension a transformer with a low leakage inductance. High current in the primary half coils.

A large core is required in order to prevent saturation.

- Parallel feeding

Transformer: Generally ferrite core (allows lower leakage inductance but comes easier in saturation)

Advantages:

Blocks the DC current before the transformer coils.

Drawbacks:

Necessity of a blocking circuit before the transformer which includes often a large coil or an electronic circuit with problems of non linearities. Therefore the feeding circuit often presents a frequency dependant equivalent impedance which is not easy to model.

2.3 Transformer Characteristics

Philosophy of the simplifications:

Let us take an ideal transformer with 1 to 1 ratio, let us consider the AC signal only and only one direction at a time.

The equivalent circuit in transmit direction will be:

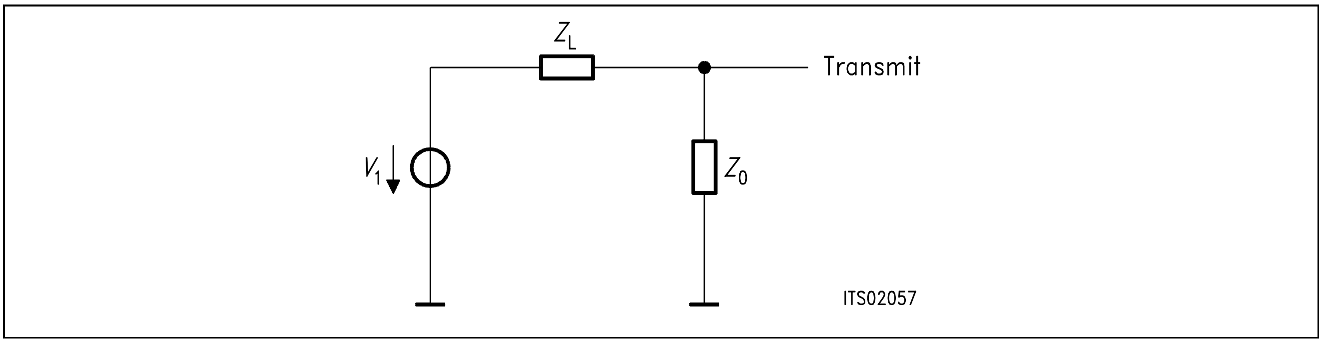


Figure 2

and in receive direction:

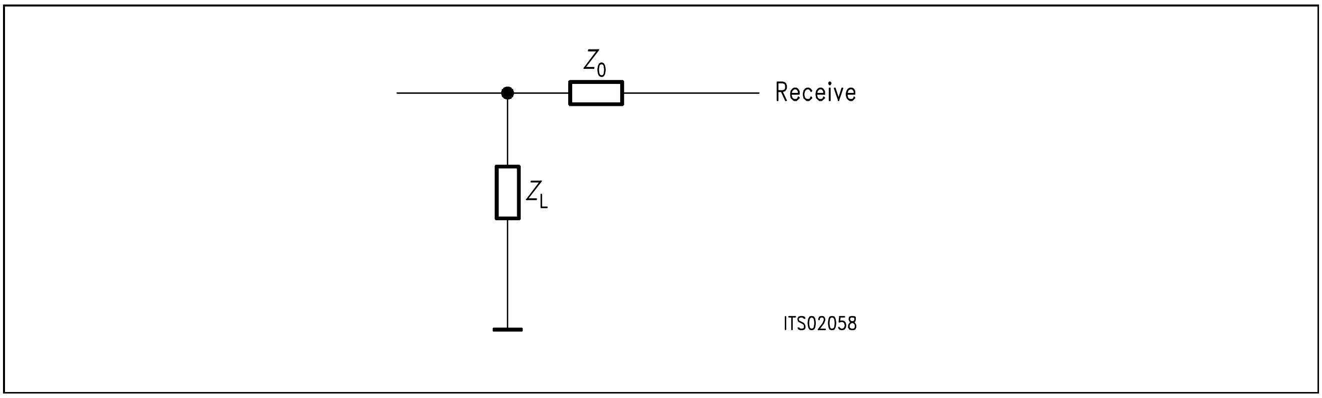


Figure 3

We can see that if $Z_L = Z_0$ the attenuation in both directions is 6 dB.

The real circuit is more complicated because of the loop added by the SICOFI Z-filter and because of the non-ideal transformer.

Optional amplifier are also used for several purposes:

- The SICOFI can drive loads only above typically 300 Ω, so that an opamp is not necessary.
- Add gain in receive direction.
- Add possibly group delay if the SICOFI B-filter can not compensate fully the transformer distortion. (Improves the trans hybrid loss at low frequencies).

2.4 Equivalent Circuit of the Transformer

A low frequency transformer can be modelled with simple parts:

L_1	main inductance
L_{s1}, L_{s2}	stray inductances
R_{CU1}, R_{CU2}	primary and secondary copper resistance
C_W	winding capacitance
W_1, W_2	number of windings at primary and secondary
ZSP with C_{SP}, R_{SP}	feeding (parallel or serial)

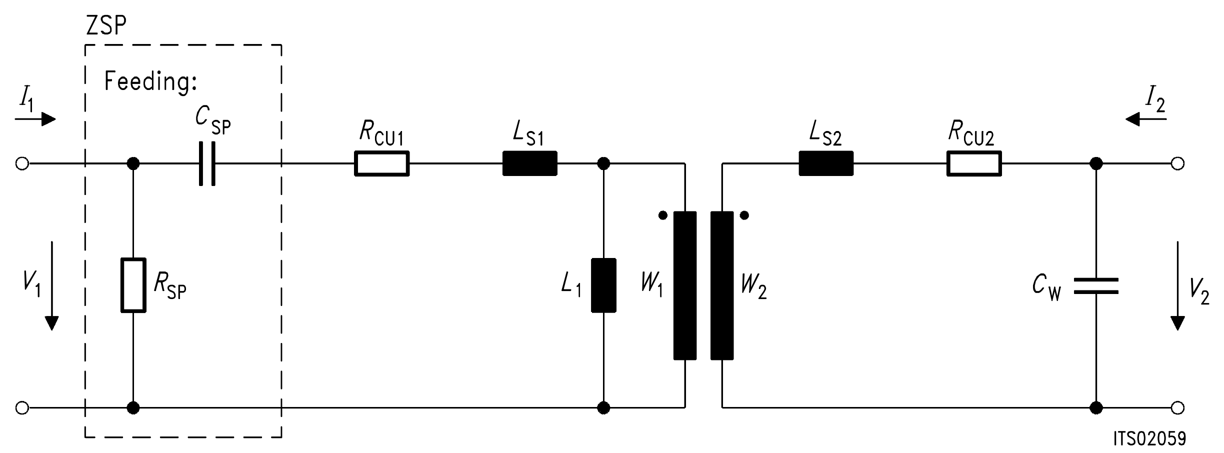


Figure 4

2.5 Transformer Measurements

Method:

- Measurement of the primary and secondary copper resistances with a simple Ohmmeter. (R_{CU1} and R_{CU2})
- Short circuit at the secondary:
  Measurement of leakage inductance (L_{s1} and L_{s2}) and winding capacitance (C_w) with an impedance analyser at 1 kHz.
- Open circuit at the secondary:
  Measurement of the main inductance (L_1) with the impedance analyser.
- The other data (number of turns primary and secondary: W_1, W_2) have to be obtained from the supplier.

Results:

In order to prove the capabilities of the SICOFI for Germany, we have choosen a transformer with series feeding which is simple to use. It has been dimensioned for the specifications of the German Post: Z_{in} must be close to 220 Ω + (820 Ω//115 nF) (see specifications in appendix A1)

R_{CU1} = 123 Ω |
R_{CU2} = 121 Ω | The sum is approximately the series resistance of Z_{in}

$L_{S2} = L_{S1}$ = 4.2 mH |
C_w = 0.1 nF | > the smaller, the better!

L_1 = 0.835 H | a value larger than 700 mH is recommended - the larger the better!

W_1 = 1400
W_2 = 1400

Note: The main inductance has a large influence on the frequency response at low frequencies: It forms a high pass filter with the copper resistances and the line impedance; the cut-off frequency should be kept as low as possible by increasing L_1.
The leakage inductances influence more the high frequency response (they form a low pass with the winding capacitance and therefore limit the frequency band of the transformer).
The winding capacitance can be decreased by using a shielding screen between the primary and secondary windings.

3 Hardware

Our circuit is a didactic circuit with a series feeding and values for Z_0 that have been optimized by trying different resistors and capacitors in order to obtain an optimum with the SLIC alone (Z-filter switched off).

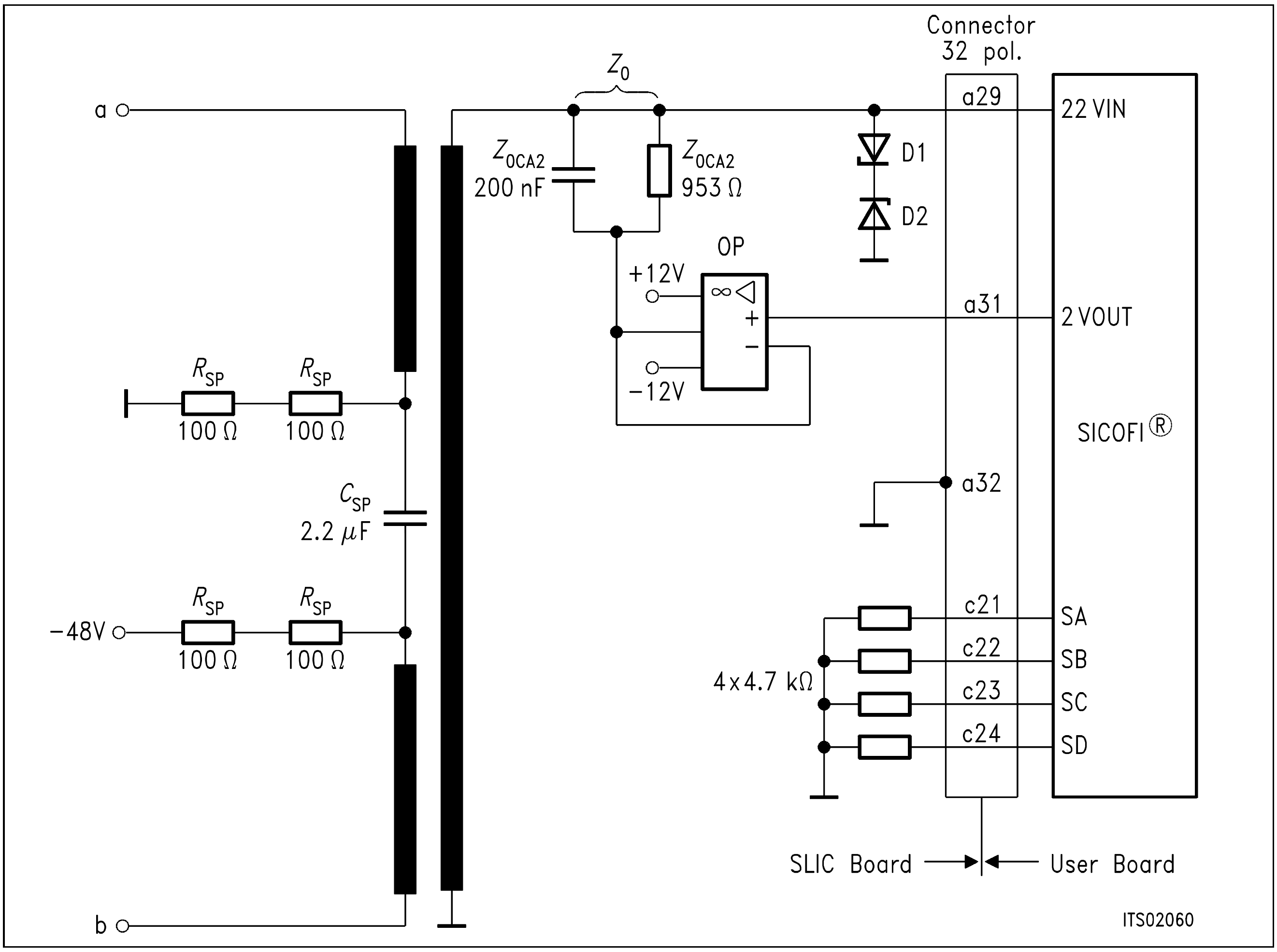


Figure 5

Transformer	Siemens EK 25 Nr. EK C39030-Z4-C15
Z_{0RA1}	953 Ω
Z_{0CA2}	200 nF
D1	3V9
D2	3V9
C_{SP}	2.2 µF, 63 V
R_{SP}	4 × 100 Ω, 1 W

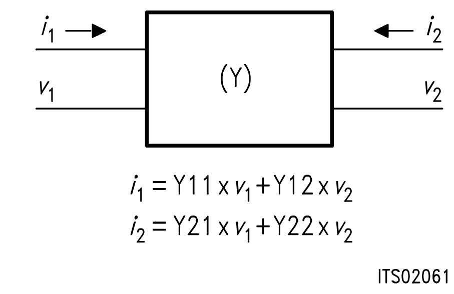
Operational-Amplifier Siemens LF356N

4 Software

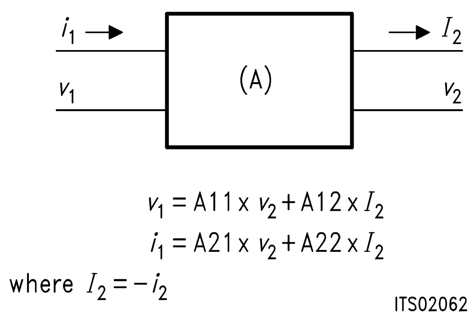
4.1 Introduction

The following two ports models ("black boxes" which the user can change as he wishes) are used to model the transformer.

Admittance Matrix:



Chain Matrix:



In the model, chain matrix (A-matrix) are first used in order to make easy chain multiplications and improve the modularity of the program.

Then the transformer is considered by its admittance matrix (subroutine TRSLIC).

4.2 Conventions

As we are working with two ports model, we need 2 × 2 matrixes and because we work with complex numbers we need a third dimension:

The matrixes are declared as arrays of dimension 3:

A(2,2,2)

where the first number is 1 for real and 2 for imaginary part and the two other ones are for lines and columns of the matrix.

After the multiplications, these matrixes are reduced to their elements (complex):

A11(2),A12(2),A21(2),A22(2)

in other words:

A(1,1,1) + j × A(2,1,1) = A11(1) + j × A11(2)

4.3 Subroutines

The transformer is modelled in the subroutine TRSLIC.

Input is FREQ (frequency);

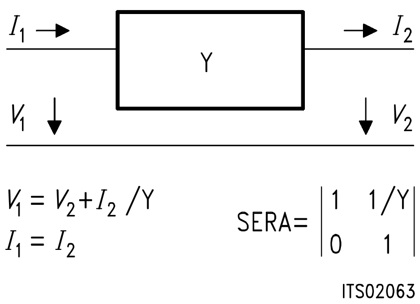
Output of this routine are the Y parameter of the transformer, including the Y-matrix determinant.

TRSLIC uses subroutines which are the elementary A-matrix calculations:

4.4 Elementary A-Matrixes

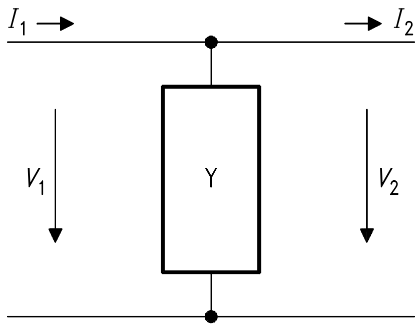
4.4.1 SERA

SERies A-matrix
Y: admittance in series



4.4.2 PARA

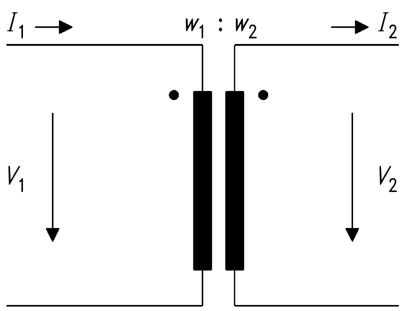
PARallel A-matrix
Y: admittance in parallel



$$V_1 = V_2$$
$$I_1 = Y \times V_2 + I_2$$
$$\text{PARA} = \begin{vmatrix} 1 & 0 \\ Y & 1 \end{vmatrix}$$

ITS02064

4.4.3 Transformer



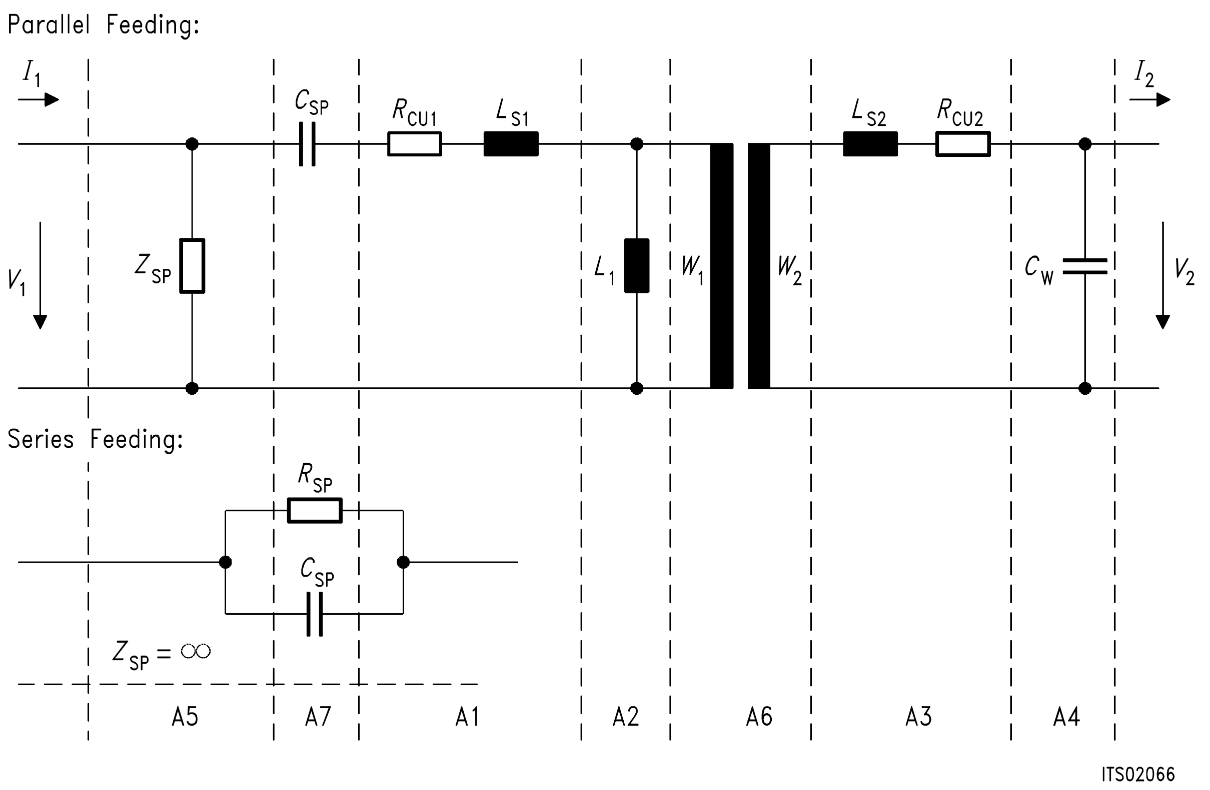
$$V_1 = (w_1/w_2) \quad V_2$$
$$I_1 = (w_1/w_2) \quad I_2$$
$$u = (w_1/w_2)$$
$$\text{A6} = \begin{vmatrix} 1/u & 0 \\ 0 & u \end{vmatrix}$$

ITS02065

$w_1 : w_2$
w_1 / w_2

If the transformer has inverted coils then change the sign of u (it is equivalent to make $w_2 = -w_2$).

4.5 Model Calculations



The resulting A-matrix is: A = A5 × A7 × A1 × A2 × A6 × A3 × A4

Figure 6

Note: "×" Is a complex matrix multiplication: See subroutine CMATMUL

Admittance elements of the different matrixes:

$W = 2\pi \times F_{REQ}$

* Y1 = 1 / (R_{CU1} + j × W × L_{S1})

* Y2 = 1 / j × W × L1

* Y3 = 1 / (R_{CU1} + j ×W × L_{S2})

* Y4 = j × W × C_W

Parallel feeding

* Y5 = 1 / Z_{SP}

* Y7 = j ×W × C_{SP}

Series feeding

* Y5 = 0

* Y7 = C_{SP} // R_{SP}

= 1/R_{SP} + j × w × C_{SP}

4.5.1 Y-Matrix

From the A parameters, we can compute the Y parameters (*):
Y11 = A22/A12 Y12 = – DETA/A12
Y21 = – 1/A12 Y22 = A11/A12
and YDET = Y11 × Y22 – Y12 × Y21

4.5.2 SLIC M-Matrix

An additional amplifier (AX) has been added in transmit direction so that the circuit is as general as possible.
Schematic circuit diagram of transformer SLIC software: **figure 7 and figure 8**.

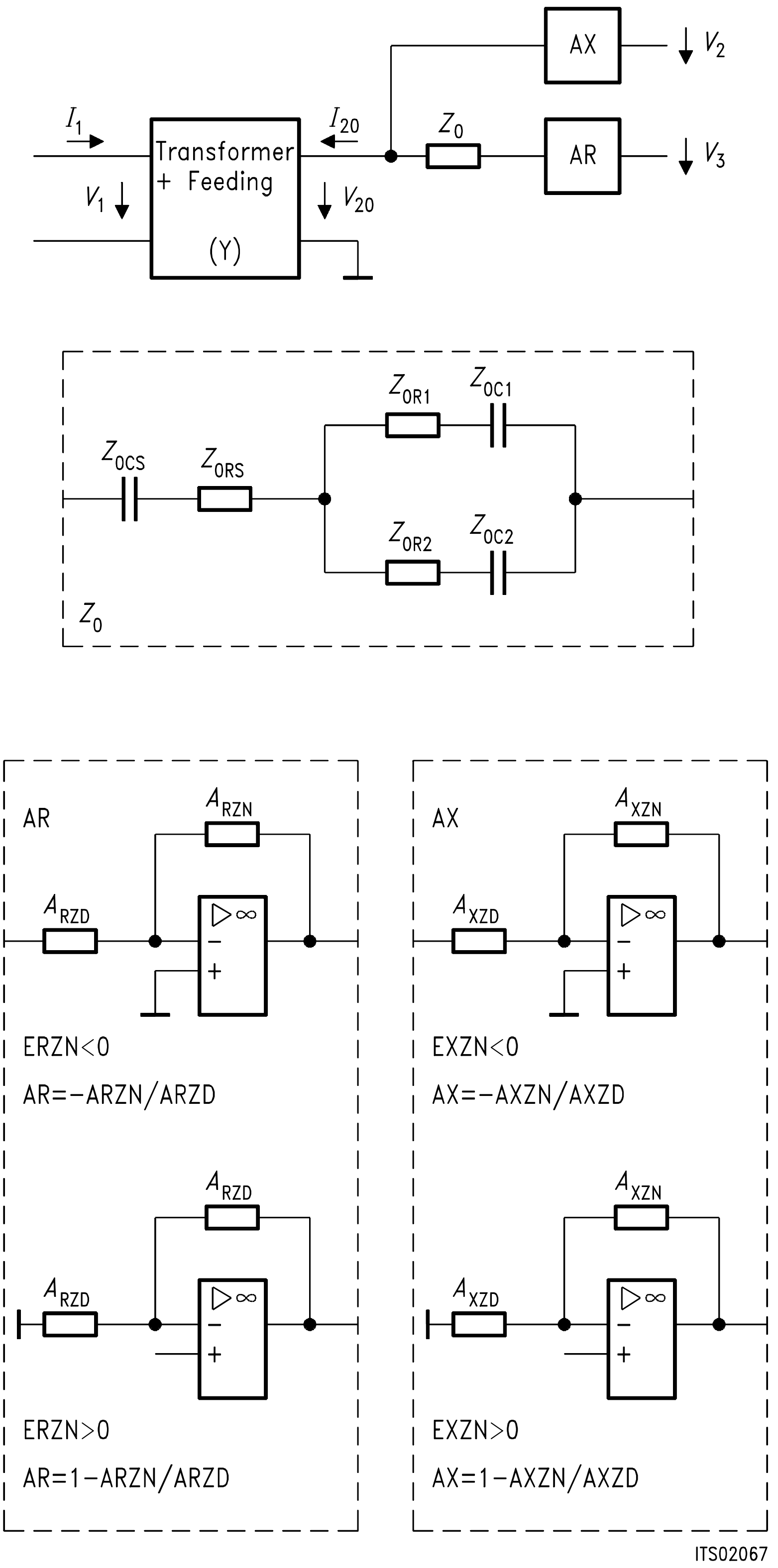

AX
AR
V_2
V_3
I_1
I_{20}
Z_0
Transformer
+ Feeding
(Y)
V_1
V_{20}
Z_{0R1}
Z_{0C1}
Z_{0CS}
Z_{0RS}
Z_{0R2}
Z_{0C2}
Z_0
AR
A_{RZN}
A_{RZD}
ERZN<0
AR=−ARZN/ARZD
A_{RZD}
A_{RZD}
ERZN>0
AR=1−ARZN/ARZD
AX
A_{XZN}
A_{XZD}
EXZN<0
AX=−AXZN/AXZD
A_{XZN}
A_{XZD}
EXZN>0
AX=1−AXZN/AXZD
ITS02067

Figure 7

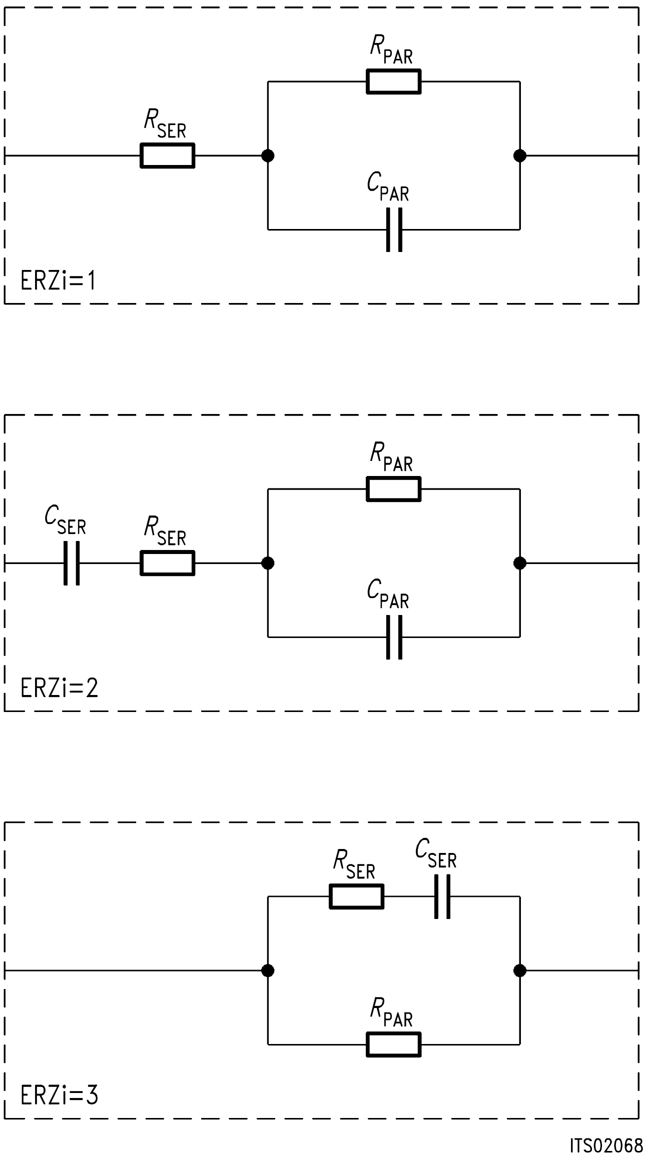


Figure 8

Impedance Models

Notes:
- Each block is modifyable by the user.
- The gains are controllable by 9 parameters:
  Example for AR (similar for AX)
- Denominator impedance: ARZD using the model ERZD=1, ERZD=2 or ERZD=3
- Nominator impedance: ARZN using the model ERZN=1, ERZN=2 or ERZN=3.
  ERZN=0 means that there is no gain in this direction (AR=1)
  Normally ERZN > 0 : AR = 1 + ARZN / ARZD
  ERZN < 0 means that we have an inverting amplifier: AR = – ARZN / ARZD

The matching impedance Z_0 is modelled with 6 parameters:
Z_{0RA1}, Z_{0CA1}, Z_{0RA2}, Z_{0CA2}: parallel part
Z_{0RS}, Z_{0CS}: serial part

Calculations:
Transformer equations:
(1) $I_1 = Y11 \times V_1 + Y12 \times V_{20}$
(2) $I_{20} = Y21 \times V_1 + Y22 \times V_{20}$
determinant: $YDET = Y11 \times Y22 - Y12 \times Y21$

A. Calculation of M11 Matrix Parameter:

M11 = I_1/V_1 when $V_3 = 0$

This is exactly the admittance Yp seen at the primary side of the transformer when the impedance Z_0 is at the secondary.(*)
Yp = (Y11 × 1/Z_0 + YDET) / Y22 + 1/Z_0
= (Y11 + YDET × Z_0) / (Y22 × Z_0 + 1)

Then:
M11 = (Y11 + YDET × Z_0) / (1 + Y22 × Z_0)

B. Calculation of M12 Matrix Parameter:

M12 = I_1/V_3 when $V_1 = 0$

The equations (1) and (2) are now:

(1) I_1 = Y12 × V_{20}
(2) I_2 = Y22 × V_{20}

The impedance seen at the secondary side of the transformer when a short circuit is at the primary side (*):

(3) Z_{OUT} = 1 / Y22
(4) V_{20} / Z_{OUT} = AR × V_3 / (Z_0 + Z_{out}) (voltage divider)

then from (3) and (4): V_{20}/V_3 = AR / (1 + Y22 × Z_0)
and with (1):
M12 = I_1/V_3 = Y12 × AR / (1 + Y22 × Z_0)

C. Calculation of M21 Matrix Parameter:

M21 = V_2/V_1 when $V_3 = 0$

The relation between V_2 and I_2 is: $V_{20} = -Z_0 \times I_2$
Then by replacing this in (2), we obtain:
– V_{20} / Z_0 = Y21 × V_1 + Y22 × V_{20}
which is equivalent to: V_{20}/V_1 = – Y21/Y22 + 1/Z_0
V_2 = AX × V20
Therefore:
M21 = – AX × Z_0 × Y21 / (1 + Z_0 × Y22)

D. Calculation of M22 Matrix Parameter:

M22 = V_2/V_3 when $V_1 = 0$

The calculations are then straightforeward:

V_2/V_3 = Ax × Ar × (Z_{IN} / Z_{IN} + Z_0)

Z_{IN} is the impedance seen at the secondary side of the transformer when there is a short circuit at the primary.(*)

Z_{IN} = 1 / Y22

Then:

M22 = V_2/V_3 = Ax × Ar / (1 + Z_0 × Y22)

(*) See "Linear Integrated Networks"
G.S.Moschytz
Bell Telephone Laboratories Series
Van Nostrand Reinhold Company

Summary:

M11 = A = (Y11 + YDET × Z_0)/(1 + Y22 × Z_0)

M12 = B = Y12 × AR / (1 + Z_0 × Y22)

M21 = C = – AX × Z_0 × Y21/(1 + Z_0 × Y22)

M22 = D = AX × AR/(1 + Z_0 × Y22)

5 Optimization

5.1 Input Data

The TRAFOS SLIC program needs a file as input which contains the data of the SLIC:

```
*ERZN :receive gain = 1+arzn/arzd or -arzn/arzd if erzn < 0
0
*ARRSN,          ARRPN,          ARCSN,          ARCPN
 0.              0.              0.              0.
*ERZD
0
*ARRSD,          ARRPD,          ARCSD,          ARCPD
 0.              0.              0.              0.
*EXZN :transmit gain = 1+axzn/axzd or -axzn/axzd if exzn < 0
0
*AXRSN,          AXRPN,          AXCSN,          AXCPN
 0.              0.              0.              0.
*EXZD
0
*AXRSD,          AXRPD,          AXCSD,          AXCPD
 0.              0.              0.              0.
*RCU1      RCU2  :cupper resistance of primary (resp. secondary)
 123.      121.
*L1
0.835
*LS1       LS2   :leakage inductances primary and secondary
 0.42E-02  0.42E-02
*CW
0.1E-09
*RSP       CSP   :feeding resistance and capacitance
 400.0     0.22E-05
*W1        W2    :Number of turn for windings
0.14E+04   0.14E+04
*ZSLI
0.5
*ZO              :matching impedance (with 6 elements)
*Z0RA1,         Z0CA1,          Z0CA2,          Z0RA2
953.               0.          0.2E-06      0.
*Z0RS,           Z0CS
 0.                0.
```

5.2 Runs

Specifications:

The specifications for West-Germany (see BRD.SPE in appendix A1)

A first run with automatical Z-filter optimization (PZIN = 0) does not give satisfiing results for the return loss.

A second run with modified specifications (see BRD4.SPE in appendix A1) is necessary with repetition of the Z-filter optimization (ZREP = Y).

Result file:

NICE.RES is a result file which has been obtained with a version V3.x of SICOFI program.

NICE.RES:

```
Input_file_name: NICE.CTL                      Date: 18.04.88  10:03
 SPEC = BRD4.SPE                               SLIC = TRAFOS.SLI
 BYTE = REF.BYT      CHNR =  0,A
 PLO  = N

 ON = ALL                     REL  = Y                    SHORT = N
 OPT =  Z+X+R+B               ZXRB =  NNNN
    FZ =  300.00       3400.0       ZLIM = 2.00
 ZREP  =N                          ZSIGN = 1
   FR =   360.00       3390.0
 RFIL =  N             RREFQ = N       RREF =  1.5367
   FX =   500.00       3300.0
 XFIL =  N             XREFQ = N       XREF = -2.5370
        PB  = 10         GWFB= 0.500E-01 TBM =  1
 FB  =    300.00       500.00       700.00       1000.0       1500.0
          2100.0       2300.0       2900.0       3200.0       3300.0
 WFB =    4.0000       2.0000       1.0000       5.0000       1.0000
          2.0000       1.0000       5.0000       1.0000       1.0000
 APOF =  0.00E+00 DPOF =  0.00E+00 APRE =  0.00E+00 DPRE =  0.00E+00
 XZQ =   0.49121093750000000E+00  -0.14257812500000000E+00
        -0.40625000000000000E+00  -0.12988281250000000E+00
         0.18359375000000000E+00
 XRQ =  0.6562500000  0.2695312500  0.0332031250  0.0234375000
         0.0244140625
 XXQ =  1.2187500000  0.1542968750 -0.1640625000 -0.0078125000
        -0.0019531250
 XBQ =   0.35937500000000000E+00   0.13867187500000000E+00
         0.74218750000000000E+00  -0.57031250000000000E+00       -
        -0.60937500000000000E+00
        -0.65625000000000000E+00   0.35937500000000000E+00
        -0.11328125000000000E+01   0.90625000000000000E+00
        -0.34375000000000000E+00
 XGQ =  0.5742187500  1.6406250000

;

 Bytes for Z-Filter (13):             30,C1,5B,92,1B,3B,13,3E
 Bytes for R-Filter (2B):             50,BA,94,42,C9,42,12,22
 Bytes for X-Filter (23):             D0,C8,8C,BB,22,23,0C,B2
 Bytes for Gain-factors (30):         31,A2,10,32
 2nd part of bytes B-Filter (0B):     00,1A,0A,AB,38,24,B1,21
 1st part of bytes B-Filter (03):     92,B2,39,13,D1,33,2B,B1
 Bytes for B-filter delay (18):       19,19,11,19

 * TRAFO SLIC

 *Z0RA1=  953.00    *Z0CA1=   .00000   *Z0RA2=  .00000
 *Z0CA2=  .20000E-06*Z0RS =   .00000   *Z0CS =  .00000
 * ERZN= 0
 *ARRSN=  .00000    *ARCSN=   .00000   *ARRPN=  .00000    *ARCPN=  .00000
 * ERZD= 0
 *ARRSD=  .00000    *ARCSD=   .00000   *ARRPD=  .00000    *ARCPD=  .00000
 * EXZN= 0
 *AXRSN=  .00000    *AXCSN=   .00000   *AXRPN=  .00000    *AXCPN=  .00000
 * EXZD= 0
```

```
*AXRSD=  .00000    *AXCSD=  .00000    *AXRPD=  .00000    *AXCPD=  .00000
*RCU1 =  123.00    *RCU2 =  121.00    *   L1 =  .83500
* LS1 =  .42000E-02* LS2 =  .42000E-02* CW  =  .10000E-09
* RSP    400.00    * CSP    .22000E-05
* W1  =  1400.0    * W2  =  1400.0
*ZSLI =  .50000

 Run #    2

 Z-FILTER calculation results
   Generator impedance ZI at a,b line!
   Calculated and quantized coefficients:

 XZ  =    0.49089  -0.14218  -0.41298  -0.13023   0.18335
 XZQ =    0.49121  -0.14258  -0.40625  -0.12988   0.18359
 Bytes for Z-Filter (13):    30,C1,5B,92,1B,3B,13,3E

 RETURN LOSS

   FREQ        loss                       FREQ        loss
   (Hz)        (dB)                        (Hz)        (dB)
    100.      10.464                      1800.      24.463
    200.      12.502                      1900.      23.683
    300.      14.850                      2000.      23.095
    400.      17.047                      2100.      22.680
    500.      19.118                      2200.      22.432
    600.      21.177                      2300.      22.359
    700.      23.354                      2400.      22.477
    800.      25.792                      2500.      22.824
    900.      28.673                      2600.      23.458
   1000.      32.201                      2700.      24.485
   1100.      35.992                      2800.      26.083
   1200.      36.559                      2900.      28.532
   1300.      33.524                      3000.      31.690
   1400.      30.624                      3100.      31.133
   1500.      28.425                      3200.      26.214
   1600.      26.758                      3300.      21.848
   1700.      25.469                      3400.      18.387

 Min. Z-loop reserve:     1.053 dB
        at frequency:    7000.0 Hz
 Min. Z-loop mirror signal reserve:      4.793 dB
                      at frequency:     6500.0 Hz

 Run #    1

 X-FILTER calculation results
   Calculated and quantized coefficients:

 XX  =    1.21418   0.15483  -0.16741  -0.00821  -0.00233
 XXQ =    1.21875   0.15430  -0.16406  -0.00781  -0.00195
 Bytes for X-Filter (23):    D0,C8,8C,BB,22,23,0C,B2

 GX results:
 All attenuation values (in dB) refer to FREF =    1014. Hz
```

```
      RLX    SLIC+Z    VREF/VSICOFI    XREF          GX
     0.00 -   2.42  -      4.42    -  -2.54    =     -4.30  ideal
     0.00 =   2.42  +      4.42    +  -2.54    +     -4.30  quant

  Second byte for Gain:      ,10,32
  Calculation of transmit transfer function (AD)
  All attenuation values (in dB) refer to FREF =     1014.0 Hz
    Generator impedance ZI at a,b line!

TGREF CA =   0.327 ms     TGREF CB =   0.340 ms
```

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
100.	18.755	3.232	2000.	0.000	0.013
200.	1.722	2.198	2100.	-0.006	0.018
300.	0.411	0.815	2200.	-0.010	0.024
400.	0.112	0.421	2300.	-0.013	0.032
500.	0.000	0.249	2400.	-0.015	0.040
600.	-0.036	0.156	2500.	-0.016	0.051
700.	-0.037	0.101	2600.	-0.015	0.062
800.	-0.024	0.065	2700.	-0.013	0.076
900.	-0.008	0.042	2800.	-0.007	0.093
1000.	0.008	0.026	2900.	0.002	0.113
1100.	0.020	0.015	3000.	0.018	0.136
1200.	0.028	0.008	3100.	0.043	0.166
1300.	0.032	0.003	3200.	0.086	0.202
1400.	0.032	0.001	3300.	0.156	0.249
1500.	0.029	0.000	3400.	0.274	0.310
1600.	0.025	0.001	3500.	0.473	0.395
1700.	0.019	0.002	3600.	0.828	0.519
1800.	0.012	0.005	3700.	1.520	0.717
1900.	0.006	0.008	3800.	3.115	1.055

```
Run #   1

R-FILTER calculation results
  Calculated and quantized coefficients:

XR  =    0.65560   0.27251   0.03267   0.02341   0.02505
XRQ =    0.65625   0.26953   0.03320   0.02344   0.02441
Bytes for R-Filter (23):    50,BA,94,42,C9,42,12,22

GR results:
All attenuation values (in dB) refer to FREF=    1014. Hz

   -RLR    SLIC+Z    VSICOFI/VREF    RREF          GR
   7.00 -   5.06  -      -4.42    -   1.54    =      4.82  ideal
   7.00 =   5.06  +      -4.42    +   1.54    +      4.82  quant

First byte for Gain (30):      31,A2
Calculation of receive transfer function (DA)
All attenuation values (in dB) refer to FREF =     1014.0 Hz
  Terminating impedance ZI at a,b line!

TGREF CA =   0.264 ms      TGREF CB =   0.247 ms
```

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
100.	5.006	0.707	2000.	-0.117	0.038
200.	1.426	0.405	2100.	-0.156	0.046
300.	0.397	0.223	2200.	-0.181	0.054
400.	0.022	0.134	2300.	-0.187	0.062
500.	-0.130	0.087	2400.	-0.176	0.070
600.	-0.182	0.060	2500.	-0.146	0.078
700.	-0.177	0.042	2600.	-0.103	0.086
800.	-0.139	0.029	2700.	-0.051	0.095
900.	-0.083	0.018	2800.	0.003	0.106
1000.	-0.019	0.011	2900.	0.048	0.121
1100.	0.041	0.005	3000.	0.076	0.141
1200.	0.089	0.001	3100.	0.080	0.167
1300.	0.119	0.000	3200.	0.057	0.204
1400.	0.128	0.001	3300.	0.013	0.254
1500.	0.116	0.004	3400.	-0.028	0.321
1600.	0.085	0.009	3500.	-0.021	0.415
1700.	0.040	0.015	3600.	0.122	0.549
1800.	-0.013	0.022	3700.	0.606	0.758
1900.	-0.067	0.030	3800.	2.014	1.104

```
Run #    1
B-FILTER calculation results
  Terminating impedance ZL at a,b line!

Calculated and quantized coefficients:

XB  =    0.35600   0.13862   0.74342  -0.56848  -0.60448
         0.65780   0.36312  -1.13668   0.89881  -0.34413
XBQ =    0.35937   0.13867   0.74219  -0.57031  -0.60937
         0.65625   0.35937  -1.13281   0.90625  -0.34375
2nd part of bytes B-Filter (0B):    00,1A,0A,AB,38,24,B1,21
1st part of bytes B-Filter (03):    92,B2,39,13,D1,33,2B,B1
```

TRANS HYBRID LOSS

FREQ (Hz)	loss (dB)	FREQ (Hz)	loss (dB)
100.	22.902	1800.	25.059
200.	13.779	1900.	24.310
300.	18.401	2000.	24.081
400.	23.795	2100.	24.341
500.	29.665	2200.	25.093
600.	32.722	2300.	26.373
700.	31.077	2400.	28.244
800.	29.704	2500.	30.798
900.	29.509	2600.	34.094
1000.	30.459	2700.	37.788
1100.	32.798	2800.	40.341
1200.	37.665	2900.	41.168
1300.	51.231	3000.	42.854
1400.	38.240	3100.	49.973
1500.	32.000	3200.	47.925
1600.	28.571	3300.	36.752
1700.	26.415	3400.	30.941

```
Additional B-filter delay (in seconds):   .625E-04
Bytes for B-filter delay (18):   19,19,11,19
```

6 Measurements

See appendix A2
The measurements are made with a "PCM4" from Wandel & Goltermann.

Return loss: correct.

Transmit direction (AD): Level at 1 kHz: – 0.18 dB (wanted: 0 dB). A small manual correction will be necessary.

Receive direction (DA): Level at 1 kHz: – 7.07 dB (wanted: – 7 dB).

Attenuation distortion (AD and DA): correct.

Trans Hybrid Loss (THL): should be improved!

To have a better THL, it is necessary to design an other transformer.

7 Strategies

The SICOFI makes it possible to use the same hardware for different countries specifications by changing the coefficients programming of the SICOFI.

In general, it is necessary to already have a good return loss with the transformer alone without SICOFI. Then SICOFI improves the figures.

This requires us however to optimize the SLIC circuitry using the program as a simulation tool (especially Z-filter optimization):

1. Set Z_0 to a given value

2. Run automatical Z-filter optimization for the given Z_0 impedance and for all the specifications.

3. Change the impedance Z_0

4. Redo step 1 until having obtained an optimum.

Appendix A1

Specifications

BRD.SPE

```
FREF = 1014.0    LAW = A
UREF= 0.9488  RLX = 0.    RLR =    -7.0
ABIMP  = ZI
ERZI= 1 RSER=  220.     RPAR=  820.     CPAR= 0.115E-06
ERZL= 1 RSL =  220.     RPL =  820.      CPL = 0.115E-06
ZIN
FR            300        500        3k       3.4k
AT-           0          20         20          16
AT+          16          20         20           0

ZMIR
FR             4k        12k
AT-           30         3
AT+           30         3

DA,UPPER
FR          300   500     2.7k       3k       3.4k
AT-        100   .75     .25        .35        .75
AT+         .75   .25     .35        .75      100

DA,LOWER
FR          300         3.4k
AT-         0           -.25
AT+         -.25         0

DA,DELAY
FR            500        600        1k        2.6k    2.8k
GD-          10k       .420       .150       .085       .150
GD+          .420        .150        .085       .150    10k

AD,UPPER
FR          300   500     2.7k       3k       3.4k
AT-        100   .75     .25        .35        .75
AT+         .75   .25     .35        .75      100

AD,LOWER
FR          300         3.4k
AT-         0           -.25
AT+         -.25         0

AD,DELAY
FR            500        600        1k        2.6k    2.8k
GD-          10k       .420       .150       .085       .150
GD+          .420        .150         .085       .150    10k
DD
FR            300        500       2.5k       3.4k
AT-         0          27          27         23
AT+          23          27          27          0
```

BRD4.SPE

```
FREF = 1014.0    LAW = A
 UREF= 0.9480  RLX = 0.    RLR =    -7.0
 ABIMP  = ZI
 ERZI= 1 RSER=  220.     RPAR=  820.     CPAR= 0.115E-06
 ERZL= 1 RSL =  220.     RPL =  820.      CPL = 0.115E-06
 ZIN
 FR            300         500        3.2k      3.4k
 AT-           0           20         20         18
 AT+          16          20         20         0

 ZMIR
 FR             4k         12k
 AT-           30          3
 AT+           30          3

 DA,UPPER
 FR          300   500      2.7k       3k       3.4k
 AT-        100   .75     .25        .35        .75
 AT+         .75   .25      .35        .75      100

 DA,LOWER
 FR          300          3.4k
 AT-         0            -.25
 AT+         -.25          0

 DA,DELAY
 FR            500         600        1k        2.6k    2.8k
 GD-          10k        .420       .150       .085       .150
 GD+          .420         .150        .085       .150    10k

 AD,UPPER
 FR          300   500      2.7k      3k      3.4k
 AT-        100   .75     .25        .35        .75
 AT+         .75   .25      .35        .75      100

 AD,LOWER
 FR          300          3.4k
 AT-         0            -.25
 AT+         -.25          0

 AD,DELAY
 FR            500         600        1k        2.6k     2.8k
 GD-          10k        .420       .150       .085       .150
 GD+          .420         .150         .085       .150    10k
 DD
 FR            300         500       2.5k       3.4k
 AT-         0           27          27          23
 AT+          23          27          27          0
```

Appendix A2

Measurements

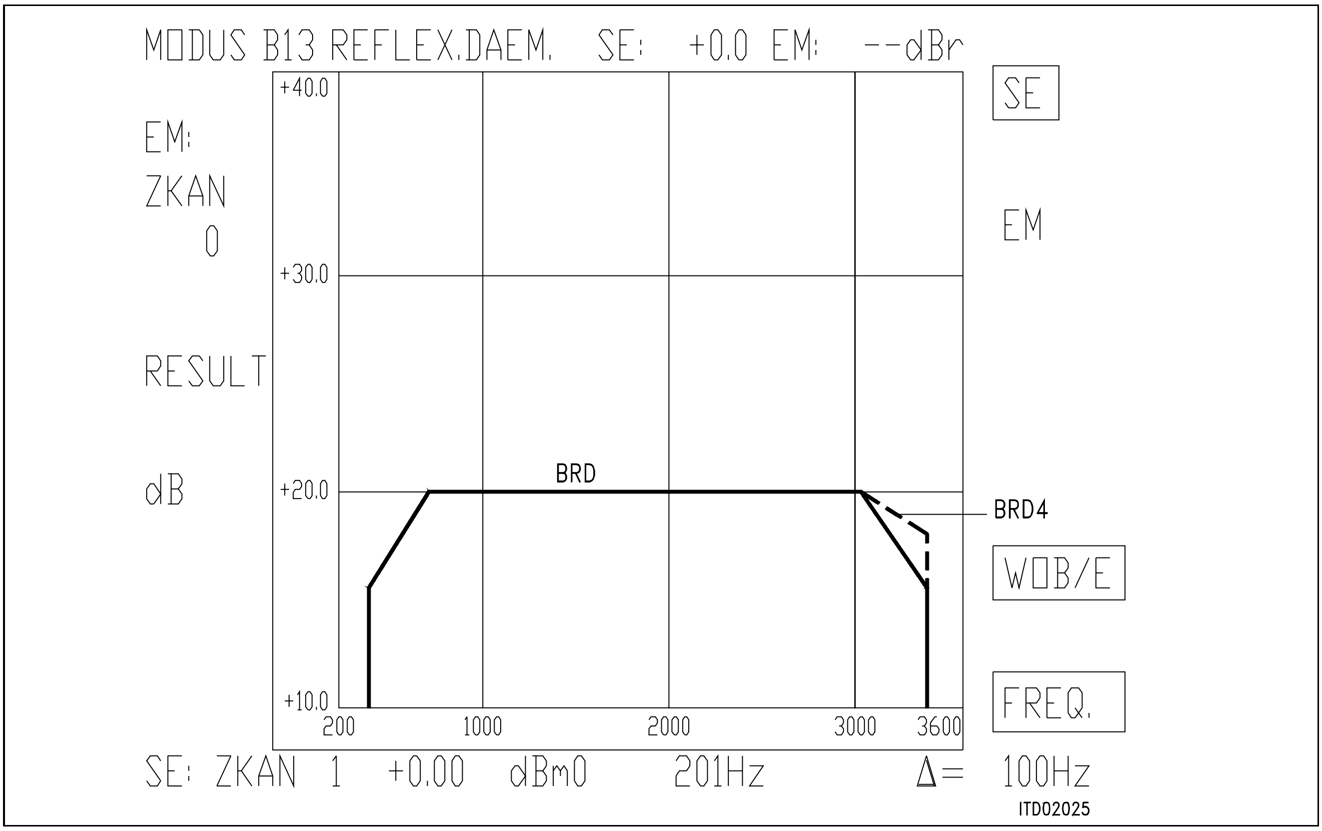


Figure 9

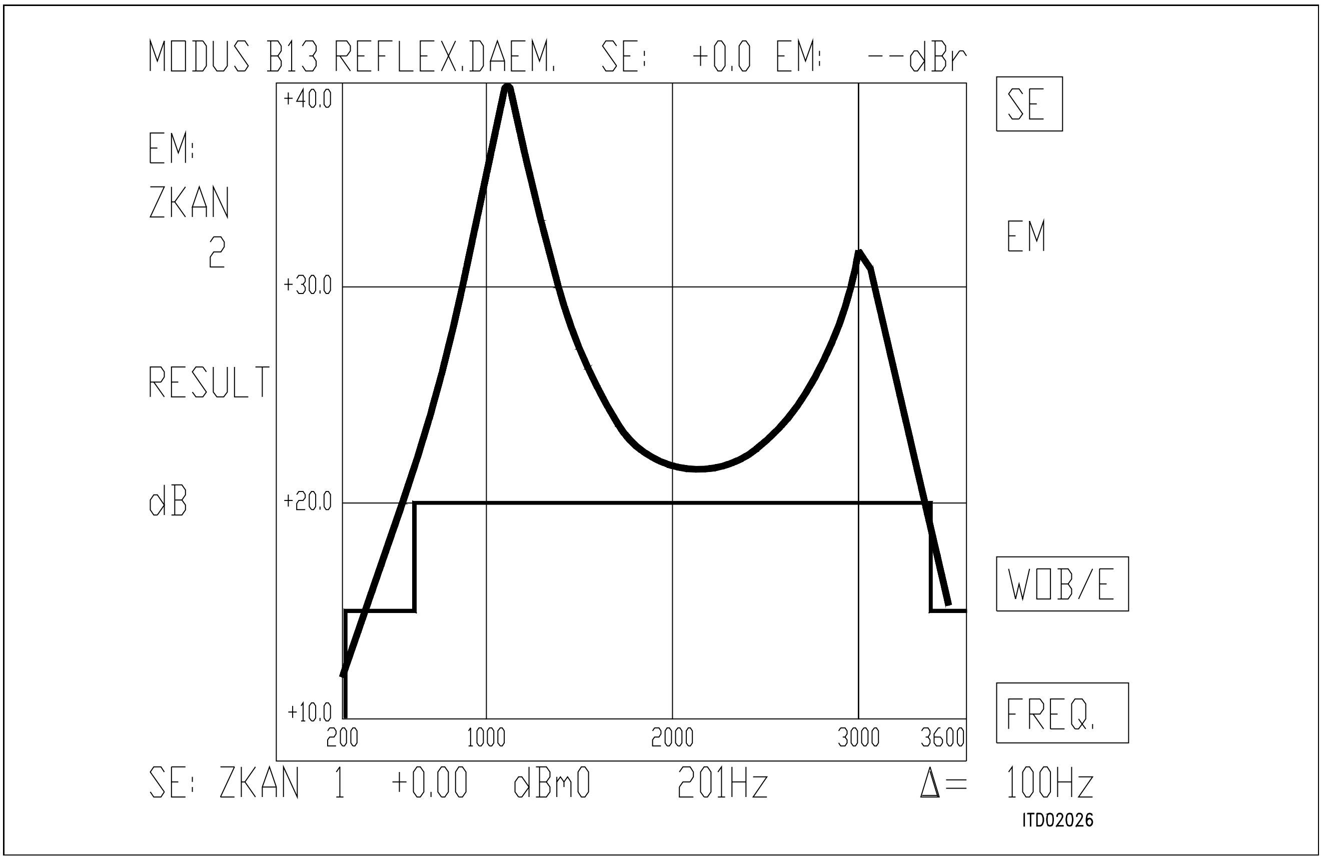


Figure 10

FREQ/Hz	RES/dB	1	FREQ/Hz	RES/dB
201	11.51*		2208	22.10
301	14.07*		2309	22.11
402	16.63		2409	22.31
502	19.08		2509	22.72
602	21.57		2610	23.41
703	24.29		2710	24.52
803	27.44		2811	26.17
903	31.60		2911	28.66
1004	37.56		3011	31.70
1104	40.98		3112	30.69
1205	35.72		3212	25.90
1305	31.58		3312	21.73
1405	28.89		3413	18.35
1506	26.99		3513	15.64
1606	25.59			
1706	24.52			
1807	23.67			
1907	23.04			
2008	22.58			
2108	22.27			

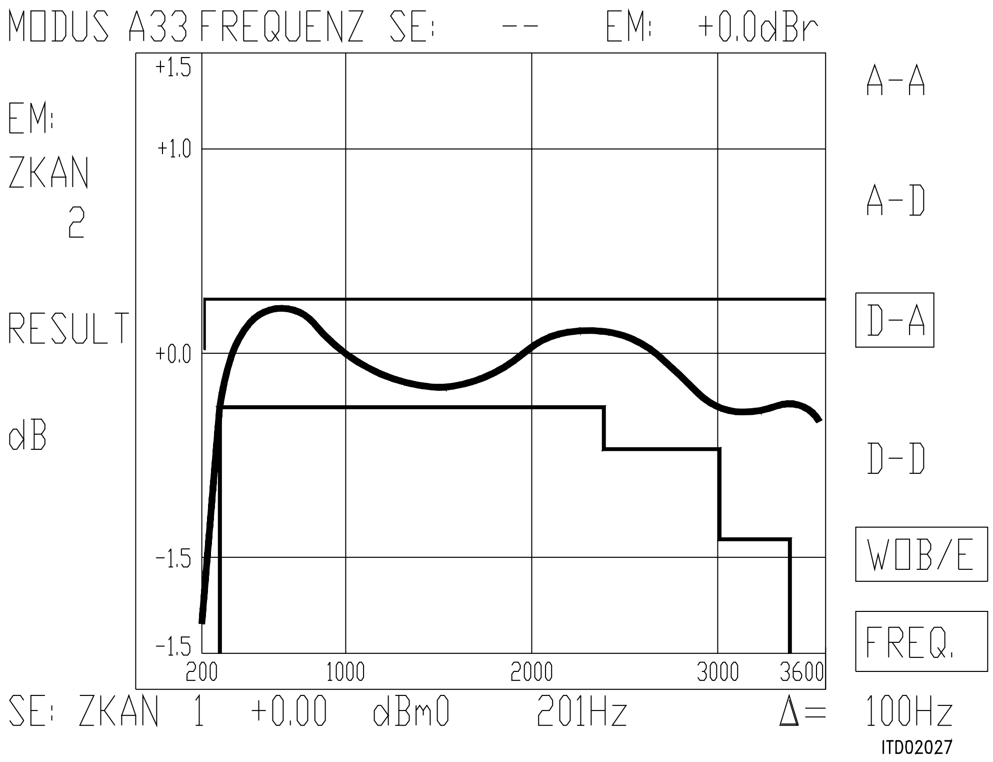


Figure 11

FREQ/Hz	RES/dB	1	FREQ/Hz	RES/dB
201	-1.32		2208	0.09
301	-0.30*		2309	0.09
402	0.00		2409	0.07
502	0.15		2509	0.03
602	0.20		2610	-0.03
703	0.19		2710	-0.09
803	0.15		2811	-0.16
903	0.08		2911	-0.21
1004	0.01		3011	-0.25
1104	-0.06		3112	-0.28
1205	-0.11		3212	-0.27
1305	-0.15		3312	-0.25
1405	-0.17		3413	-0.25
1506	-0.16		3513	-0.30
1606	-0.14			
1706	-0.09			
1807	-0.05			
1907	0.00			
2008	0.05			
2108	0.08			

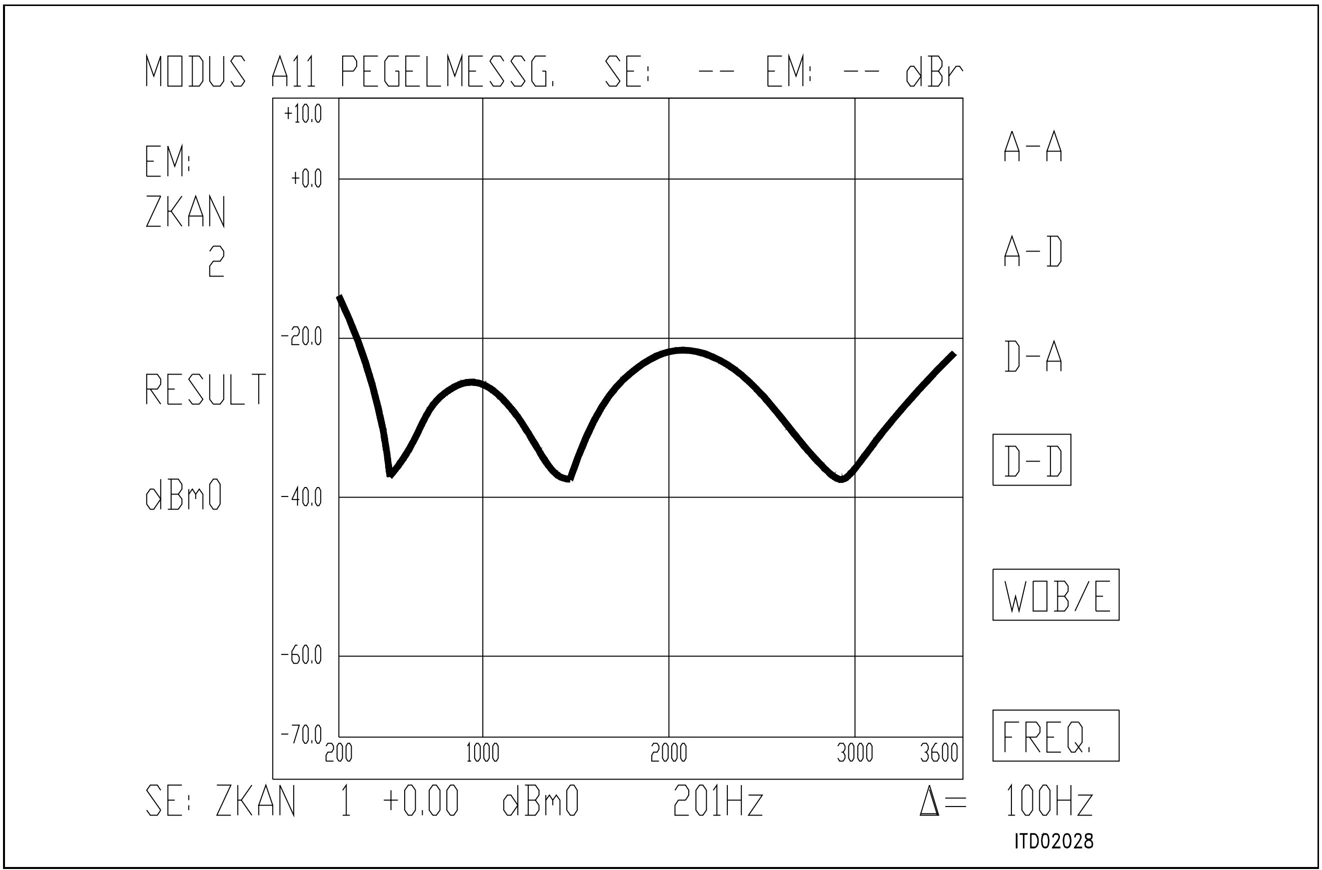


Figure 12

FREQ/Hz	RES/dBm0	FREQ/Hz	RES/dBm0
201	-14.32	2208	-22.65
301	-19.56	2309	-23.55
402	-26.21	2409	-25.00
502	-36.18	2509	-26.98
602	-33.50	2610	-29.40
703	-28.91	2710	-32.46
803	-27.03	2811	-35.77
903	-26.54	2911	-37.64
1004	-27.04	3011	-36.55
1104	-28.52	3112	-34.04
1205	-31.13	3212	-31.04
1305	-34.86	3312	-28.26
1405	-35.41	3413	-25.53
1506	-31.36	3513	-23.16
1606	-27.81		
1706	-25.38		
1807	-23.76		
1907	-22.76		
2008	-22.26		
2108	-22.23		

SICOFI® Application Together with Transformer SLIC with Transverse Feeding

Contents **Page**

1 Introduction

Allthough the trend in Subcriber Line Interface Circuit is to integrate as many functions as possible, transformers are still often used in the design of public or private exchange line cards mainly because of their low cost, high reliability and better symmetry and galvanic separation.

This note describes an application of the Siemens SIgnal COdec FIlter (SICOFI) in a line card equipped with a transformer for the connection of analog subcriber lines.

Terminology:
In the following, we will call "SLIC" the hardware and software corresponding to the analog components in a Subscriber Line Interface Circuit **excluding** the SICOFI chip.

Overview:
This note begins with generalities about SLIC functions.

Then comes an example of solution for the line card circuitry.

The next part is the calculation of the model for the SLIC.

The corresponding software is then described and used in combination with the SICOFI coefficient program.

Measurements show the fulfilment of the German Post specifications. Next comes a word about possible strategies to optimize SICOFI coefficients. In the appendix, the listing of the TRAFO SLIC FORTRAN program (written with **Microsoft** FORTRAN compiler) is given.

2 Generalities

2.1 SLIC Functions

The main functions of the SLIC are to provide the BORSHT functions (**B**attery feeding, **O**vervoltage protection, **R**inging, **S**ignaling, **H**ybrid function, **T**esting). In the case of a SLIC circuit in combination with the SICOFI, the Hybrid function is splitted into the two-wire to four-wire conversion realized by the SLIC and the hybrid balancing provided by the internal B-filter of the SICOFI. The other functions (such as off-hook detection, metering, standby mode, ringing) do not affect the speech signal. Therefore we will not consider these in the scope of this note.

The signal on a telephone line can be considered as comprising of two parts:

- A DC voltage to feed the subcriber terminal.
- An AC voltage (the speech signal) which has to be tranferred in both directions: PABX-line (TRANSMIT) and line-PABX (RECEIVE) with the right attenuation and without distortion.

To separate AC and DC correctly, the circuit has to present a high pass with a very low cut-off frequency and a specified input impedance (matching impedance) in regard to the AC signal. A flat frequency response is also required.

2.2 Principles

Schematic:

A simple SLIC circuit can be schematized as follow:

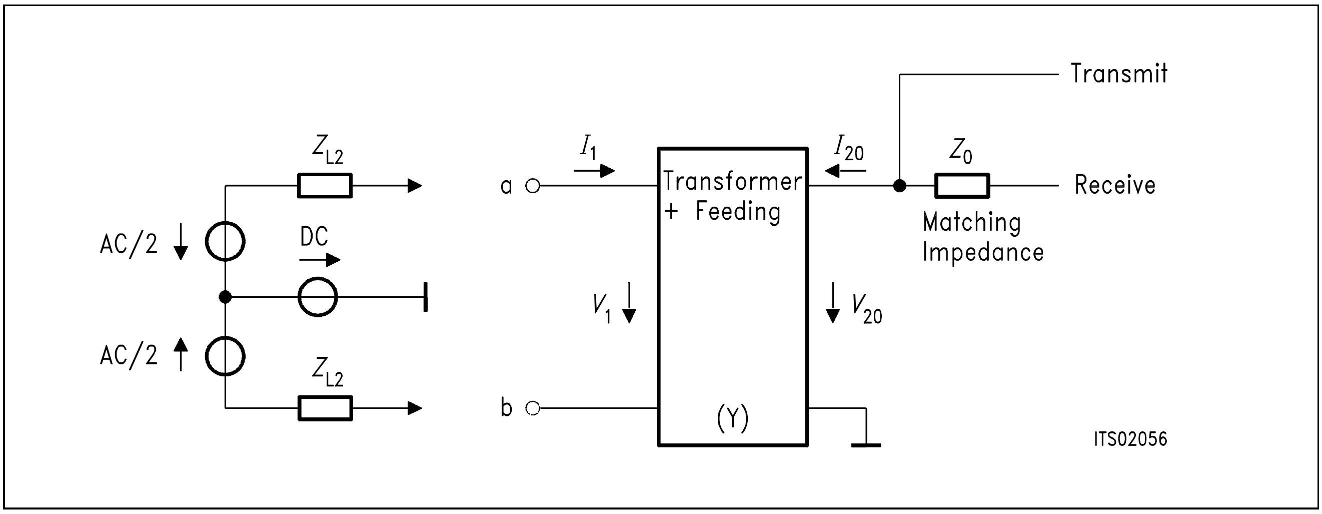


Figure 1

The feeding can be of different kind:

- Series feeding

Transformer: Generally iron core

Advantages:

– The high frequency current is stopped by the coils of the transformer itself.

Drawbacks:

– It is difficult to dimension a transformer with a low leakage inductance.

– High current in the primary half coils.

– A large core is required in order to prevent saturation.

- Parallel feeding

Transformer: Generally ferrite core (allows lower leakage inductance but comes faster in saturation)

Advantages:

– Blocks the DC current before the transformer coils.

Drawbacks:

– Necessity of blocking circuit before the transformer which includes often a large coil or an electronic circuit with problems of non linearities. Therefore the feeding circuit often presents a frequency dependant equivalent impedance which is not easy to model.

2.3 Transformer Characteristics

Philosophy of the simplifications:

Let us take an ideal transformer with 1 to 1 ratio, let us consider the AC signal only and only one direction at a time.

The equivalent circuit in transmit direction will be:

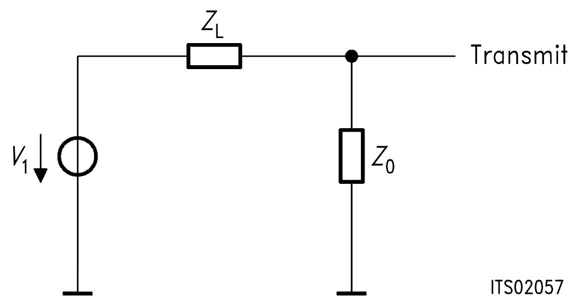


Figure 2

and in receive direction:

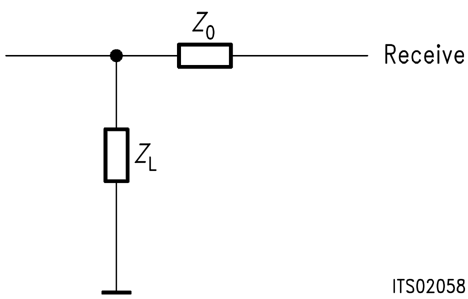


Figure 3

We can see that if $Z_L = Z_0$ the attenuation in both directions is 6 dB.

The real circuit is more complicated because of the loop added by the SICOFI Z-filter and because of the non-ideal transformer.

The SICOFI can drive loads only above typically 300 Ω, so that an opamp is not necessary.

3 Hardware

A transformer SLIC with transverse feeding was choosen with the corresponding T-circuit model with mutual inductance.

3.1 Equivalent Circuit

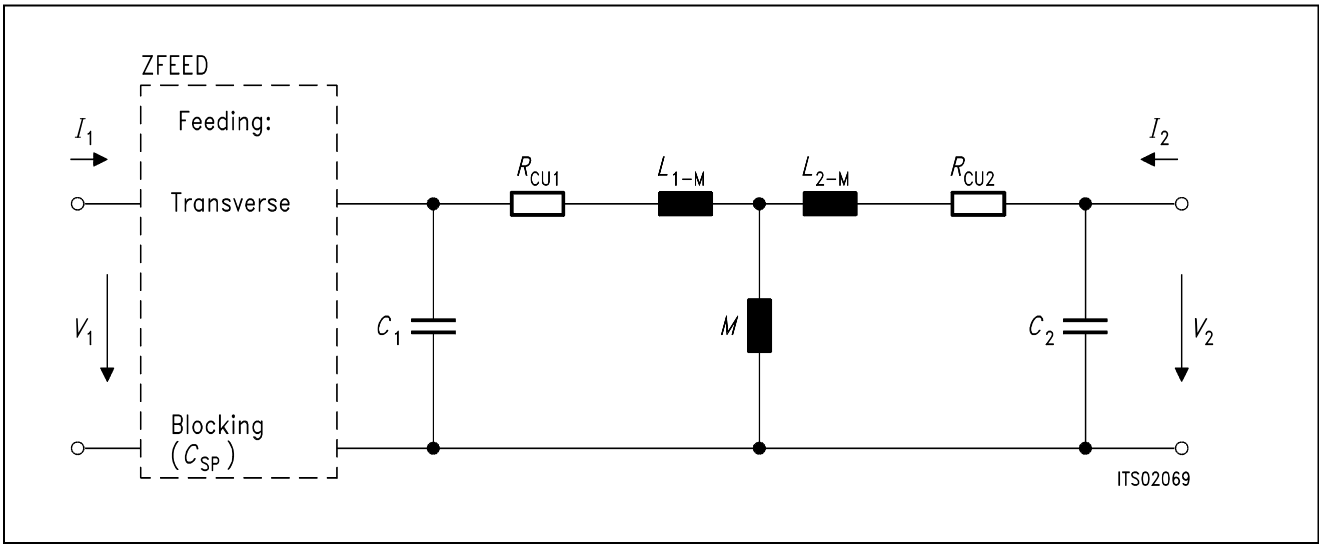


Figure 4

Components of the equivalent circuit:

M	mutual inductance
L_{1s}, L_{2s}	theoretical stray inductances ($L_{1s} = L_1 - M$, $L_{2s} = L_2 - M$)
R_{CU1}, R_{CU2}	primary and secondary resistances
C_{W1}, C_{W2}	primary and secondary winding capacitances
ZFEED	complex feeding impedance

3.2 Measurement Method

The whole measurement occurs in 7 steps:

Step 1: Measurement of the primary and secondary copper resistance with a simple Ohmmeter (R_{CU1} and R_{CU2}).

Step 2: open circuit at the secondary
Measurement of the transformer resonance frequencies by using an impedance analyzer, with **Parallel** equivalent circuit **[P]** or **Series** equivalent circuit **[S]**.

– primary side $\rightarrow f_{01}$ with **[P]** and f_{02} with **[S]**
– secondary side $\rightarrow f_{01}'$ with **[P]** and f_{02}' with **[S]**

Step 3: open circuit at the secondary
Measurement of winding inductance L_{1M} and L_{2M} at low frequency (f_m = 300 Hz) and with **[S]**.

Step 4: Determination of the correction factors n_1 and n_2

with $n_1 = f_m / f_{01}$ and $n_2 = f_m / f_{01}'$

Step 5: Calculation of the actual primary and secondary inductance

$L_1 = L_{1M} (1 - n_1^2)$ and $L_2 = L_{2M} (1 - n_2^2)$

Step 6: short circuit at the secondary
Measurement of the stray inductance L_{1k} at frequency f_{01} with **[S]**

Step 7: Determination of the theoretical mutual inductance M, stray factor s and response ratio

$M = \sqrt{L_2 \times (L_1 - L_{1k})}$ ü $= \sqrt{L_1/L_2}$

$L_{1s} = L_1 - M$ s $= L_{1s}/L_1$

$$C_{W1} = \frac{ü}{(2\pi \times f_{02}')^2 \times L_1 \times s}$$

$$C_{W2} = \frac{1}{(2\pi \times f_{02})^2 \times L_2 \times s \times ü}$$

Results:

In order to prove the capabilities of the SICOFI for Germany with this model, we have choosen a transformer with following data.

R_{CU1} = 84 Ω R_{CU2} = 105 Ω
L_1 = 1.15 H L_2 = 1.15 H
M = 1.148 H
$C_1 = C_{W1}$ = 113 pF $C_2 = C_{W2}$ = 135 pF

3.3 Trafo SLIC Layout

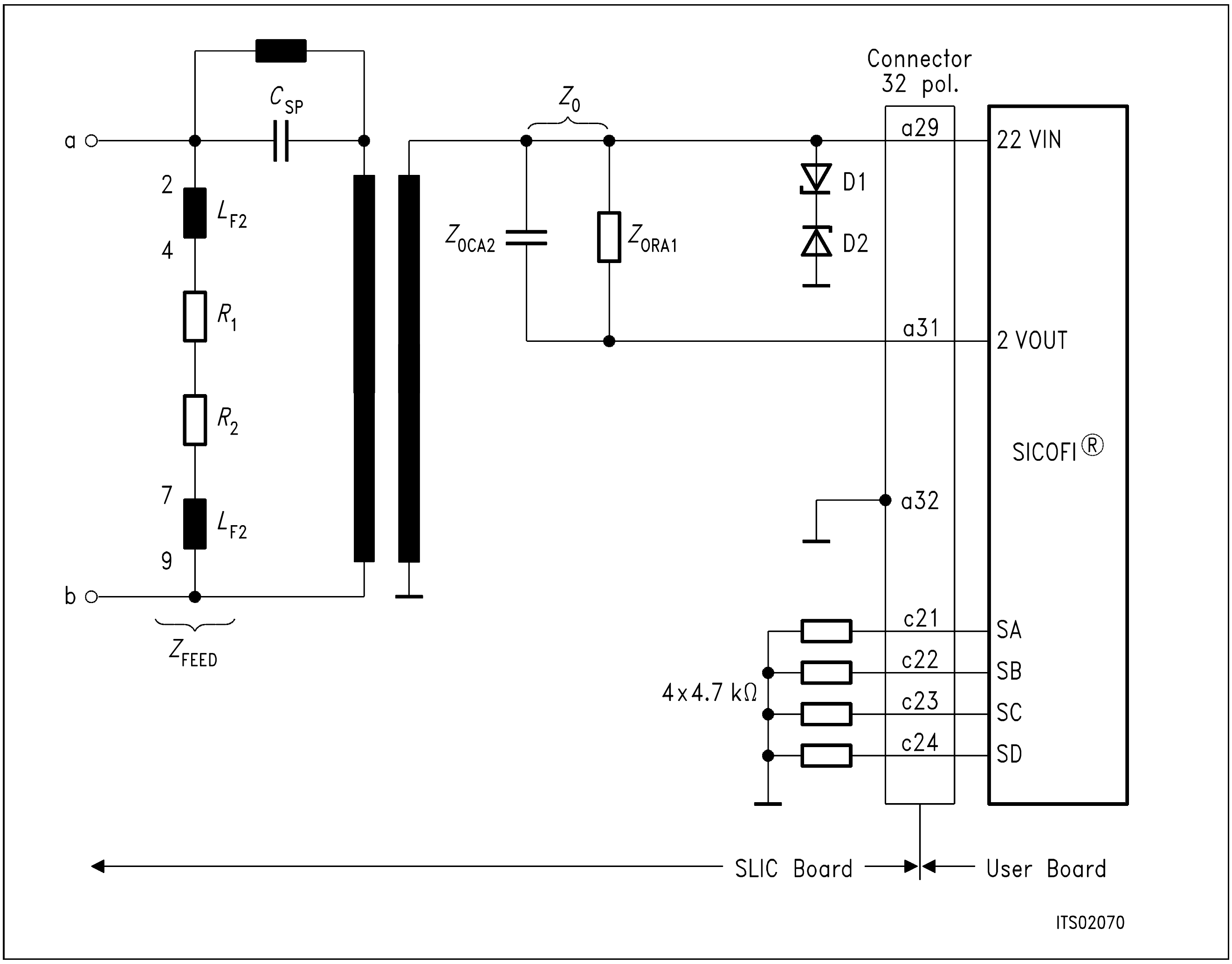


Figure 5

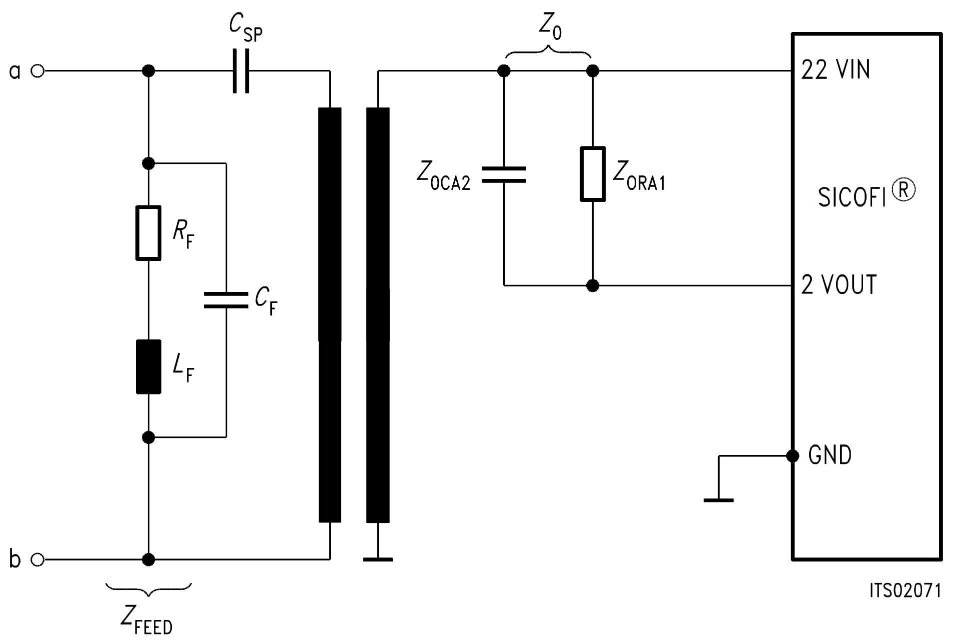


Figure 6

Equivalent Circuit

D1, D2 : Overvoltage protection zener-diodes C2V7
C_{SP} = 1 µF
Z_{0RA1} = 700 Ω
Z_{0CA2} = 0.1 µF
R_F = R_{CU} + R_1 + R_2 = 792 Ω
L_F = 2 H
C_F = 2 nF

R_{CU} is the copper resistor of the coil L_F;

C_F is the stray capacitor of the coil. It is therefore not actually in the layout of the circuit but was measured with the impedance analyser.

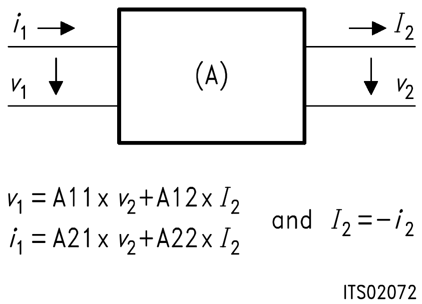
Our circuit is a didactic circuit with a value for Z_0 that has been optimized by trying different resistors and capacitors with a decade in order to obtain an optimal return loss with the SLIC while the Z-filter is switched off.

4 Software

4.1 Introduction

The following two ports model ("black box" which the user can change as he wishes) is used to model the transformer.

Chain matrix:



The model matrix (A-matrix) are used in order to make easy matrix multiplications and improve the modularity of the program.

4.2 Conventions

As we are working with two ports model, we need 2×2 matrixes and because we work with complex numbers, we need a third dimension:

The matrixes are declared as arrays of dimension 3:

A(2,2,2)

where the first number is 1 for real and 2 for imaginary part and the two other ones are for lines and columns of the matrix.

After the multiplications, these matrixes are reduced to their elements (complex):

A11,A12,A21,A22

Example: A12 = A(1,1,2) + j $\times$ A(2,1,2)

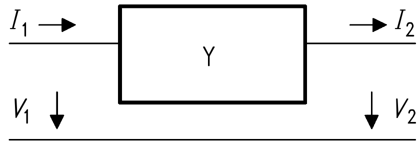
4.3 Subroutines

The transformer is modeled in the subroutine TRSLIC.
The input variable is FREQ (frequency);
Outputs of this routine are the A-parameter of the transformer, including the determinant.
The feeding circuit is modelled in the subroutine ZFEED.

Note: The subroutines TRSLIC and ZFEED have to be modified by the user in order to model his own circuit.

TRSLIC uses subroutines which are the elementary A-matrix calculations:

Subroutine SERA (SERies A-matrix)
Y: admittance in series

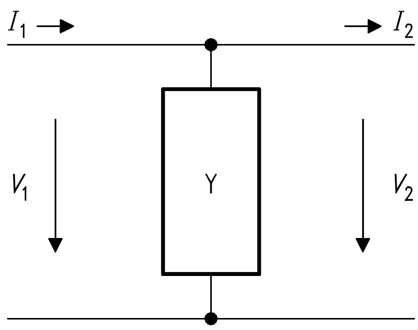


$V_1 = V_2 + I_2 / Y$
$I_1 = I_2$

$$\text{SERA} = \begin{vmatrix} 1 & 1/Y \\ 0 & 1 \end{vmatrix}$$

ITS02073

Subroutine PARA (PARallel A-matrix)
Y: admittance in parallel



$V_1 = V_2$
$I_1 = Y \times V_2 + I_2$

$$\text{PARA} = \begin{vmatrix} 1 & 0 \\ Y & 1 \end{vmatrix}$$

ITS02074

4.4 Model of the Transformer with Transverse Feeding

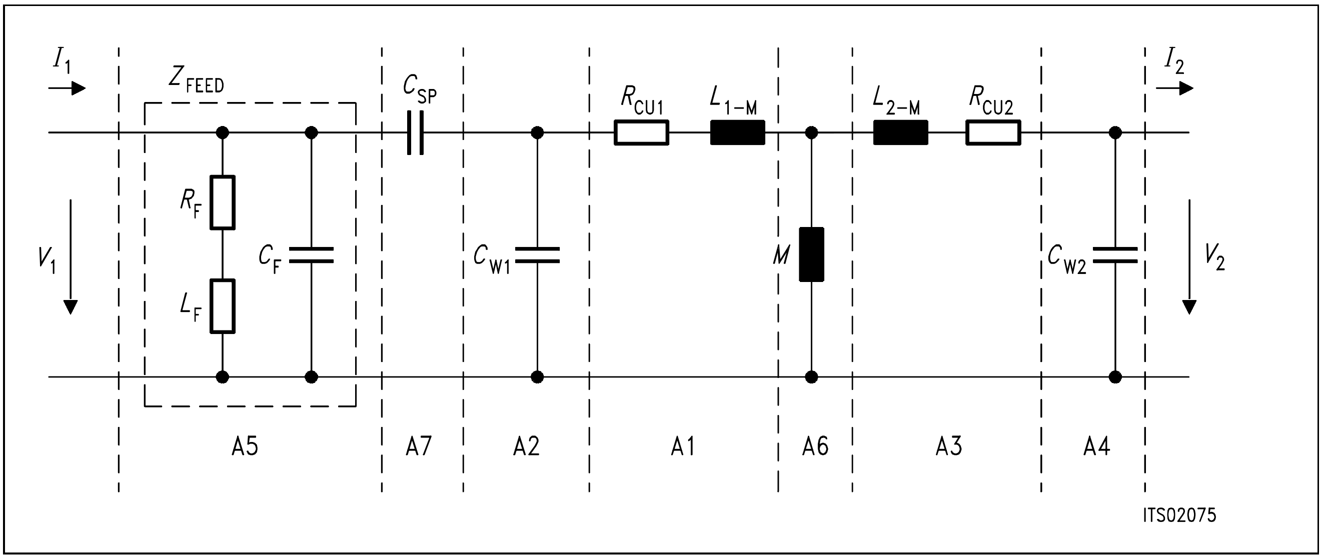


Figure 7

$$A = A5 \times A7 \times A2 \times A1 \times A6 \times A3 \times A4$$

Note: "×" is a complex multiplication: see subroutine CMATMUL

Admittance elements of the different matrixes
$w = 2\pi \times f$
$Y1 = 1 / (R_{CU1} + j \times W \times (L_{1M}))$
$Y2 = j \times 2 \times C_{W1}$
$Y3 = 1 / (R_{CU2} + j \times W \times (L_{2M}))$
$Y4 = j \times W \times C_{W2}$
$Y6 = 1 / j \times W \times M$
here transverse feeding:
$Y5 = 1 / Z_{FEED} = (R_F + (j \times w \times L_F)) \,//\, C_F$
$Y7 = j \times W \times C_{SP}$

4.5 K or M Matrix Calculations

(see the SICOFI program description for the definition of these parameters)

Transformer equations:
(1) $V_1 = A11 \times V_{20} + A12 \times (-I20)$
(2) $I_1 = A21 \times V_{20} + A22 \times (-I20)$
and $ADET = A11 \times A22 - A12 \times A21$
(**see figure 1**)

4.5.1 M-Parameters

The SLIC is described by the following two equations:
I_1 = M11 × V_1 + M12 × V_3
V_2 = M21 × V_1 + M22 × V_3

A. Calculation of M11 Matrix Parameter

M11 = I_1/V_1 when V_3 = 0

This is exactly the admittance Yp seen at the primary side of the transformer when the impedance Z_0 is at the secondary.(*)
Yp = (A21 × Z_0 + A22)/(A11 × Z_0 + A12)

Then:
M11 = (A21 × Z_0 + A22)/(A11 × Z_0 + A12)

B. Calculation of M12 Matrix Parameter

M12 = I_1/V_3 when V_1 = 0

The equations (1) and (2) are now:
(1) – I_{20} = – (A11/A12) × V_{20}
(2) I_1 = A21 × V_{20} + A22 × (– I_{20})

(2) <=> I_1 = A21 × V_{20} + A22 × (– A11/A12)V_{20}
<=> I_1 = – (ADET/A12) × V_{20}

The impedance seen at the secondary side of the transformer when a short circuit is at the primary side is (*):

(3) Z_{OUTt} = A12 / A11
(4) V_{20} / Z_{OUT} = V_3 / (Z_0 + Z_{OUTt}) (voltage divider)

then from (3) and (4):
V_{20} = V_3 × A12 / (A12 + A11 × Z_0)
and with (2):

M12 = I_1/V_3 = – ADET/(A12 + A11 × Z_0)

C. Calculation of M21 Matrix Parameter

M21 = V_2/V_1 when $V_3 = 0$

The relation between V_2 and I_2 is: $V_{20} = -Z_0 \times I_2$
Then by replacing this in (2), we obtain:
$-V_{20} / Z_0 = (-1/A12) \times V_1 + (A11/A12) \times V_{20}$
which is equivalent to:
$V_{20}/V_1 = Z_0 / (A11 \times Z_0 + A12)$

$V_2 = V_{20}$ therefore:

M21 = $Z_0 / (A12 + A11 \times Z_0)$

D. Calculation of M22 Matrix Parameter:

M22 = V_2/V_3 when $V_1 = 0$

The calculations are then straightforeward:

$V_2/V_3 = (Z_{eq} / Z_{eq} + Z_0)$

Z_{eq} is the impedance seen at the secondary side of the transformer when there is a short circuit at the primary.(*)
$Z_{eq} = A12 / A11$
Then:

M22 = $V_2/V_3 = 1 / (1 + Z_0 \times (A11/A12))$

4.5.2 K-Parameters

These parameters are easier to measure than the M-parameters but the calculations necessitate the knowledge of the generator impedance Z_g and of the generator voltage V_g.

The SLIC is described by the following two equations:
b1 = $K11 \times a1 + K12 \times V_3$
$V_2 = K21 \times a1 + K22 \times V_3$

with a1 = $V_1 - Z_g \times I_1$
b1 = $V_1 + Z_g \times I_1$
and (4) $V_1 = V_g - Z_g \times I_1$

A. Calculation of K11 Matrix Parameter

K11 = b1/a1 when $V_3 = 0$

K11 = $(Z_{IN} - Z_g) / (Z_{IN} + Z_g)$

with Z_{IN}: admittance seen at the primary side of the transformer when the impedance Z_0 is at the secondary.(*)
$Z_{IN} = (A11 \times Z_0 + A12) / (A12 \times Z_0 + A22)$

Note: The return loss (RL) is defined by:
RL = $-20 \times \log10(| (Z_{IN} + Z_g) / (Z_{IN} - Z_g) |)$
that is:
RL = $20 \times \log10(|K11|)$

B. Calculation of K12 Matrix Parameter

K12 = $2 \times V_1/V_3$ when a1 = 0

The equations (1) and (2) are now:

(1) $V_1 = A11 \times V_{20} + A12 \times (-I_{20})$
(2) $I_1 = A21 \times V_{20} + A22 \times (-I_{20})$
(3) $V_3 = V_{20} + Z_0 \times I_{20}$
(4) $V_1 = -Z_g \times I_1$

(3) $\Leftrightarrow V_{20} = V_3 - Z_0 \times I_{20}$
by reporting in (1) and (2):
(5) $V_1 = A11 \times (V_3 - Z_0 \times I_{20}) - A12 \times I_{20}$
(6) $I_1 = A21 \times (V_3 - Z_0 \times I_{20}) - A22 \times I_{20}$

by combination of (4), (5) and (6):

$$V_1/V_3 = \frac{(A22 + A11 \times Z_0) + (1/Z_g) \times (A12 + A11 \times Z_0)}{A11(A22 + A21 \times Z_0) - A21 \times (A12 + A11 \times Z_0)}$$

then

$$V_1/V_3 = \frac{2 \times ADET \times Z_g}{Z_g \times (A22 + A21 \times Z_0) + (A12 + A11 \times Z_g)}$$

C. Calculation of K21 Matrix Parameter

K21 = V_2 / V_g when $V_3 = 0$

The equations are now:

$V_2 = V_{20}$
$I_2 = I_{20}$
$V_{20} = - Z_0 \times I_{20}$
(1) $V_1 = A11 \times V_{20} - A12 \times I_{20}$
(2) $I_1 = A21 \times V_{20} - A22 \times I_{20}$
(4) $V_g - V_1 = Z_g \times I_1$

the relation between V_2 and I_2 is:

$V_{20} = - Z_0 \times I_{20}$

replacing (4) in (1) and (2):

(1) $V_g - Z_g \times I_1 = A11 \times V_{20} - A12 \times I_{20}$
(2) $I_1 = A21 \times V_{20} - A22 \times I_{20}$

by combination:

$V_g = (A11 + Z_g \times A21) \times V_{20} + (A12 + A22 \times Z_g) \times (- I_{20})$

and by replacing I_{20}:

$$V_2/V_g = \frac{Z_0}{(A11 + A21 \times Z_g) \times Z_0 + A12 + Z_g \times A22}$$

D. Calculation of K22 Matrix Parameter

K22 = V_2/V_3 when a1 = 0

The equations are now:

$V_2 = V_{20}$
$I_2 = I_{20}$
$V_{20} = - Z_0 \times I_{20}$
(1) $V_1 = A11 \times V_{20} - A12 \times I_{20}$
(2) $I_1 = A21 \times V_{20} - A22 \times I_{20}$
(4) $V_g - V_1 = Z_g \times I_1$

The calculations are then straightforeward:

$V_2/V_3 = (Z_{eq} / (Z_{eq} + Z_0))$

Z_{eq} is the impedance seen at the secondary side of the transformer when there is a short circuit at the primary.(*)

$Z_{eq} = (A22 \times Z_g + A12) / (A11 + A21 \times Z_g)$

Then:

$$K22 = V_2/V_3 = \frac{(A22 \times Z_g + A12)}{(A22 \times Z_g + A12) + Z_0 \times (A11 + Z_g \times A21)}$$

Summary:

$$M11 = (A21 \times Z_0 + A22) / (A11 \times Z_0 + A12)$$

$$M12 = – ADET / (A12 + A11 \times Z_0)$$

$$M21 = Z_0 / (A12 + A11 \times Z_0)$$

$$M22 = A12 / (A12 + Z_0 \times A11)$$

$$K11 = (Z_{IN} – Z_g) / (Z_{IN} + Z_g)$$

with $Z_{IN} = (A21 \times Z_0 + A22) / (A11 \times Z_0 + A12)$

$$K12 = \frac{2 \times ADET \times Z_0}{Z_g \times (A22 + A21 \times Z_0) + (A12 + A11 \times Z_0)}$$

$$K21 = \frac{Z_0}{(A11 + A21 \times Z_g) \times Z_0 + A12 + Z_g \times A22}$$

$$K22 = \frac{(A22 \times Z_g + A12)}{(A22 \times Z_g + A12) + Z_0 \times (A11 + Z_g \times A21)}$$

Schematic circuit diagram of transformer SLIC software:

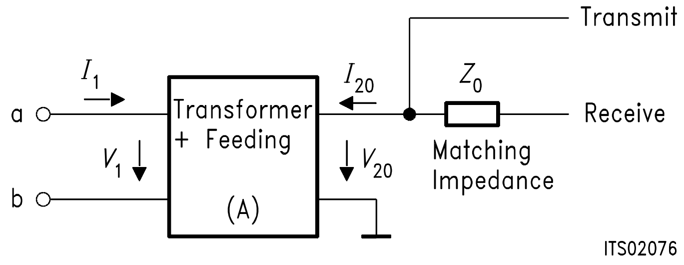


Figure 8

Note:* Each block is modifyable by the user.

Impedances

The matching impedance Z_0 and the generator impedance are modeled with 6 parameters:
Example:
Z_{0R1},Z_{0C1},Z_{0R2},Z_{0C2}: parallel part
Z_{0RS},Z_{0CS}: serial part

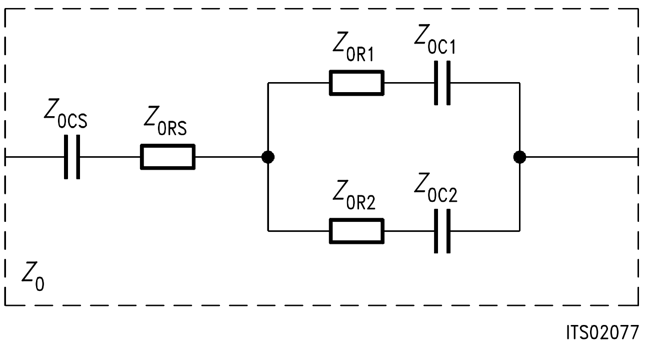


Figure 9

5 Optimization

5.1 Input Data

The TRAFOT SLIC program (written with Microsoft FORTRAN compiler) needs an input file which contains the data for the SLIC:

TRAFOT.INP:

```
* PARAmeter (K[default] or M)
K
*RCU1     *RCU2        :copper resistor of primary (resp. secondary)
 84.       105.
*CW1,     *CW2         :winding capacitors primary and secondary
1.135E-10  135.4E-12
*LS1      *LS2     *M  :leaking inductances primary and secondary
 1.15      1.15     1.148
*CSP                   :blocking capacitor
  1.E-6
*RF       *LF     *CF  :feeding ( cannot be all 0 at the same time)
 792.      2.23    2.67E-9
*ZSLI                  :worst case half loop
0.5
*Z0 : matching impedance  (with 6 elemnts )
*Z0RA1, Z0CA1, Z0CA2, Z0RA2, Z0RS , Z0CS
 700.    0.    .1E-6    0.     0.     0.
*Zg : source/line impedance  (with 6 elements )
*ZgRA1, ZgCA1, ZgCA2, ZgRA2, ZgRS, ZGCS
820.    0.   115.E-09   0.   220.  0.
```

5.2 Runs

Specifications:

The .SPE file needed by the SICOFI coefficient program makes use of values based on the specifications for West-Germany (see BRD.SPE in appendix A1). A first run with automatical Z-filter optimization (PZIN=0) does not give satisfying results for the return loss.

A second run with modified specifications (see BRD2.SPE in appendix A1) is necessary with repetition of the Z-filter optimization (ZREP=Y).

Result file:

The corresponding result file TRAFOT.RES can be found in appendix A3.

6 Measurements

Measurements are made with a "PCM4" from Wandel & Goltermann. The specifications for West-Germany are fulfilled.

We have measured the return loss, the (attenuation in) transmit direction (AD), the attenuation in the receive direction (DA), the attenuation distortion (AD and DA) and the transhybrid loss (DD).

Correlation

The correlation between the calculated values and the measured values for return loss (all filters off and calculated values with the "Sim"-function of the SICOFI program) can be seen in the last diagram of appendix A2. The lower line in the picture stands for the calculated values.

7 Strategies

The SICOFI makes it possible to use the same hardware for different country specifications by changing the programming of the SICOFI.

In general, it is necessary to allready have a good return loss with the transformer alone without SICOFI. Then SICOFI improves the figures.

This requires us however to optimize the SLIC circuitry in four steps using the SICOFI program as an simulation tool (especially Z-filter optimization):

1. Set Z_0 to a given value

2. Run automatical Z-filter optimization for the given Z_0 impedance and for all the specifications.

3. Change the impedance Z_0

4. Redo step 1 until having obtained an optimal return loss.

Appendix A1

Specifications

BRD.SPE

```
FREF = 1014.0    LAW = A
UREF = 0.9480    RLX = 0.    RLR =    -7.0
ABIMP  = ZI
ERZI= 1  RSER=  220.     RPAR=  820.     CPAR= 0.115E-06
ERZL= 1  RSL =  220.     RPL =  820.     CPL = 0.115E-06

ZIN
FR            300         500       3k       3.4k
AT-           0          20        20       16
AT+           16          20        20       0

ZMIR
FR            4k        12k
AT-            30         3
AT+           30         3

DA,UPPER
FR          300   500     2.7k      3k       3.4k
AT-         100   .75     .25       .35      .75
AT+         .75   .25     .35       .75      100

DA,LOWER
FR          300         3.4k
AT-         0           -.25
AT+         -.25         0

DA,DELAY
FR            500       600       1k        2.6k    2.8k
GD-           10K      .420       .150      .085    .150
GD+          .420      .150       .085      .150    10k

AD,UPPER
FR          300    500    2.7k     3k        3.4k
AT-         100   .75     .25      .35       .75
AT+         .75   .25     .35      .75       100

AD,LOWER
FR          300         3.4k
AT-         0           -.25
AT+         -.25         0

AD,DELAY
FR           500      600       1k        2.6k    2.8k
GD-          10k      .420      .150      .085    .150
GD+          .420     .150      .085      .150    10k
DD
FR            300        500      2.5k         3.4k
AT-           0          27       27           23
AT+          23          27       27           0
```

BRD.SPE

```
FREF = 1014.0   LAW = A
UREF = 0.9480   RLX = 0.    RLR =    -7.0
ABIMP  = ZI
ERZI= 1  RSER=  220.     RPAR=  820.     CPAR= 0.115E-06
ERZL= 1  RSL =  220.     RPL =  820.     CPL = 0.115E-06

ZIN
FR            300         500         3K        3.4k
AT-           0           20          20        20
AT+           16          20          20        0

ZMIR
FR            4k         12k
AT-           30          3
AT+           30          3

DA,UPPER
FR          300   500     2.7k      3k         3.4k
AT-         100   .75     .25       .35        .75
AT+         .75   .25     .35       .75        100

DA,LOWER
FR          300         3.4k
AT-         0           -.25
AT+         -.25         0

DA,DELAY
FR           500         600         1k         2.6K    2.8k
GD-          10K        .420        .150        .085    .150
GD+          .420       .150        .085        .150    10K

AD,UPPER
FR          300    500    2.7k      3k        3.4k
AT-         100    .75   .25        .35       .75
AT+         .75    .25   .35        .75       100

AD,LOWER
FR          300        3.4k
AT-         0          -.25
AT+         -.25        0

AD,DELAY
FR           500       600       1k        2.6k    2.8k
GD-          10k      .420       .150      .085    .150
GD+          .420     .150       .085      .150    10k
DD
FR            300        500         2.5k     3.4k
AT-           0          29          29       23
AT+          23          29          29       0
```

Appendix A2

Measurements

Note: The masks on the plots corresponds to CCITT Recommendations G.712 and G.714

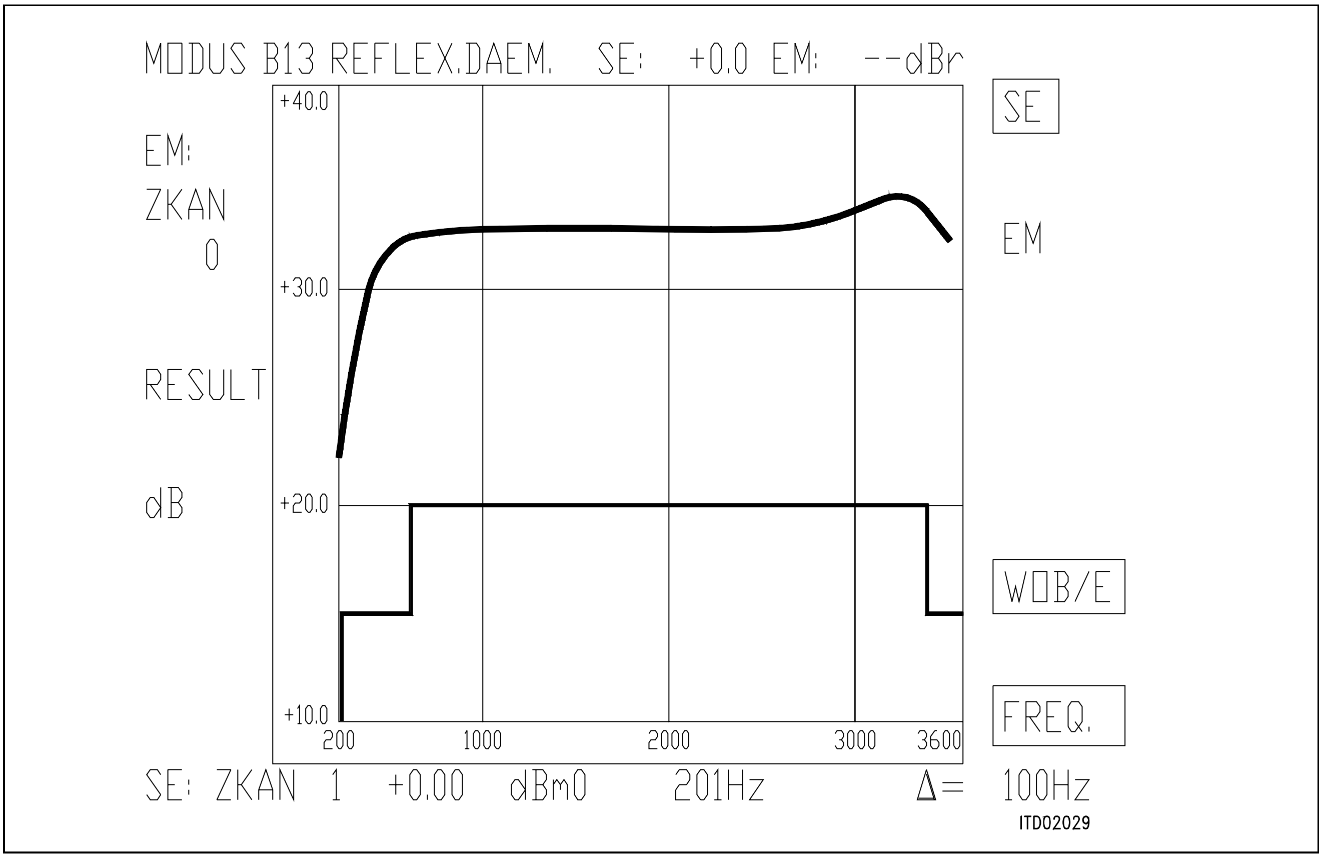


Figure 10

FREQ/Hz	RES/dBm0	1	FREQ/Hz	RES/dBm0
201	22.10		2208	32.77
301	28.28		2309	32.69
402	31.08		2409	32.65
502	32.02		2509	32.67
602	32.34		2610	32.76
703	32.50		2710	32.91
803	32.65		2811	33.14
903	32.80		2911	33.43
1004	32.96		3011	33.74
1104	33.11		3112	34.03
1205	33.26		3212	34.18
1305	33.37		3312	34.05
1405	33.45		3413	33.55
1506	33.48		3513	32.66
1606	33.46			
1706	33.39			
1807	33.29			
1907	33.16			
2008	33.02			
2108	32.89			

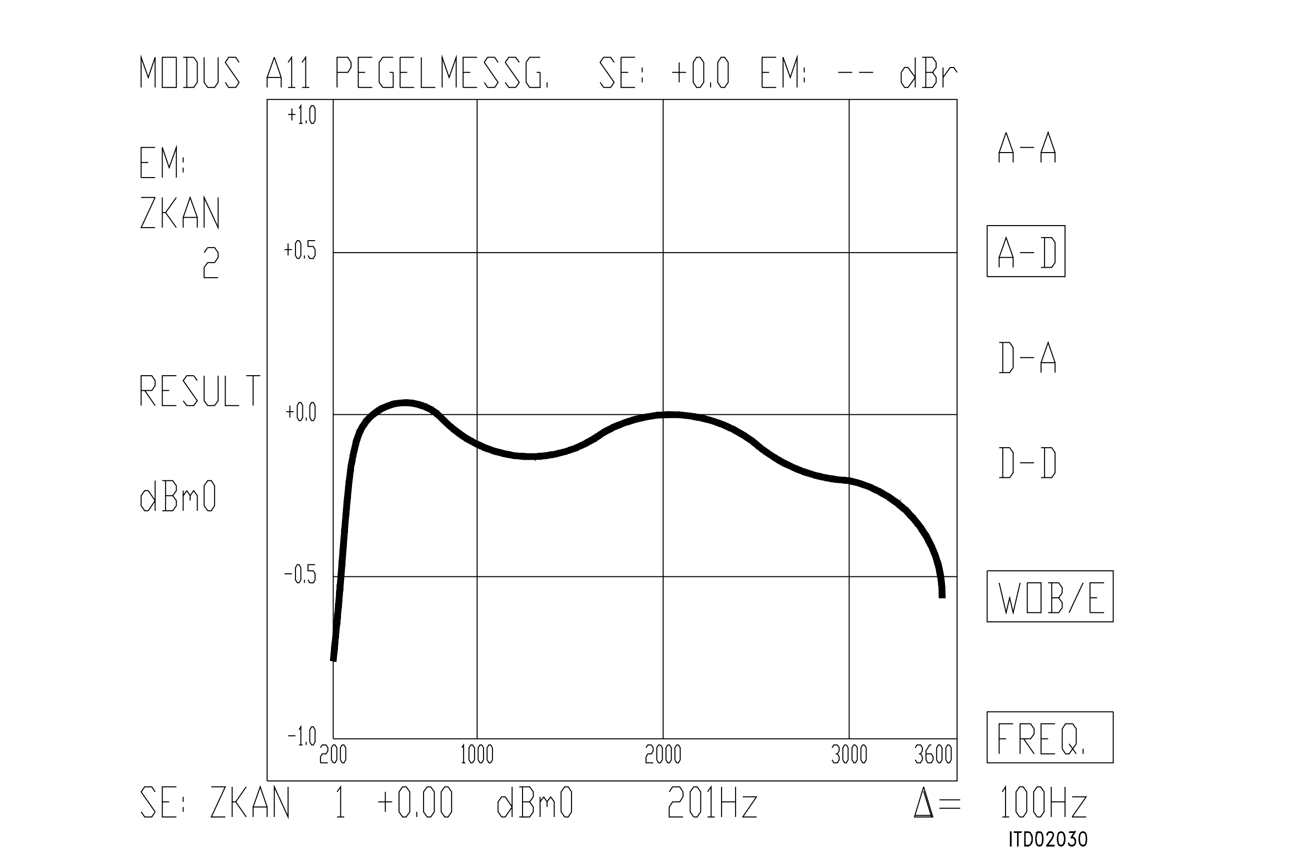


Figure 11

FREQ/Hz	RES/dBm0	1	FREQ/Hz	RES/dBm0
201	-0.72		2208	-0.01
301	-0.05		2309	-0.02
402	-0.01		2409	-0.04
502	-0.03		2509	-0.08
602	-0.04		2610	-0.13
703	-0.01		2710	-0.16
803	-0.02		2811	-0.18
903	-0.06		2911	-0.19
1004	-0.11		3011	-0.20
1104	-0.14		3112	-0.21
1205	-0.15		3212	-0.24
1305	-0.15		3312	-0.28
1405	-0.15		3413	-0.36
1506	-0.12		3513	-0.58
1606	-0.09			
1706	-0.06			
1807	-0.04			
1907	-0.01			
2008	-0.01			
2108	-0.00			

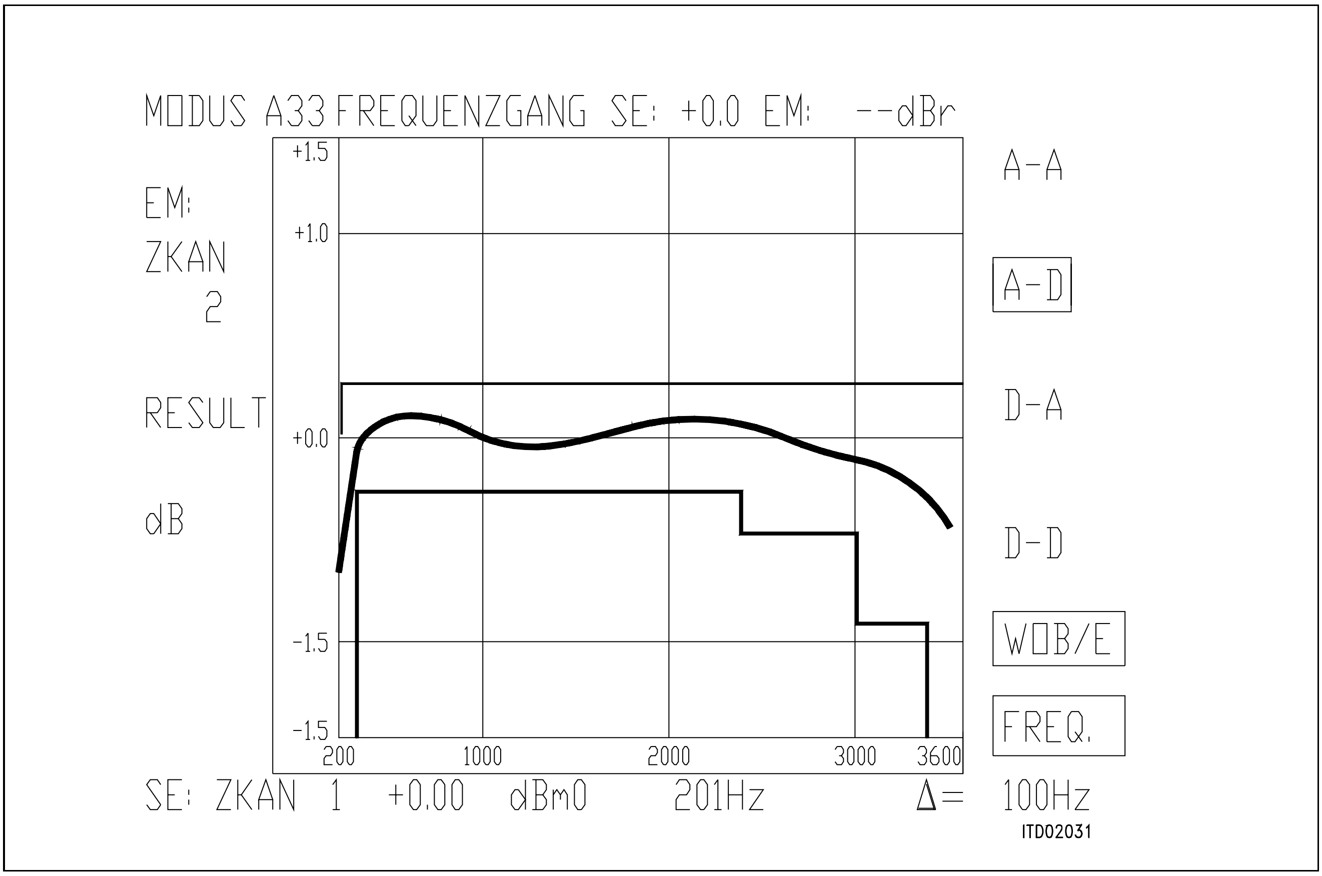


Figure 12

FREQ/Hz	RES/dBm	1	FREQ/Hz	RES/dBm
201	-0.65		2208	-0.09
301	0.04		2309	-0.07
402	0.09		2409	-0.05
502	0.12		2509	-0.02
602	0.12		2610	-0.00
703	0.10		2710	-0.04
803	0.07		2811	-0.06
903	0.03		2911	-0.09
1004	0.00		3011	-0.11
1104	-0.03		3112	-0.13
1205	-0.04		3212	-0.14
1305	-0.04		3312	-0.19
1405	-0.02		3413	-0.26
1506	0.00		3513	-0.43
1606	0.02			
1706	0.04			
1807	0.06			
1907	0.09			
2008	0.10			
2108	0.09			

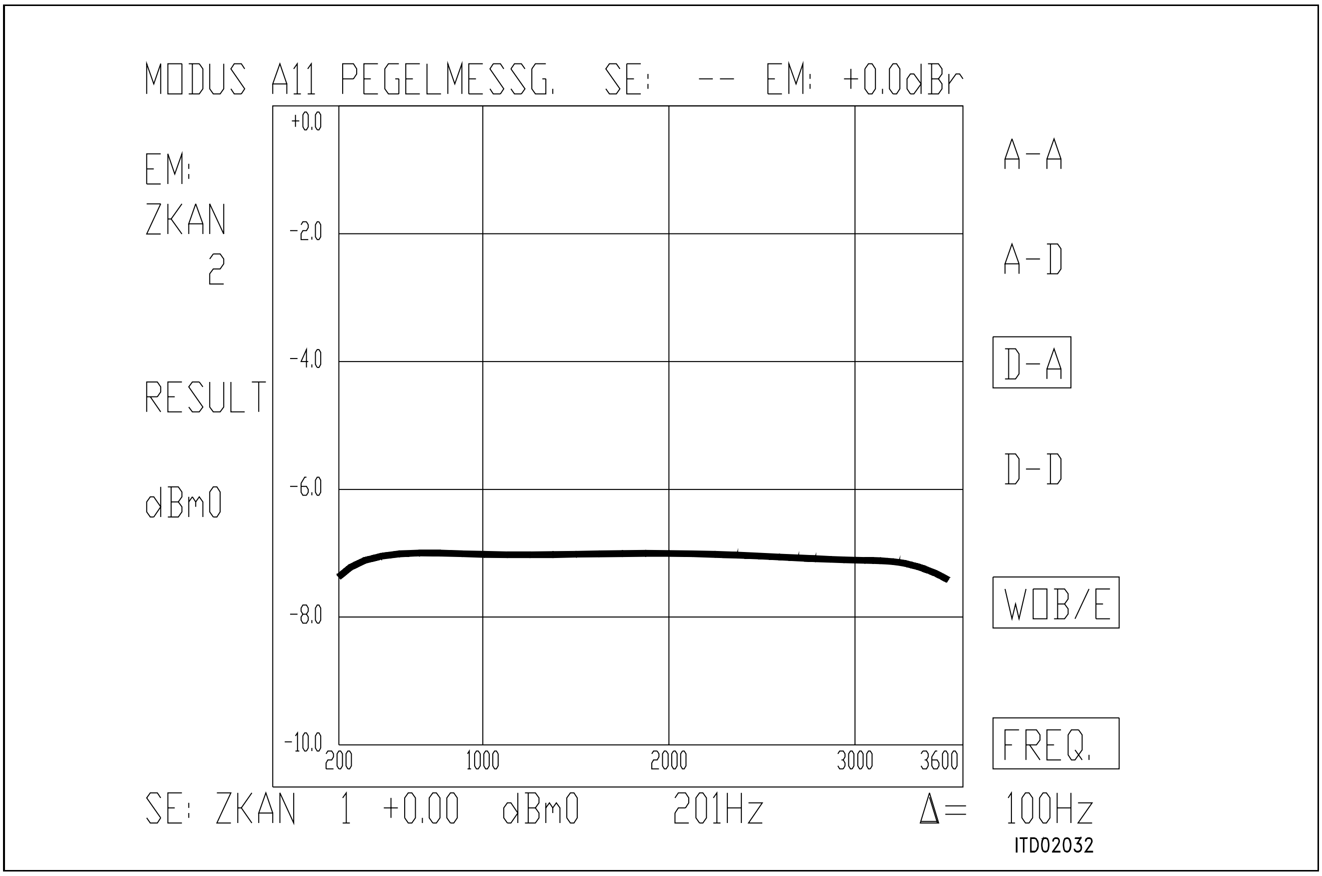


Figure 13

FREQ/Hz	RES/dBm0	1	FREQ/Hz	RES/dBm0
201	-7.36		2208	-6.94
301	-7.00		2309	-6.95
402	-6.93		2409	-6.98
502	-6.91		2509	-7.00
602	-6.91		2610	-7.03
703	-6.94		2710	-7.05
803	-6.97		2811	-7.07
903	-7.00		2911	-7.09
1004	-7.02		3011	-7.11
1104	-7.03		3112	-7.12
1205	-7.03		3212	-7.14
1305	-7.02		3312	-7.18
1405	-7.01		3413	-7.26
1506	-6.99		3513	-7.42
1606	-6.97			
1706	-6.95			
1807	-6.93			
1907	-6.92			
2008	-6.92			
2108	-6.93			

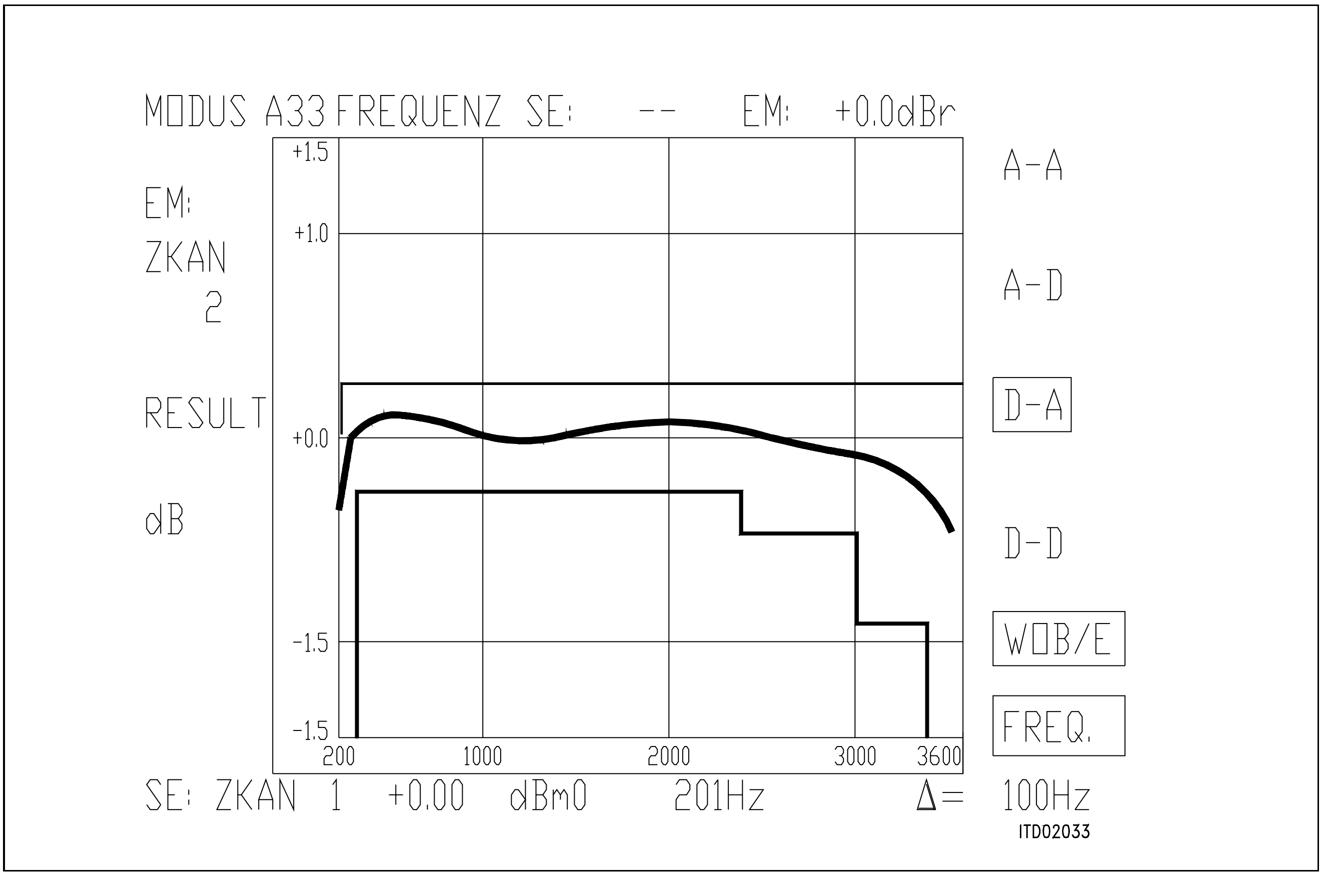


Figure 14

FREQ/Hz	RES/dBm	1	FREQ/Hz	RES/dBm
201	-0.36		2208	0.08
301	0.01		2309	0.06
402	0.09		2409	0.03
502	0.11		2509	0.01
602	0.11		2610	-0.02
703	0.08		2710	-0.05
803	0.05		2811	-0.07
903	0.02		2911	-0.08
1004	0.00		3011	-0.10
1104	-0.01		3112	-0.11
1205	-0.01		3212	-0.13
1305	-0.01		3312	-0.17
1405	0.01		3413	-0.26
1506	0.03		3513	-0.41
1606	0.05			
1706	0.07			
1807	0.08			
1907	0.09			
2008	0.09			
2108	0.09			

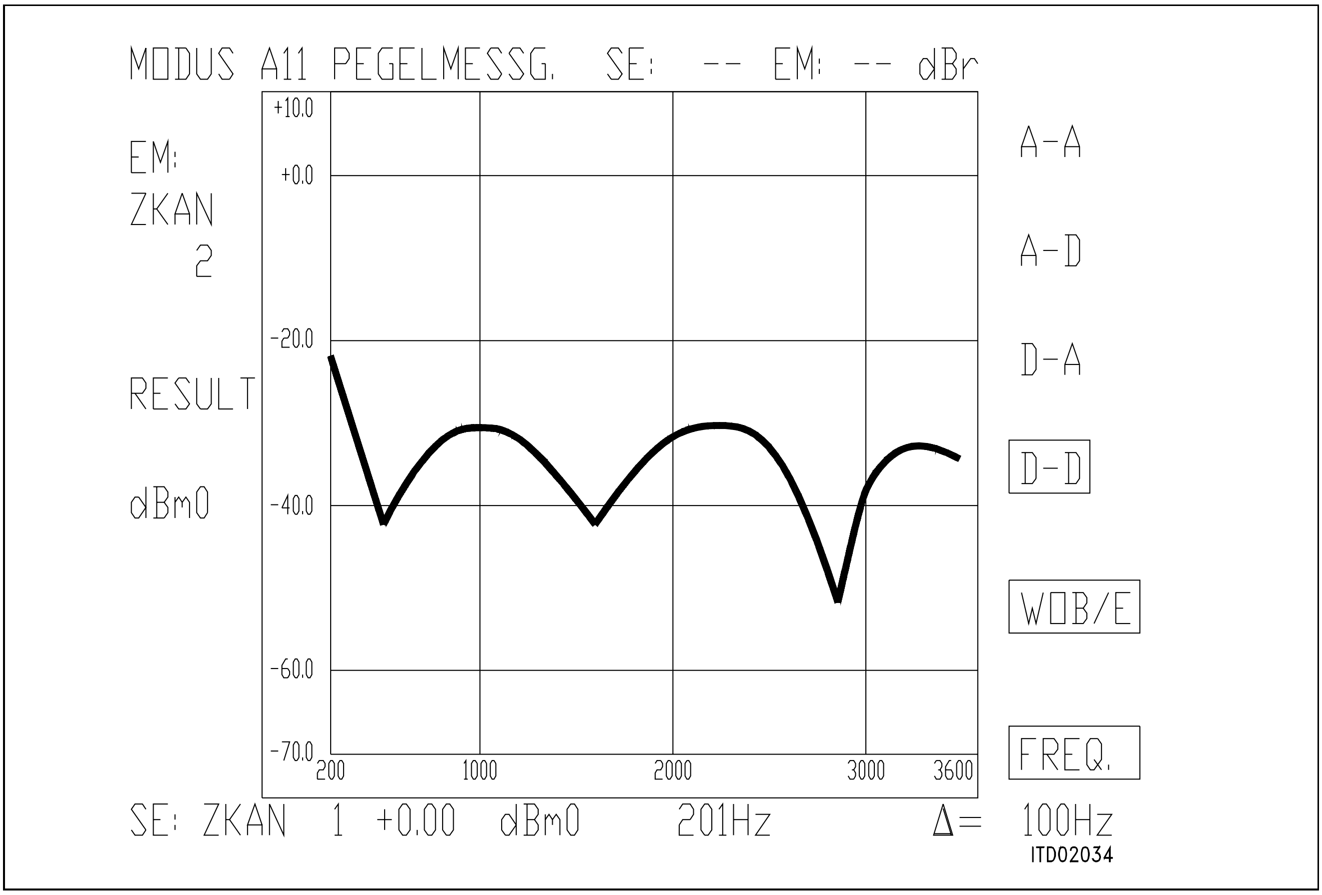


Figure 15

FREQ/Hz	RES/dBm0	1	FREQ/Hz	RES/dBm0
201	-22.83		2208	-29.72
301	-28.06		2309	-29.91
402	-34.42		2409	-30.72
502	-41.08		2509	-32.26
602	-36.73		2610	-34.98
703	-33.12		2710	-39.64
803	-31.24		2811	-50.70
903	-30.36		2911	-43.61
1004	-30.17		3011	-37.18
1104	-30.58		3112	-33.95
1205	-31.56		3212	-32.40
1305	-33.20		3312	-32.05
1405	-35.67		3413	-32.50
1506	-39.10		3513	-33.51
1606	-41.22			
1706	-38.35			
1807	-35.00			
1907	-32.63			
2008	-31.05			
2108	-30.09			

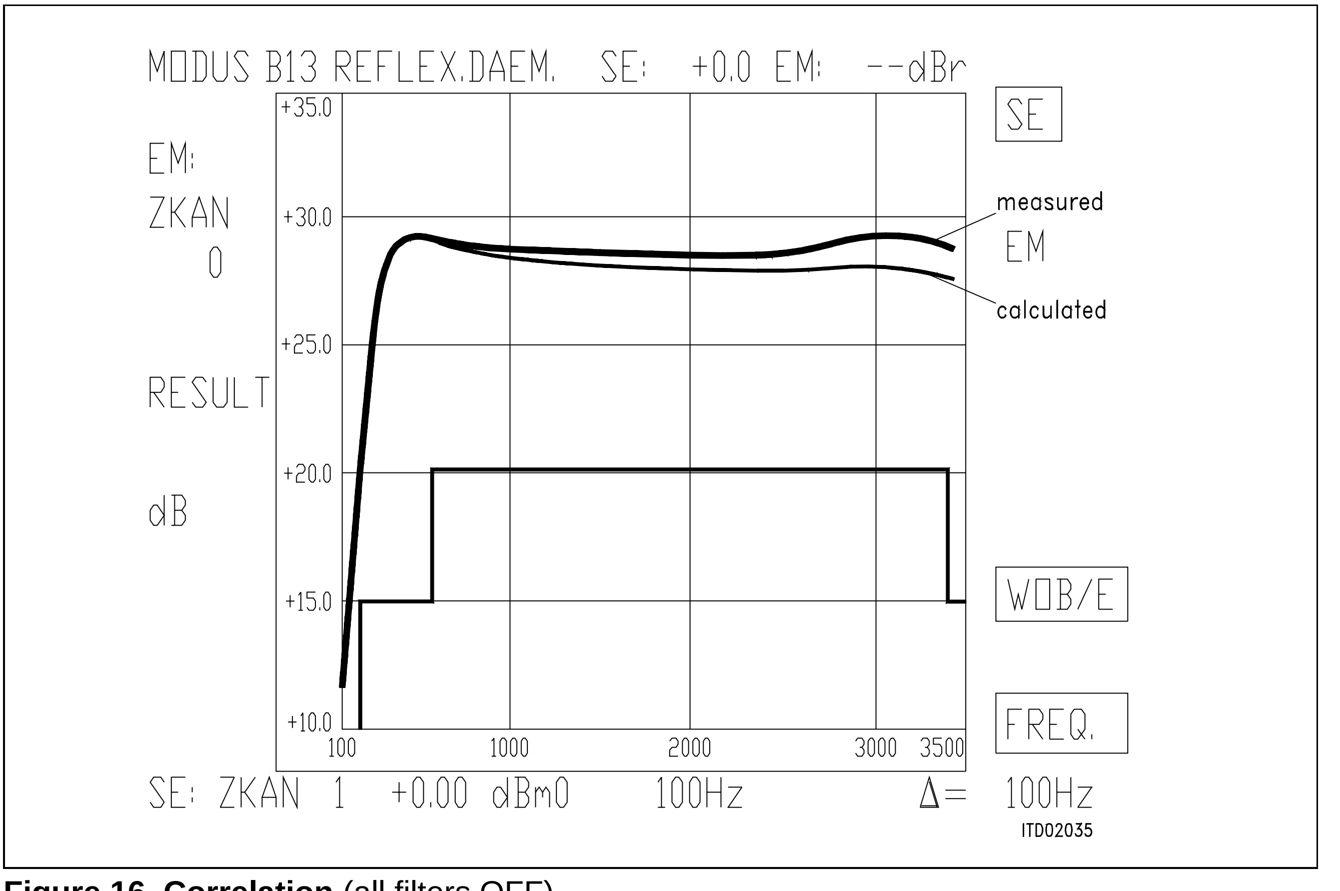


Figure 16 Correlation (all filters OFF)

FREQ/Hz	RES/dBm	FREQ/Hz	RES/dBm
100	12.10	2108	28.28
201	20.35	2208	28.38
301	25.27	2309	28.49
402	27.73	2409	28.62
502	28.85	2509	28.75
602	29.25	2610	28.87
703	29.31	2710	28.98
803	29.19	2811	29.07
903	29.01	2911	29.13
1004	28.82	3011	29.17
1104	28.63	3112	29.14
1205	28.47	3212	29.08
1305	28.31	3312	28.95
1405	28.21	3413	28.77
1506	28.13		
1606	28.09		
1706	28.07		
1807	28.09		
1907	28.13		
2008	28.19		

Appendixes A3

Result File TRAFOT.RES

```
 Input_file_name: TRAFOT.CTL             Date:  11.08.88  13:35
SPEC = BRD2.SPE                          SLIC = TRAFOT.SLI
BYTE = REF.BYT      CHNR = 0,A
PLQ = N

ON = ALL                      REL = Y                    SHORT = N
OPT =  Z+X+R+B                ZXRB = NNNN
        PZIN= 0          PSP = 0
   FZ =  300.00        3400.0       ZLIM =  2.00
ZREP  =Y                               ZSIGN =  1
  FR =   300.00        3400.0
RFIL =  Y              RREFQ = N      RREF =  .66179
  FX =   300.00        3400.0
XFIL =  Y              XREFO = N      XREF = -.13731
  FB =   300.00        3400.0       BLIM =  2.00 TBM =  1
BREP = N                               BSIGN =  1
APOF =   .00     DPOF =   .00     APRE =   .00     DPRE =   .00
XZQ =   -.108886718750000000E+00    .289062500000000000E+00
         .634765625000000000E-02   -.304687500000000000E+00
         .195312500000000000E+00
XRQ =    .967773437500000000E+00   -.488281250000000000E-01
        -.145263671875000000E-01   -.488281250000000000E-03
         .903320312500000000E-02
XXQ =    .101757812500000000E+01    .150756835937500000E-01
         .114746093750000000E-01    .341796875000000000E-02
         .973510742187500000E-02
XBQ =    .210937500000000000E+00    .343750000000000000E+00
         .254150390625000000E+00   -.121582031250000000E+00
        -.957031250000000000E-01
         .152343750000000000E+00    .178222656250000000E-01
        -.187988281250000000E+00    .183593750000000000E+00
        -.859375000000000000E-01
XGQ =    .534912109375000000E+00    .211718750000000000E+01
;

Bytes for Z-Filter (13):             20,BA,2A,7B,1B,32,B2,5B
Bytes for R-Filter (2B):             70,23,8F,EC,3C,AC,0B,5D
Bytes for X-Filter (23):             70,E2,97,73,C1,D6,03,36
Bytes for Gain-factors (30):         41,C3,00,C3
2nd part of bytes B-Filter (0B):     00,2C,31,C1,AA,6F,33,23
1st part of bytes B-Filter (03):     BB,CA,DB,2B,46,22,21,2B
Bytes for B-filter delay (18):       19,19,11,19
```

```
* TRAFO SLIC
* PARAMETER : M
*Z0R1=  700.0     *Z0C1=  .0000     *Z0R2=  .0000     *Z0C2= .1000E-06
*Z0RS=  .0000     *Z0CS=  .0000
*RCU1=  84.00     *RCU2=  105.0     *CW1 =  .1135E-09 *CW2 = .1354E-09
* L1 =  1.150     * L2 =  1.150     * M =   1.148
*CSP =  .1000E-05
* RF =  792.0     * LF =  2.230     * CF =  .2670E-08
*ZSLI = 0.500

Run #   1

Z-FILTER calculation results

  Reference impedance for optimization (ZI):
ERZI = 1  RSER =   220. CSER =  .000  RPAR =    820. CPAR =  .115E-0

  Calculated and quantized coefficients:

XZ  =    -.10895    .28881    .00646   -.30563    .19882
XZQ =    -.10889    .28906    .00635   -.30469    .19531
Bytes for Z-Filter (13):    20,BA,2A,7B,1B,32,B2,5B
```

RETURN LOSS

FREQ (Hz)	loss (dB)	FREQ (Hz)	loss (dB)
100.	11.948	1800.	32.679
200.	21.095	1900.	32.716
300.	28.062	2000.	32.727
400.	31.054	2100.	32.721
500.	31.555	2200.	32.712
600.	31.454	2300.	32.713
700.	31.340	2400.	32.738
800.	31.309	2500.	32.798
900.	31.359	2600.	32.901
1000.	31.471	2700.	33.051
1100.	31.626	2800.	33.244
1200.	31.807	2900.	33.459
1300.	31.999	3000.	33.660
1400.	32.186	3100.	33.776
1500.	32.357	3200.	33.714
1600.	32.499	3300.	33.375
1700.	32.608	3400.	32.702

```
Min. Z-loop reserve:      5.721 dB
       at frequency:     8500.0 Hz
Min. Z-loop mirror signal reserve:     10.365 dB
                     at frequency:     9000.0 Hz
Run #   1

X-FILTER calculation results
  Calculated and quantized coefficients:

XX  =    1.01799    .01508    .01135    .00340    .00974
XXQ =    1.01758    .01508    .01147    .00342    .00974
Bytes for X-Filter (23):    70,E2,97,73,C1,D6,03,36

X-filter attenuation function (in dB),(always absolute values)

  FREQ         loss       GD              FREQ         loss        GD
  (Hz)         (dB)     (msec)            (Hz)         (dB)      (msec)
   300.        -.432      .008            1900.        -.137       .002
   400.        -.395      .006            2000.        -.137       .002
   500.        -.351      .004            2100.        -.131       .002
   600.        -.305      .002            2200.        -.119       .001
   700.        -.257      .000            2300.        -.103       .001
   800.        -.213     -.002            2400.        -.082      -.000
   900.        -.173     -.003            2500.        -.060      -.002
  1000.        -.141     -.004            2600.        -.038      -.003
  1100.        -.118     -.005            2700.        -.019      -.004
  1200.        -.103     -.005            2800.        -.005      -.005
  1300.        -.097     -.004            2900.         .003      -.005
  1400.        -.098     -.004            3000.         .003      -.005
  1500.        -.105     -.002            3100.        -.004      -.005
  1600.        -.114     -.001            3200.        -.018      -.004
  1700.        -.124      .000            3300.        -.039      -.003
  1800.        -.133      .001            3400.        -.064      -.002
  1900.        -.137      .002            3500.         .008       .000
  2000.        -.137      .002            3600.         .006       .000

GX results:
All attenuation values (in dB) refer to FREF =    1014. Hz

    RLX    SLIC+Z    VREF/VSICOFI    XREF          GX
    .00 -   2.22  -       4.42    -   -.14    =     -6.50  ideal
   -.01 =   2.22  +       4.42    +   -.14    +     -6.52  quant

Second byte for Gain:      ,00,C3
Calculation of transmit transfer function (AD)
All attenuation values (in dB) refer to FREF =     1014.0 Hz

  Reference impedance for optimization (ZI):
ERZI = 1 RSER =    220. CSER =  .000     RPAR =    820. CPAR =  .115E-0
```

TGREF CA = .305 ms TGREF CB = .318 ms

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
100.	17.538	5.266	2000.	-.076	.012
200.	.700	2.515	2100.	-.079	.016
300.	.018	.901	2200.	-.077	.022
400.	-.056	.459	2300.	-.070	.028
500.	-.079	.271	2400.	-.059	.035
600.	-.078	.171	2500.	-.046	.043
700.	-.062	.112	2600.	-.031	.053
800.	-.040	.073	2700.	-.017	.065
900.	-.018	.047	2800.	-.004	.079
1000.	.001	.029	2900.	.008	.097
1100.	.014	.017	3000.	.021	.119
1200.	.020	.009	3100.	.037	.147
1300.	.018	.004	3200.	.062	.181
1400.	.010	.001	3300.	.107	.226
1500.	-.004	.000	3400.	.189	.285
1600.	-.020	.001	3500.	.339	.367
1700.	-.038	.002	3600.	.627	.488
1800.	-.054	.005	3700.	1.228	.685
1900.	-.067	.008	3800.	2.702	1.023

Run # 1

R-FILTER calculation results
Calculated and quantized coeffizients:

XR = .96755 -.04884 -.01447 -.00040 .00910
XRQ = .96777 -.04883 -.01453 -.00049 .00903
Bytes for R-Filter (2B): 70,23,8F,EC,3C,AC,0B,5D

R-filter attenuation function (in dB), (always absolute values)

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
300.	.797	-.007	1900.	.101	.008
400.	.798	-.008	2000.	.065	.009
500.	.796	-.009	2100.	.040	.009
600.	.788	-.010	2200.	.026	.008
700.	.773	-.010	2300.	.020	.007
800.	.749	-.010	2400.	.022	.006
900.	.714	-.010	2500.	.030	.005
1000.	.669	-.009	2600.	.039	.003
1100.	.614	-.007	2700.	.050	.002
1200.	.551	-.005	2800.	.057	.001
1300.	.482	-.003	2900.	.061	.000
1400.	.409	-.001	3000.	.060	-.000
1500.	.337	.001	3100.	.052	-.000
1600.	.267	.004	3200.	.039	.000
1700.	.203	.005	3300.	.020	.001
1800.	.147	.007	3400.	-.002	.002
1900.	.101	.008	3500.	-.007	.000
2000.	.065	.009	3600.	-.008	.000

GR results:
All attenuation values (in dB) refer to FREF= 1014. Hz

```
   -RLR    SLIC+Z    VSICOFI/VREF   RREF           GR
   7.00 -   5.32  -     -4.42    -   .66     =       5.44  ideal
   7.00 =   5.32  +     -4.42    +   .66     +       5.43  quant

First byte for Gain (30):      41,C3
Calculation of receive transfer function (DA)
All attenuation values (in dB) refer to FREF =      1014.0 Hz

  Reference impedance for optimization (ZI):
ERZI = 1 RSER =    220. CSER =  .000     RPAR =     820. CPAR = .115E-0
TGREF CA =    .262 ms      TGREF CB =    .244 ms
```

FREQ (Hz)	loss (dB)	GD (msec)	FREQ (Hz)	loss (dB)	GD (msec)
100.	3.702	2.741	2000.	-.105	.025
200.	.355	.717	2100.	-.105	.031
300.	.008	.300	2200.	-.099	.037
400.	-.086	.159	2300.	-.089	.043
500.	-.105	.093	2400.	-.075	.051
600.	-.094	.056	2500.	-.059	.059
700.	-.070	.034	2600.	-.043	.069
800.	-.044	.019	2700.	-.028	.082
900.	-.021	.010	2800.	-.014	.097
1000.	-.004	.004	2900.	-.003	.115
1100.	.004	.001	3000.	.008	.137
1200.	.004	.000	3100.	.021	.164
1300.	-.004	.000	3200.	.043	.199
1400.	-.017	.002	3300.	.083	.243
1500.	-.035	.005	3400.	.158	.302
1600.	-.054	.008	3500.	.300	.384
1700.	-.072	.012	3600.	.577	.506
1800.	-.088	.016	3700.	1.166	.703
1900.	-.099	.020	3800.	2.625	1.041

Run #   1

```
B-FILTER calculation results

  Reference impedance for optimization (ZL):
ERZL = 1 RSL  =    220. CSL  =  .000     RPL  =     820. CPL = .115E-0

Calculated and quantized coefficients:

XB  =     .20818    .34529    .25405   -.12179   -.09620
          .15308    .01798   -.18711    .18355   -.08915
XBQ =     .21094    .34375    .25415   -.12158   -.09570
          .15234    .01782   -.18799    .18359   -.08594
2nd part of bytes B-Filter (0B):    00,2C,31,C1,AA,6F,33,23
1st part of bytes B-Filter (03):    BB,CA,DB,2B,46,22,21,2B

TRANS HYBRID LOSS

  FREQ        loss                             FREQ        loss
  (Hz)        (dB)                              (Hz)        (dB)
   100.      22.979                            1800.      38.757
   200.      21.665                            1900.      36.141
   300.      26.651                            2000.      34.677
   400.      32.370                            2100.      34.020
   500.      42.075                            2200.      34.049
   600.      47.207                            2300.      34.748
   700.      37.954                            2400.      36.166
   800.      34.818                            2500.      38.311
   900.      33.479                            2600.      40.525
  1000.      33.128                            2700.      40.406
  1100.      33.521                            2800.      37.955
  1200.      34.636                            2900.      35.622
  1300.      36.631                            3000.      34.139
  1400.      40.013                            3100.      33.619
  1500.      46.646                            3200.      34.277
  1600.      57.076                            3300.      36.848
  1700.      43.595                            3400.      44.261

Additonal B-filter delay (in seconds):   .625E-04
Bytes for B-filter delay (18):  19,19,11,19
```

Appendix A4

Listing of FORTRAN SLIC Program

```
C################################################################C
C###                                                         ###C
   PROGRAM TRAFOT
C###                                                         ###C
C### Version  V3.1  Mr. Glasser  Jan 1989                    ###C
C### Revision V3.2  Mr. Kliese   Feb 1989                    ###C
C### Revision V3.3  Subroutine IMPED6                        ###C
C###                   Mr. Kliese     Aug 1989               ###C
C###                                                         ###C
C### Copyright 1989 Siemens AG Munich, West Germany          ###C
C### Mr Kliese tel (089) 4144-3662                           ###C
C###                                                         ###C
C################################################################C
C###                                                         ###C
C### The following program calculates the M- or K-           ###C
C### parameters of a transformer slic.                       ###C
C### It uses complex calculations and A-parameters matrixes.###C
C### The data to be hold during the execution are stored     ###C
C### in 'COMMON fields', which names begin by 'Q'.           ###C
C### The transformer is calculated in the subroutine         ###C
C### TRSLIC and its feeding in the subroutine ZFEED.         ###C
C### Complex matrix multiplication is made by the            ###C
C### subroutine CMATMUL.                                     ###C
C###
C### Note: FORTRAN requires at least 7 spaces at the         ###C
C### beginning of a line ; a sign (e.g.'&')in the 6th        ###C
C### place means that the line continues underneath.         ###C
C### '*'or 'c' are comments.                                 ###C
C###                                                         ###C
C################################################################C
*
****************************************************************
*        Declaration of Variables                              *
****************************************************************
* implicit variables beginning with A,B,...K and
* M...Z are declared as logical; variables beginning
* with L are declared as character : if a variable
* has not been declared the compiler will give a warning.
*
  IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
*
  INTEGER IN,OUT,I,ERZ0
*
  CHARACTER*1  PARA
  CHARACTER*12 FILEOUT,INFILE,B1,B2,B3,B4
*
  REAL CSP,CW1,M,L1,L2,RCU1,RCU2,RF,LF,CF,CW2
  REAL PI2,R5,R6,R7,C5,R4,R3,C3,ZSLI,FREQ
```

```
  REAL Z0R1,Z0R2,Z0C1,Z0C2,Z0RS,Z0CS
  REAL ZgR1,ZgR2,ZgC1,ZgC2,ZgRS,ZgCS
  COMPLEX Z0,A,B,A11,A12,A21,A22,ADET,AR,AX,ZIN,Zg,DEN
  COMPLEX M11TAB(399),M12TAB(399),M21TAB(399),M22TAB(399)
  COMPLEX M11,M12,21,M22
  COMPLEX K11TAB(399),K12TAB(399),K21TAB(399),K22TAB(399)
  COMPLEX K11,K12,K21,K22
  LOGICAL  LINFIL
* data storage for 2*Pi
  COMMON /QPI2/ PI2
* data storage for PARAmeter
  COMMON /QPARA/ PARA
* data storage for matching impedance Z0
  COMMON /QZ0/ Z0R1,Z0R2,Z0C1,Z0C2,Z0RS,Z0CS
* data storage for line/source impedance Zg
  COMMON /QZg/ ZgR1,ZgR2,ZgC1,ZgC2,ZgRS,ZgCS
* data storage for transformer
  COMMON /QTR/ RCU1,RCU2,CW1,L1,CW2,RF,LF,CF,CSP,L2,M
* data storage for M-parameters tables (containing 399 values each)
  COMMON /QM/ M11TAB,M12TAB,M21TAB,M22TAB
*
*****************************************************************
*       Program Begins:                                         *
*****************************************************************

* screen
    OUT = 6
* keyboard
    IN = 5
* 2*pi calculation
    PI2 = 4.* ASIN(1.)
* reading file names
    FILEOUT = ''
    INFILE = ''
     WRITE(OUT,'(A)')  'TRAFOT SLIC Program Version V3.3
Siemens AG Munich, Aug. 1989'
     WRITE(OUT,'(A\)')
  &' Enter input file name(xxxxxxxx.INP):'
10     READ (IN,'(A)') INFILE
      INQUIRE (FILE = INFILE,EXIST = LINFIL)
       IF (INDEX(INFILE,'').EQ.1.OR.(.NOT.LINFIL)
  &     .OR.(INDEX(INFILE,'.INP').EQ.0
  &     .AND.INDEX(INFILE,'.inp').EQ.0))THEN
       WRITE (OUT,'(A\)')'Enter correct input file name:'
       INFILE=''
       GOTO 10
      ENDIF
* Reading input file
* note: every second line is read
   OPEN (10, FILE=INFILE, ERR=1100, STATUS= 'OLD')
C   WRITE(6,*) 'Reading input file'
   READ(10,'(A)')
```

```
   READ(10,'(A)')PARA
   READ(10,'(A)')
   READ(10,*) RCU1,RCU2
   READ(10,'(A)')
   READ(10,*) CW1,CW2
   READ(10,'(A)')
   READ(10,*) L1,L2,M
   READ(10,'(A)')
   READ(10,*) CSP
   READ(10,'(A)')
   READ(10,*) RF,LF,CF
   READ(10,'(A)')
   READ(10,*) ZSLI
   READ(10,'(A)')
   READ(10,'(A)')
   READ(10,*) Z0R1,Z0C1,Z0C2,Z0R2,Z0RS,Z0CS
   READ(10,'(A)')
   READ(10,'(A)')
   READ(10,*) ZgR1,ZgC1,ZgC2,ZgR2,ZgRS,ZgCS
   READ(10,'(A)')
   CLOSE (10)
*
C**************************************************************
C     Screen picture of TRAFOT SLIC
C     using ANSI.SYS driver
C**************************************************************

   WRITE (OUT,'(A)')'       ---------
  &        |    +---------+'
   WRITE (OUT,'(A)')        | Trans- |     transmit->
  &      +---------|Vin   ¦'
   WRITE (OUT,'(A)')'       | verse  |
  &      ¦ |    ¦       ¦'
   WRITE (OUT,'(A)')'    __ | feeding |    __ __
  &__  __  ¦ |__ ¦       ¦'
   WRITE (OUT,'(A)') +-¦__+---o----¦+----o---¦__+---¦__+---o---¦
  &__+---¦__+---o---¦__+--¦Vout   ¦'
   WRITE (OUT,'(A)')¦Zg/2|¦ CSP=| ¦ RCU1= L1-M ¦ L
  &2-M RCU2= ¦ |Z0 ¦     ¦'
   WRITE (OUT,20) CSP, RCU1 RCU2
20  FORMAT        (' O  |¦',G10.4,'¦ ', G10.4,'¦
  & ',G10.4,'¦ |  ¦ S¦')
   WRITE (OUT,21) M
21  FORMAT        (' ¦   |+-+  | ---          +-+ M=
  &' ,G10.4,'---|  ¦ | ¦')
   WRITE (OUT,'(A)')' ¦   |+-+ZSP | --- CW1=        +-+
  &  CW2= --- |   ¦  C    ¦'
   WRITE (OUT,22) CW1, CW2
22  FORMAT        (' O  |¦     |¦',G10.4,'  ¦
  & ',G10.4,'¦ |  ¦ O¦')
   WRITE (OUT,'(A)')' ¦__ |¦    |¦        ¦
```

```
  &       ¦ |  ¦ F ¦'
   WRITE (OUT,'(A)')' +-¦__+---o----------o----------------o----
  &-------------o |  ¦ | ¦'
   WRITE (OUT,'(A)')' Zg/2 |    |
  &        |   ¦    ¦'
   WRITE (OUT,'(A)')'   |_________|    <-receive
  &        |   +---------+'
   WRITE (OUT,42) ZSLI
42  FORMAT('SLIC Loop Attenuation ZSLI=', G10.4)
   WRITE (OUT,43) RF, LF, CF
43  FORMAT('Feeding ZSP:     RF=',G10.4,'  LF=',G10.4,
  &'  CF=',G10.4)
   WRITE (OUT,44) L1, L2
44  FORMAT('Leaking inductance: L1=',G10.4,' L2=',G10.4)
   WRITE(OUT,45)
45  FORMAT('Matching impedance: Z0R1  Z0C1  Z0C2  Z0R2
  &  Z0RS  Z0C')
   WRITE(OUT,46) Z0R1, Z0C1, Z0C2, Z0R2, Z0RS, Z0CS
46  FORMAT('            ',G10.4, G10.4, G10.4,
C46  FORMAT('            ',G10.4,'', G10.4,'', G10.4,
C  &'', G10.4,'', G10.4,'',G10.4)
  & G10.4, G10.4, G10.4)
   WRITE(OUT,47)
47  FORMAT('Source/line impedance: ZgR1  ZgC1  ZgC2  ZGR2
  &  ZgRS  ZGCS')
   WRITE(OUT,48) ZgR1, ZgC1, ZgC2, ZgR2, ZGRS, ZgCS
48  FORMAT('            ', G10.4, G10.4, G10.4,
C 48  FORMAT('            ', G10.4,'', G10.4,'', G10.4,'',
C  & G10.4,'', G10.4,'',G10.4)
  & G10.4, G10.4, G10.4)
C**********************************************************
   WRITE(OUT,'(A\)')' Enter output file name (xxxxxxxx.SLI):'
50  READ (IN,'(A)') FILEOUT
   IF (INDEX(FILEOUT,'').EQ.1
  &   .OR.(INDEX(FILEOUT,'.SLI').EQ.0
  &     .AND.INDEX(FILEOUT,'.sli').EQ.0)) THEN
     WRITE (OUT,'(A\)')
  & 'Enter correct output file name (with extention .SLI):'
    FILEOUT=''
    GOTO 50
  ENDIF
```

```
*************************************************************
*         Documentaion Part                                 *
*************************************************************
* Opening and writing output file              *
*                                      *
* Each variable (e.g.ZgR1) is put in a buffer (e.g.B1)      *
* and this buffer is concatenate with the string containing  *
* the variable name (e.g.'*ZgR1').
*                                      *
* Note: The "*" at the beginning is necessary for the SICOFI *
*     program to consider these lines as comments.       *
*************************************************************
*
   OPEN (30, FILE=FILEOUT, ERR=1000, STATUS='UNKNOWN')
*
   WRITE (30,'(A)')'* TRAFO SLIC'
   WRITE (30,'(A)')'* PARAMETER:'//PARA
   IF (PARA.NE.'M') THEN
    WRITE (B1,'(G11.4)') ZgR1
    WRITE (B2,'(G11.4)') ZgC1
    WRITE (B3,'(G11.4)') ZgR2
    WRITE (B4,'(G11.4)') ZgC2
    WRITE (30,'(A)')'*ZgR1='//B1//'*ZgC1='//B2//
  &        '*ZgR2='//B3//'*ZgC2='//B4
    WRITE (B2,'(G11.4)') ZgRS
    WRITE (B3,'(G11.4)') ZgCS
    WRITE (30,'(A)')'*ZgRS='//B2//'*ZgCS='//B3
   ENDIF
   WRITE (B1,'(G11.4)') Z0R1
   WRITE (B2,'(G11.4)') Z0C1
   WRITE (B3,'(G11.4)') Z0R2
   WRITE (B4,'(G11.4)') Z0C2
   WRITE (30,'(A)')'* Z0R1='//B1//'*Z0C1='//B2//
  &        '*Z0R2='//B3//'*Z0C2='//B4
   WRITE (B2,'(G11.4)') Z0RS
   WRITE (B3,'(G11.4)') Z0CS
   WRITE (30,'(A)')'*Z0RS='//B2//'*Z0CS='//B3
   WRITE (B1,'(G11.4)') RCU1
   WRITE (B2,'(G11.4)') RCU2
   WRITE (B3,'(G11.4)') CW1
   WRITE (B4,'(G11.4)') CW2
   WRITE (30,'(A)')'*RCU1='//B1//'*RCU2='//B2//
  &        '*CW1='//B3//'*CW2='//B4
   WRITE (B1,'(G11.4)') L1
   WRITE (B2,'(G11.4)') L2
   WRITE (B3,'(G11.4)') M
   WRITE (30,'(A)')'* L1='//B1//'*L2='//B2//'* M ='//B3
   WRITE (B2,'(G11.4)') CSP
   WRITE (30,'(A)')'* CSP ='//B2
   WRITE (B1,'(G11.4)') RF
   WRITE (B2,'(G11.4)') LF
   WRITE (B3,'(G11.4)') CF
   WRITE (30,'(A)')'* RF ='//B1//'*LF ='//B2//'* CF ='//B3
* ZSLI: worst case half loop
```

```
   WRITE (B2,'(G11.4)') ZSLI
   WRITE (30,'(A)')'*ZSLI='//B2
   WRITE (30,'(A)')'ZSLI'
   WRITE (30,'(G11.4)') ZSLI
*
**************************************************************
*          Calculation Part                                  *
**************************************************************
*
   WRITE (OUT,*)'Running preliminary calculations...'
   DO 177 I=1,399
    FREQ = REAL(I*10)
* calculates for M parameters
    IF (PARA.EQ.'M') THEN
* M11
     CALL Z0W(FREQ,Z0)
     CALL TRSLIC(FREQ,A11,A12,A21,A22,ADET)
     DEN = A11*Z0 + A12
     M11 =(A21*Z0+A22)/DEN
C       (A11*Z0+A12)
* M12
     M12 =  -ADET/DEN
C        (A12+A11*Z0)
* M21
     M21 =  Z0/DEN
C        (A12+Z0*A11)
* M22
     M22 =  A12/DEN
C       (A12+Z0*A11)
* put the calculated values in the corresponding tables
     M11TAB(i)=M11
     M12TAB(i)=M12
     M21TAB(i)=M21
     M22TAB(i)=M22
    ELSE
* calculates for K parameters
* K11
     CALL Z0W(FREQ,Z0)
     CALL ZgW(FREQ,Zg)
     CALL TRSLIC(FREQ,A11,A12,A21,A22,ADET)
     ZIN = (A11*Z0+A12)/(A21*Z0+A22)
     K11 = (Zin-Zg)/(Zin+Zg)
* K12
     K12 =       2.*ADET*Zg/
   &     (Zg*(A22+A21*Z0) + (A12+A11*Z0))
* K21
     K21 =    Z0/
   &     (Z0*(A11+A21*Zg) + (A12+A22*Zg))
* K22
     K22 =    (A22*Zg+A12)/
   &     (Z0*(A11+A21*Zg) + (A12+A22*Zg))
C put the calculated values in the corresponding tables
     K11TAB(i)=K11
     K12TAB(i)=K12
     K21TAB(i)=K21
     K22TAB(i)=K22
```

```
    ENDIF
177  CONTINUE
*
   IF (PARA.EQ.'M') THEN

* Writing the Mij values in the output file
     write (30,'(A)')'M11-TABLE'
     WRITE (OUT,'(A)')'+Running M11 calculation...
     DO 100 I=1,399
      FREQ = REAL(I*10)
      WRITE (30,*) FREQ,REAL(M11TAB(i)),AIMAG(M11TAB(i))
100   CONTINUE
     WRITE (30,'(A)')'M12-TABLE'
     WRITE (OUT,'(A)')'+Running M11, M12 calculation...'
     DO 110 I=1,399
      FREQ = REAL(I*10)
      WRITE (30,*) FREQ,REAL(M12TAB(i)),AIMAG(M12TAB(i))
110   CONTINUE
     WRITE (30,'(A)')'M21-TABLE'
     WRITE (OUT,'(A)')'+Running M11, M12, M21 calculation...'
     DO 120 I=1,399
      FREQ = REAL(I*10)
      WRITE (30,*) FREQ,REAL(M21TAB(i)),AIMAG(M21TAB(i))
120   CONTINUE
     WRITE (30,'(A)')'M22-TABLE'
     WRITE (OUT,'(A)')'+Running M11, M12, M21, M22 calculation...'
     DO 130 I=1,399
      FREQ = REAL(I*10)
      WRITE (30,*) FREQ,REAL(M22TAB(i)),AIMAG(M22TAB(i))
130   CONTINUE

   ELSE

* Writing the Kij value in the output file
     write (30,'(A)')'K11-TABLE'
     WRITE (OUT,'(A)')'+Running K11 calculation...
     DO 200 I=1,399
      FREQ = REAL(I*10)
      WRITE (30,*) FREQ,REAL(K11TAB(i)),AIMAG(K11TAB(i))
200   CONTINUE
     WRITE (30,'(A)')'K12-TABLE'
     WRITE (OUT,'(A)')'+Running K12 calculation...'
     DO 210 I=1,399
      FREQ = REAL(I*10)
      WRITE (30,*) FREQ,REAL(K12TAB(i)),AIMAG(K12TAB(i))
210   CONTINUE
     WRITE (30,'(A)')'K21-TABLE'
     WRITE (OUT,'(A)')'+Running K21 calculation...'
     DO 220 I=1,399
      FREQ = REAL(I*10)
      WRITE (30,*) FREQ,REAL(K21TAB(i)),AIMAG(K21TAB(i))
220   CONTINUE
     WRITE (30,'(A)')'K22-TABLE'
     WRITE (OUT,'(A)')'+Running K22 calculation...'
     DO 230 I=1,399
      FREQ = REAL(I*10)
```

```
      WRITE (30,*) FREQ,REAL(K22TAB(i)),AIMAG(K22TAB(i))
200   CONTINUE
    ENDIF
    WRITE(30,'(A1)')';'
    CLOSE (30)
    WRITE(OUT,'(A)')'+Data written in file:   '//FILEOUT
    STOP
* error melding
1000 WRITE(OUT,'(A)')'OPEN ERROR AT OUTPUT-FILE:'//FILEOUT
    STOP 1
1100 WRITE(OUT,'(A)')'OPEN ERROR AT INPUT-FILE:'//INFILE
    STOP 2
    END
* end of main program
*
* auxiliary subroutines:
C
C################################################################C
C
   SUBROUTINE ZFEED(FREQ,Y5)
C
C################################################################C
C
C  Input parameters: FREQ
C
C  Output parameters: Y5 [COMPLEX]
C             (admittance of transverse feeding)
C
C  Common blocks:     QTR,QPI2
C
C  Task of this routine: Calculates the equivalent admittance
c                 of the transverse feeding:
C                 Y5 = (RF + LF) // CF
c
C  Routine called in the following subroutines or functions:
C                 TRSLIC
C################################################################C
C
  IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
  REAL FREQ,PI2,OMEGA,RF,LF,CF,QU
  REAL RCU1,RCU2,CW1,L1,CW2,CSP,L2,M
  COMPLEX Y5
*
  COMMON/QTR/RCU1,RCU2,CW1,L1,CW2,RF,LF,CF,CSP,L2,M
  COMMON/QPI2,PI2
C
  OMEGA = PI2*FREQ
  Y5 = ( 1./CMPLX(RF,OMEGA*LF)) + CMPLX(0,OMEGA*CF)
  RETURN
  END
C
```

```
C#####################################################################
C
   SUBROUTINE TRSLIC(FREQ,A11,A12,A21,A22,ADET)
C
C#####################################################################
C
C  Input parameters:  FREQ  [REAL]
C
C  Output parameters:  A11, A12, A21, A22, ADET
C                     [COMPLEX]
C
C  Common blocks:     QTR,QSLIC,QPI2
C
C  Task of this routine: Calculates the A-parameters describing
c                  the transformer.
c
C  Required subroutines: ZFEED,CMATMUL
C
C  Note: AA(1,i,j): REAL part of AA(i,j)
C      AA(2,i,j):IMAGinary part of AA(i,j)
C
C#####################################################################
C
  IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
  REAL R(6,3),Y(2,2,2),OMCSP
  REAL X(4,2),OMEGA,PI2
  REAL CSP,CW2,FREQ,CW1,L1,L2,RCU1,RCU2,RF,LF,CF,M
  REAL AA(2,2,2),BB(2,2,2),YINV(2,2,2)
  REAL A1(2,2,2),A2(2,2,2),A3(2,2,2),A4(2,2,2)
  REAL A5(2,2,2),A6(2,2,2),A7(2,2,2)
  COMPLEX Y1,Y2,Y3,Y4.Y5,C,D,E,F,XD,U,V,A11,A12
  COMPLEX A21,A22,ADET,Y6,Y7
*
  COMMON/QTR/RCU1,RCU2,CW1,L1,CW2,RF,LF,CF,CSP,L2,M
  COMMON/QPI2/PI2
C
  OMEGA = PI2*FREQ
  OMCSP = OMEGA*CSP
* blocking capacitor
     Y7 = CMPLX(0.,OMCSP)
* parallel feeding
     CALL ZFEED(FREQ,Y5)
* admitances in the equivalent circuit
* Y1
    Y1 = 1./CMPLX(RCU1,(OMEGA*(L1-M)))
*Y2
   Y2 = CMPLX(0.,(OMEGA*CW1))
*Y3
   Y3 = 1./CMPLX(RCU2,(OMEGA*(L2-M)))
*Y4
   Y4=CMPLX(0.,OMEGA*CW2))
*Y6
```

```
   Y6=CMPLX(0.,(-1./(omega*M)))
* corresponding matrixe
    CALL PARA(Y6,A6)
    CALL SERA(Y1,A1)
    CALL SERA(Y3,A3)
    CALL PARA(Y2,A2)
    CALL PARA(Y4,A4)
    CALL PARA(Y5,A5)
    CALL SERA(Y7,A7)
* matrix multiplications
    CALL CMATMUL(A5,A7,BB,2,2,2)
    CALL CMATMUL(BB,A2,AA,2,2,2)
    CALL CMATMUL(AA,A1,BB,2,2,2)
    CALL CMATMUL(BB,A6,AA,2,2,2)
    CALL CMATMUL(AA,A3,BB,2,2,2)
    CALL CMATMUL(BB,A4,AA,2,2,2)
C making complex out of two REAL
    A11 = CMPLX(AA(1,1,1),AA(2,1,1))
    A12 = CMPLX(AA(1,1,2),AA(2,1,2))
    A21 = CMPLX(AA(1,2,1),AA(2,2,1))
    A22 = CMPLX(AA(1,2,2),AA(2,2,2))
C adet=(a11*a22)-(a12*a21) is the determinant of the a-matrix
    ADET = (11*A22)-(A12*A21)
    RETURN
    END
```

```
C
C#####################################################################
C
   SUBROUTINE SERA(Y,A)
C
C#####################################################################
C
C  Input parameters: Y  [COMPLEX]
C
C  Output parameters: A(2,2,2) [ARRAY OF REAL]
C
C  Common blocks: /
C
C  Task of this routine: A matrix for serial admittance
C
C  Routine called in the following subroutines or functions:
C   TRSLIC
C#####################################################################
C
  IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
  REAL A(2,2,2)
  COMPLEX Y,Z
*
  Z = 1./Y
  A(1,1,1)= 1.
  A(2,1,1)= 0.
  A(1,1,2)= REAL(Z)
  A(2,1,2)= AIMAG(Z)
  A(1,2,1)= 0.
  A(2,2,1)= 0.
  A(1,2,2)= 1.
  A(2,2,2)= 0.
  RETURN
  END
C
C#####################################################################
C
   SUBROUTINE PARA(Y,A)
C
C#####################################################################
C
C  Input parameters: Y  [COMPLEX]
C
C  Output parameters: A(2,2,2) [array of REAL]
C
C  Common blocks:/
C
C  Task of this routine: A matrix for serial admittance
C
C  Routine called in the following subroutines or functions:
C   TRSLIC
C#####################################################################
C
  IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
  REAL A(2,2,2)
  COMPLEX Y
```

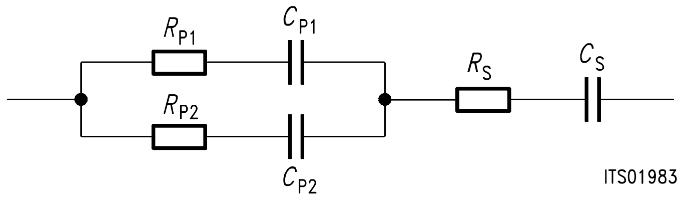
```
* A(1,1)
   A(1,1,1)= 1.
   A(2,1,1)= 0.
* A(1,2)

   A(1,1,2)= 0.
   A(2,1,2)= 0.
* A(2,1)
   A(1,2,1)= REAL(Y)
   A(2,2,1)= AIMAG(Y)
* A(2,2)
   A(1,2,2)= 1.
   A(2,2,2)= 0.
   RETURN
   END
C
C##################################################################C
C
   SUBROUTINE Z0W(FREQ,Z0)
C
C##################################################################C
   IMPLICIT LOGICAL (A-K,M-Z),CHARACTER(L)
   COMPLEX Z0
   REAL Z0R1,FREQ,Z0R2,Z0C1,Z0C2,Z0RS,Z0CS
   COMMON/QZ0/Z0R1,Z0R2,Z0C1,Z0C2,Z0RS,Z0CS
*
   CALL IMPED6(Z0R1,Z0R2,Z0C1,Z0C2,Z0RS,Z0CS,FREQ,Z0)
   RETURN
   END

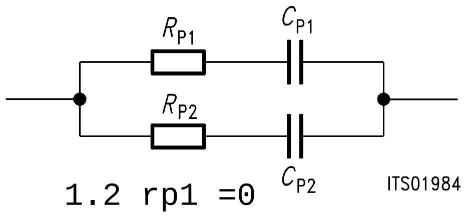
C##################################################################C
C
   SUBROUTINE ZgW(FREQ,Zg)
C
C##################################################################C
   IMPLICIT LOGICAL (A-K,M-Z),CHARACTER(L)
   COMPLEX Zg
   REAL ZgR1,FREQ,ZgR2,ZgC1,ZgC2,ZgRS,ZgCS
   COMMON/QZg/ZgR1,ZgR2,ZgC1,ZgC2,ZgRS,ZgCS
*
   call imped6(ZgR1,ZgR2,ZgC1,ZgC2,ZgRS,ZgCS,FREQ,Zg)
   RETURN
   END
```

```
C###################################################################C
C###                                                             ###C
   SUBROUTINE IMPED6(RP1,RP2,CP1,CP2,RS,CS,FREQ,Zeq)
C###                                                             ###C
C### Note: when a parameter is set to 0 then the                 ###C
C### corresponding resistor or capacitance does not exist        ###C
C###                                                             ###C
C### Formal parameter list:RP1,RP2,CP1,CP2,RS,CS,FREQ,Zeq        ###C
C###                                                             ###C
C### Input parameters:                                           ###C
C###   RS   [REAL] ; series resistance                           ###C
C###   CS   [REAL] ; series capacitance                          ###C
C###   RP1  [REAL] ; parallel resistance                         ###C
C###   RP2  [REAL] ; parallel resistance                         ###C
C###   CP1  [REAL] ; parallel capacitance                        ###C
C###   CP2  [REAL] ; parallel capacitance                        ###C
C###   FREQ [REAL] ; frequency                                   ###C
C###                                                         ###C
C### Output parameters:                                      ###C
C###   Zeq  [COMPLEX]                                        ###C
C###                                                         ###C
C### Common blocks: QPI2                                     ###C
C###                                                         ###C
```

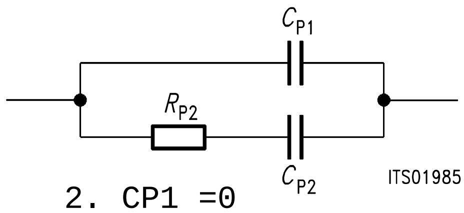
```
C### Task of this routine: Equivalent impedance of:              ###C
C###                                                              ###C
C###                                                             ###C
C###                                                             ###C
C###                                                             ###C
C###                                                             ###C
C###                                                             ###C
C###                                                             ###C
```



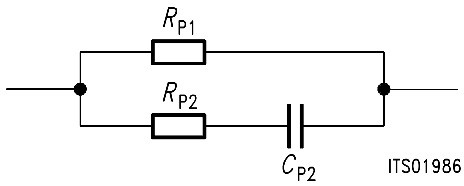

```
C### SPECIAL CASES:                                              ###C
C###      A. SYSTEM Parallel                                     ###C
C###        1. CP1 not 0                                         ###C
C###          1.1 rp1 not 0                                      ###C
C###                                                             ###C
C###                                                             ###C
C###                                                             ###C
C###                                                             ###C
C###                                                             ###C
C###                                                              ###C
```



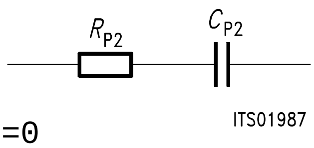

```
C###            1.2 rp1 =0                                       ###C
C###                                                             ###C
C###                                                             ###C
C###                                                             ###C
C###                                                              ###C
C###                                                             ###C
C###                                                             ###C
C###                                                              ###C
```



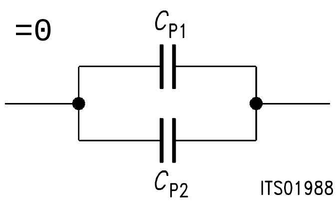

```
C###            2. CP1 =0                                        ###C
C###                                                             ###C
C###            2.1 rp1 not 0                                    ###C
C###                                                             ###C
C###                                                             ###C
C###                                                             ###C
C###                                                             ###C
C###                                                             ###C
C###                                                             ###C
C###                                                              ###C
```



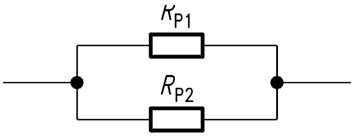

```
C###            2.2 rp1 =0                                       ###C
C###                                                             ###C
C###                                                             ###C
C###                                                             ###C
```




```
C###            3. idem if CP2 =0                                ###C
C###                                                              ###C
C###            4. RP2=0 and rp1 =0                              ###C
C###                                                             ###C
C###                                                             ###C
C###                                                             ###C
C###                                                              ###C
C###                                                             ###C
```

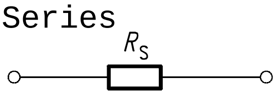


```
C###            5.CP2 =0 and CP1 =0                                    ###C
```



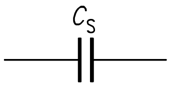
ITS01989

```
C###                                                                   ###C
C###           B. SYSTEM Series                                        ###C
C###            1. CS = 0                                              ###C
```



ITS01990

```
C###            1. RS = 0                                              ###C
C###                                                                   ###C
C###            idem system A                                          ###C
```



ITS01991

```
C###                                                                   ###C
C###           C. Conclusion: Zeq = sum of the two                     ###C
C###                 systems in any case                               ###C
C###                                                                   ###C
C#################################################################C
C                                                                     ###C
   IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
   REAL CP1,CP2,RP1,RP2
   REAL CS,RS,N,UL
   REAL FREQ,PI2,OMEGA
   COMPLEX D,C,Zeq,ZA,ZB
*
   COMMON/QPI2/PI2
*
   OMEGA = PI2*FREQ
   IF (CP1.EQ.0) THEN
     C=CMPLX(RP1,0.)
   ELSE
     C = RP1 + (1./CMPLX(0.,OMEGA*CP1))
   ENDIF
   IF (CP2.EQ.0) THEN
     D=CMPLX(RP2,0.)
   ELSE
     D = RP2 + (1./CMPLX(0.,OMEGA*CP2))
   ENDIF
   N  = CABS(C)
   UL = CABS(D)
* if one of them is 0 then no parallel calculation
   IF ((N.EQ.0.).OR.(UL.EQ.0.)) then
       ZA=C+D
   ELSE
* ZA = C & D in parallel
       ZA=C*D/(C+D)
   ENDIF
C System series
   IF (CS.EQ.0) THEN
     ZB=CMPLX(RS,0.)
   ELSE
     ZB = RS +(1./CMPLX(0.,OMEGA*CS))
   ENDIF
```

```
c both
   Zeq=ZA+ZB
   RETURN
   END
C
C###################################################################
C
   SUBROUTINE CMATMUL(A,B,C,L,MM,N)
C
C###################################################################
C
C  Input parameters:
C    A  [REAL] ARRAY [2,L,MM]
C    B  [REAL] ARRAY [2,MM,N]
C    L  (INTEGER)
C    MM   (INTEGER)
C    N  (INTEGER)
C
C  Example: A(i,j) = A(1,i,j) + j*A(2,i,j)

C  Output parameters:
C    C = [REAL] ARRAY [2,L,N]
C
C  Task of this routine: C = A*B
c    SUBROUTINE FOR THE COMPLEX MATRIX MULTIPLICATION
c
C  Routine called in the following subroutines or functions:
C    TRSLIC
C  Important notice: It is not possible to do A*A=A
C###################################################################
C
   IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
   INTEGER I,J,K,L,MM,N
   REAL A(2,L,MM),B(2,MM,N)
   REAL C(2,L,N)
*
   DO 10 I=1,L
   DO 10 J=1,N
    C(1,I,J)=0.0
    C(2,I,J)=0.0
C  COMPLEX multiplication: a(2,i,k) * b(2,k,j) = d(2,i,j)
    DO 20 K=1,MM
     C(1,I,J)=C(1,I,J)+A(1,I,K)*B(1,K,J)-A(2,I,K)*B(2,K,J)
     C(2,I,J)=C(2,I,J)+A(2,I,K)*B(1,K,J)+A(1,I,K)*B(2,K,J)
20  CONTINUE
10 CONTINUE
  RETURN
  END
```

Appendix A5

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SICOFI® Application Together with Transformer SLIC for USA Specification

Contents **Page**

1 Introduction

The requirements for an analog line card on the USA market are oriented on the AT&T specification for the public network.

The return loss has to be very high (> 32 dB) and it is a 3 dB gain in transmit direction and a 3 dB loss in receive direction needed. If a transformer SLIC with series line feeding will be used, a great transformer (for DC-current) has to be taken.

In this note a SLIC circuit for the USA-specification with series feeding, a high return loss and a good echo return loss is presented.

2 Circuit Description

This SLIC needs some external components, which support the 3 dB gain in transmit direction and a loss of 3 dB in receive direction. This hardware supports the B-filter of the SICOFI, too. In the following **refer to figure 1** on the next page.

The resistor R_8 is used for serial feeding. The feeding has to be symmetrically to ground and therefore it is possible to place the battery between the half of R_8 of both lines. This resistor and the impedance Z_0 put in the return loss. The Z_0 is transformed with the winding ratio of the transformer. By the resistor R_8 and by the ratio of the transformer (here: ü = 1) the OP1 has to amplify the signal. The OP1 amplifies the received signal and the transmit direction must have a gain of 3 dB, therefore the B-filter of the SICOFI can not set the echo return loss. The OP2 is used as a subtraction amplifier. OP2 amplifies the transmit signal and subtracts the receive signal. In this case a good echo return loss can be achieved.

R_5 and R_6 set the gain of the transmit signal. C_3, R_3 and R_4 set the subtracting factor. The capacitances C_1 and C_3 are decoupling the DC of the OP's. Because the input impedance of the SICOFI is very high (MΩ – GΩ). R_7 forms together with C_2 a defined time constant.

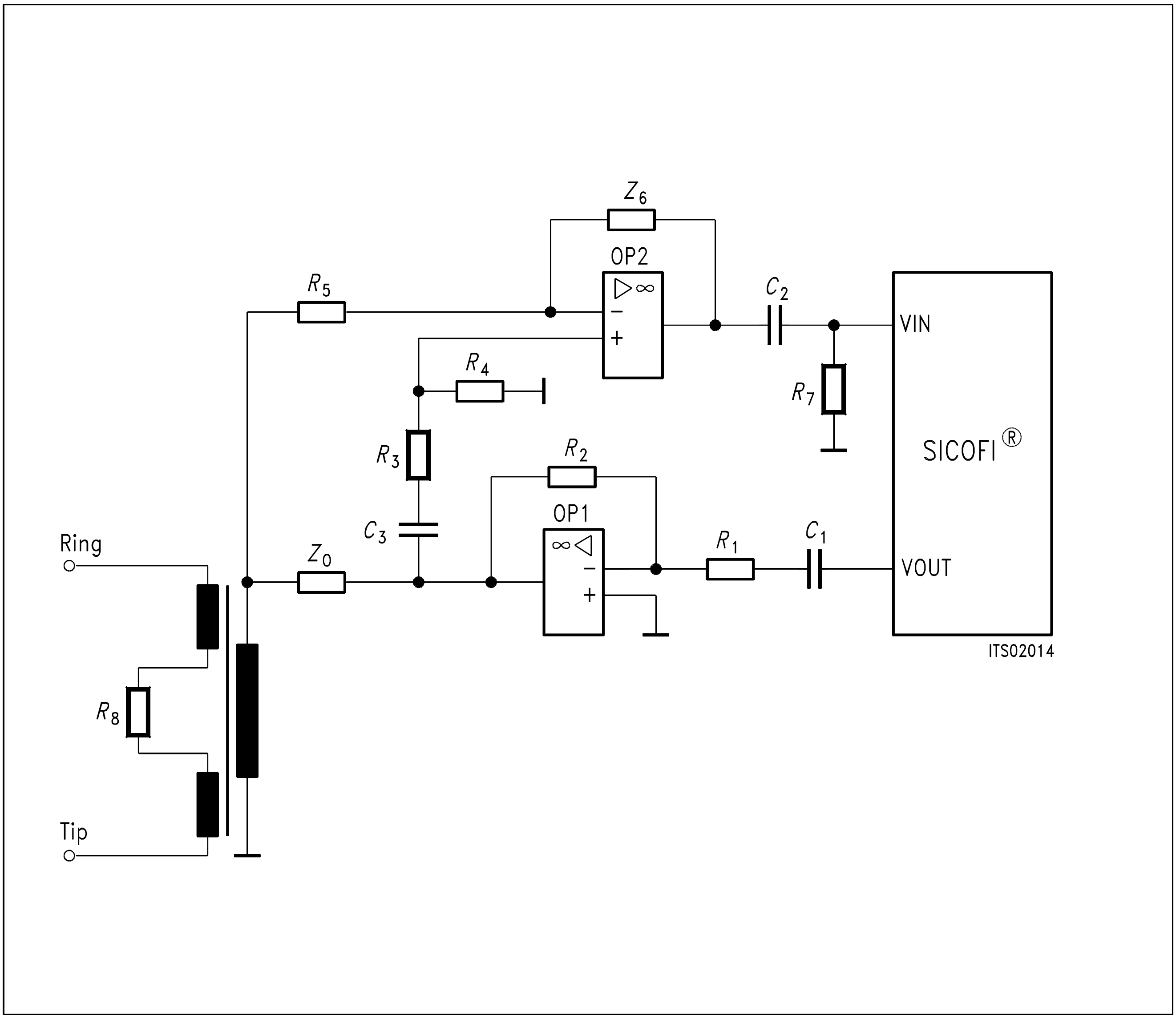


Figure 1

Transformer SLIC with Series Feeding

3 Calculation

The SICOFI coefficient program calculates the coefficients for this transformer SLIC application. The result file is shown now:

Result file:

```
  Input_file_name:                         Date: 19. April 1989
  SPEC = USA.SPE                               SLIC = TEST1.MES
  BYTE = COM.BYT      CHNR = 0,A
  PLQ = N

  ON = ALL                     REL   = Y                    SHORT = N
  OPT =    Z+X+R+B             ZXRB =  OOON
     FZ =  300.00       3400.0       ZLIM =  2.00
  ZREP  =N                          ZSIGN =  1
    FR =   200.00       3400.0
  RFIL =  Y             RREFQ = N       RREF = 0.13303
    FX =   300.00       3300.0
  XFIL =  Y             XREFQ = N       XREF =-0.20747
    FB =   300.00       3400.0       BLIM =  2.00 TBM =  1
  BREP = Y                          BSIGN =  1
  APOF =  0.00E+00 DPOF =  0.00E+00 APRE =  0.00E+00 DPRE =  0.00E+00
  XZQ =   0.42968750000000000E-01  -0.97656250000000000E-03
         -0.21484375000000000E-01  -0.11962890625000000E-01
          0.23681640625000000E-01
  XRQ =  0.9921875000 -0.0019531250  0.0087890625  0.0000000000
0.0058590000

  XXQ =  1.0234375000  0.0175781250 -0.0058593750  0.0175781250 -
0.000976000

  XBQ =   0.12451171875000000E+00  -0.20312500000000000E+00
          0.24023437500000000E+00  -0.66894531250000000E-01
         -0.19531250000000000E+00
          0.18359375000000000E+00   0.46630859375000000E-01
         -0.27929687500000000E+00   0.26953125000000000E+00
         -0.13671875000000000E+00
  XGQ =  0.5390625000  1.9062500000

  ;

  Bytes for Z-Filter (13):            50,DA,AE,EC,A1,8F,5B,A1
  Bytes for R-Filter (2B):            60,29,90,60,B9,8D,0C,9E
  Bytes for X-Filter (23):            D0,D8,95,EB,29,95,0B,A5
  Bytes for Gain-factors (30):        31,1A,00,AB
  2nd part of bytes B-Filter (0B):    00,4B,21,24,3A,5C,E1,13
  1st part of bytes B-Filter (03):    AC,BA,4C,23,2D,BA,31,9F
  Bytes for B-filter delay (18):      19,19,11,19
```

```
Run #  1

Z-FILTER calculation results
  Reference impedance for optimization (ZI):
ERZI = 1 RSER = 0.60E+03  CSER = 0.00E+00  RPAR = 0.00E+00  CPAR = 0.00E+0
  Calculated and quantized coefficients:

XZ  =    0.04365  -0.00107  -0.02153  -0.01207   0.02380
XZQ =    0.04297  -0.00098  -0.02148  -0.01196   0.02368
Bytes for Z-Filter (13):    50,DA,AE,EC,A1,8F,5B,A1

RETURN LOSS
```

FREQ (Hz)	loss (dB)	FREQ (Hz)	loss (dB)
100.	20.730	1800.	45.638
200.	26.652	1900.	45.382
300.	30.370	2000.	46.163
400.	34.691	2100.	47.060
500.	36.589	2200.	48.100
600.	40.543	2300.	48.591
700.	44.228	2400.	49.615
800.	47.593	2500.	50.019
900.	51.728	2600.	51.354
1000.	57.415	2700.	54.655
1100.	60.717	2800.	55.913
1200.	53.655	2900.	54.597
1300.	50.692	3000.	53.429
1400.	47.352	3100.	52.410
1500.	46.852	3200.	51.385
1600.	46.116	3300.	49.153
1700.	45.321	3400.	47.402

```
Min. Z-loop reserve:     42.834 dB
       at frequency:     8500.0 Hz
Min. Z-loop mirror signal reserve:     44.918 dB
                     at frequency:    16000.0 Hz
```

```
  Run #  1

  X-FILTER calculation results
    Calculated and quantized coefficients:

  XX  =    1.02160   0.01799  -0.00562   0.01789  -0.00021
  XXQ =    1.02344   0.01758  -0.00586   0.01758  -0.00098
  Bytes for X-Filter (23):    D0,D8,95,EB,29,95,0B,A5
    FREQ        loss                                FREQ        loss
    (Hz)        (dB)                                (Hz)        (dB)
     300.      -0.409                               1900.      -0.219
     400.      -0.387                               2000.      -0.243
     500.      -0.361                               2100.      -0.265
     600.      -0.331                               2200.      -0.286
     700.      -0.300                               2300.      -0.302
     800.      -0.269                               2400.      -0.313
     900.      -0.238                               2500.      -0.317
    1000.      -0.211                               2600.      -0.313
    1100.      -0.188                               2700.      -0.301
    1200.      -0.170                               2800.      -0.280
    1300.      -0.158                               2900.      -0.250
    1400.      -0.154                               3000.      -0.213
    1500.      -0.156                               3100.      -0.170
    1600.      -0.164                               3200.      -0.122
    1700.      -0.179                               3300.      -0.072
    1800.      -0.197                               3400.      -0.021
    1900.      -0.219                               3500.       0.005
    2000.      -0.243                               3600.       0.004

  GX results:
  All attenuation values (in dB) refer to FREF =    1014. Hz

      RLX    SLIC+Z    VREF/VSICOFI    XREF          GX
    -3.00 -  -3.33  -      6.17    -  -0.21    =     -5.63  ideal
    -2.97 =  -3.33  +      6.17    +  -0.21    +     -5.60  quant

  Second byte for Gain:      ,00,AB
  Calculation of transmit transfer function (AD)
  All attenuation values (in dB) refer to FREF =     1014.0 Hz

    Reference impedance for optimization (ZI):
  ERZI = 1 RSER =    600. CSER = 0.000E+00 RPAR =      0. CPAR =
0.000E+0

    FREQ        loss                                FREQ        loss
    (Hz)        (dB)                                (Hz)        (dB)
     100.      44.913                               2000.      -0.055
     200.       0.339                               2100.      -0.082
     300.      -0.121                               2200.      -0.098
     400.      -0.089                               2300.      -0.115
     500.      -0.082                               2400.      -0.126
     600.      -0.073                               2500.      -0.130
```

700.	-0.063	2600.	-0.121
800.	-0.041	2700.	-0.088
900.	-0.021	2800.	-0.057
1000.	-0.004	2900.	-0.008
1100.	0.010	3000.	0.058
1200.	0.028	3100.	0.145
1300.	0.031	3200.	0.269
1400.	0.044	3300.	0.380
1500.	0.032	3400.	0.514
1600.	0.023	3500.	0.730
1700.	0.009	3600.	1.073
1800.	-0.016	3700.	1.695
1900.	-0.032	3800.	3.223

Run # 1

R-FILTER calculation results
Calculated and quantized coefficients:

```
XR  =    0.98877  -0.00364   0.00934   0.00048   0.00679
XRQ =    0.99219  -0.00195   0.00879   0.00000   0.00586
Bytes for R-Filter (2B):    60,29,90,60,B9,8D,0C,9E
```

FREQ (Hz)	loss (dB)	FREQ (Hz)	loss (dB)
300.	-0.014	1900.	0.097
400.	0.006	2000.	0.094
500.	0.029	2100.	0.094
600.	0.053	2200.	0.097
700.	0.077	2300.	0.103
800.	0.099	2400.	0.109
900.	0.118	2500.	0.116
1000.	0.131	2600.	0.122
1100.	0.140	2700.	0.124
1200.	0.144	2800.	0.123
1300.	0.142	2900.	0.118
1400.	0.137	3000.	0.107
1500.	0.129	3100.	0.091
1600.	0.120	3200.	0.071
1700.	0.111	3300.	0.048
1800.	0.103	3400.	0.023
1900.	0.097	3500.	1.003
2000.	0.094	3600.	0.002

GR results:
All attenuation values (in dB) refer to FREF= 1014. Hz

```
   -RLR    SLIC+Z    VSICOFI/VREF    RREF           GR
   3.00 -   3.70  -      -6.17    -   0.13    =      5.34  ideal
   3.03 =   3.70  +      -6.17    +   0.13    +      5.37  quant
```

First byte for Gain (30): 31,1A
Calculation of receive transfer function (DA)

```
  All attenuation values (in dB) refer to FREF =     1014.0 Hz

    Terminating impedance ZI at a,b line!
  ERZI = 1 RSER =    600. CSER = 0.000E+00 RPAR =      0. CPAR =
0.000E+0
```

FREQ (Hz)	loss (dB)	FREQ (Hz)	loss (dB)
100.	35.758	2000.	-0.079
200.	0.033	2100.	-0.079
300.	-0.086	2200.	-0.076
400.	-0.067	2300.	-0.065
500.	-0.064	2400.	-0.054
600.	-0.059	2500.	-0.037
700.	-0.036	2600.	-0.021
800.	-0.024	2700.	-0.009
900.	-0.005	2800.	0.010
1000.	-0.002	2900.	0.025
1100.	0.007	3000.	0.039
1200.	0.011	3100.	0.062
1300.	-0.001	3200.	0.092
1400.	-0.006	3300.	0.143
1500.	-0.024	3400.	0.227
1600.	-0.033	3500.	0.381
1700.	-0.052	3600.	0.671
1800.	-0.061	3700.	1.264
1900.	-0.076	3800.	2.649

```
  Run #    2

  B-FILTER calculation results

    Terminating impedance for optimization (ZL):
  ERZL = 1 RSL  =    600. CSL  = 0.000E+00 RPL  =       0.CPL =
0.000E+0
    Terminating impedance ZL at a,b line!

  Calculated and quantized coefficients:

  XB  =    0.12434  -0.20703   0.24080  -0.06671  -0.19477
           0.18490   0.04671  -0.27867   0.27106  -0.13596
  XBQ =    0.12451  -0.20312   0.24023  -0.06689  -0.19531
           0.18359   0.04663  -0.27930   0.26953  -0.13672
  2nd part of bytes B-Filter (0B):    00,4B,21,24,3A,5C,E1,13
  1st part of bytes B-Filter (03):    AC,BA,4C,23,2D,BA,31,9F
```

```
TRANS HYBRID LOSS

    FREQ        loss                                   FREQ        loss
    (Hz)        (dB)                                   (Hz)        (dB)
     100.      26.747                                  1800.      33.657
     200.      20.474                                  1900.      30.738
     300.      26.448                                  2000.      29.176
     400.      34.852                                  2100.      28.525
     500.      37.946                                  2200.      28.141
     600.      31.736                                  2300.      28.321
     700.      29.294                                  2400.      28.877
     800.      27.968                                  2500.      30.016
     900.      27.463                                  2600.      31.356
    1000.      27.519                                  2700.      32.514
    1100.      28.381                                  2800.      32.774
    1200.      30.012                                  2900.      32.179
    1300.      31.863                                  3000.      31.047
    1400.      36.126                                  3100.      30.917
    1500.      41.026                                  3200.      30.506
    1600.      47.533                                  3300.      31.842
    1700.      37.952                                  3400.      34.411
  Additonal B-filter delay (in seconds): .625E-04
  Bytes for B-filter delay (18):  19,19,11,19
```

The coefficients for the SICOFI can now be extracted from the result file. In the appendix the transfer measurements of the analog line card for the USA-specification can be found.

4 Conclusion

This transformer SLIC fulfills the AT&T specifications in terms of return loss, echo return loss, the gain in transmit and the loss in receive direction. The frequency distortion in both directions fulfill the specification, too. Other specifications, like long lines with a terminating impedance of 600 Ω + 2.16 µF or other levels have not been tested.

5 Appendix

In the appendix you will find

- parts list
- plots of transfer measurements:
  a) return loss
  b) echo return loss
  c) level in transmit and receive direction
  d) frequency distortion in transmit and receive direction.

Parts List

R_1	150 kΩ
R_2	200 kΩ
R_3	15 kΩ
R_4	24 kΩ
R_5	20 kΩ
R_6	75 kΩ
R_7	10 kΩ
R_8	220 Ω
C_1	1 µF
C_2	1 µF
C_3	330 nF
Z_0	243 Ω
OP1	LM356
OP2	LM356

Transformer

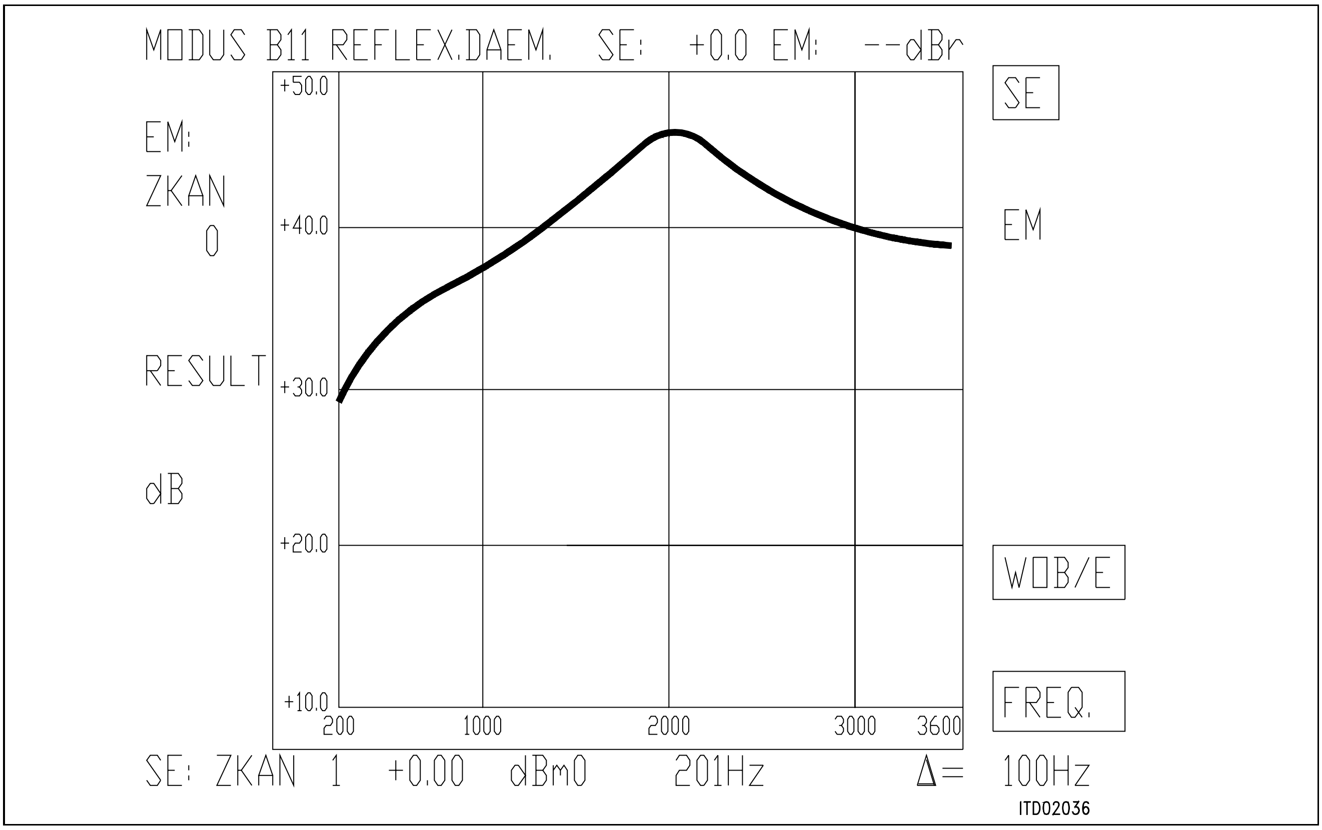


Figure 2

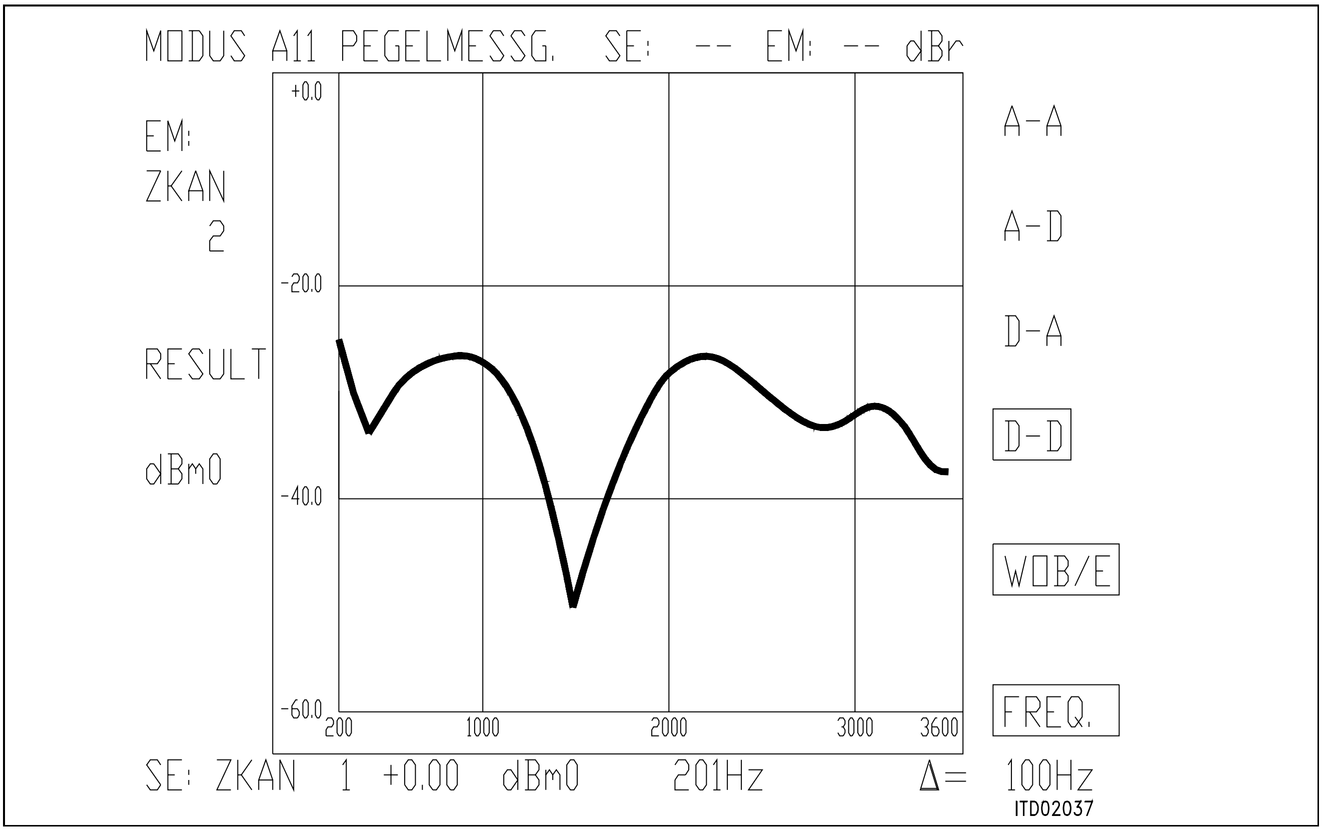


Figure 3

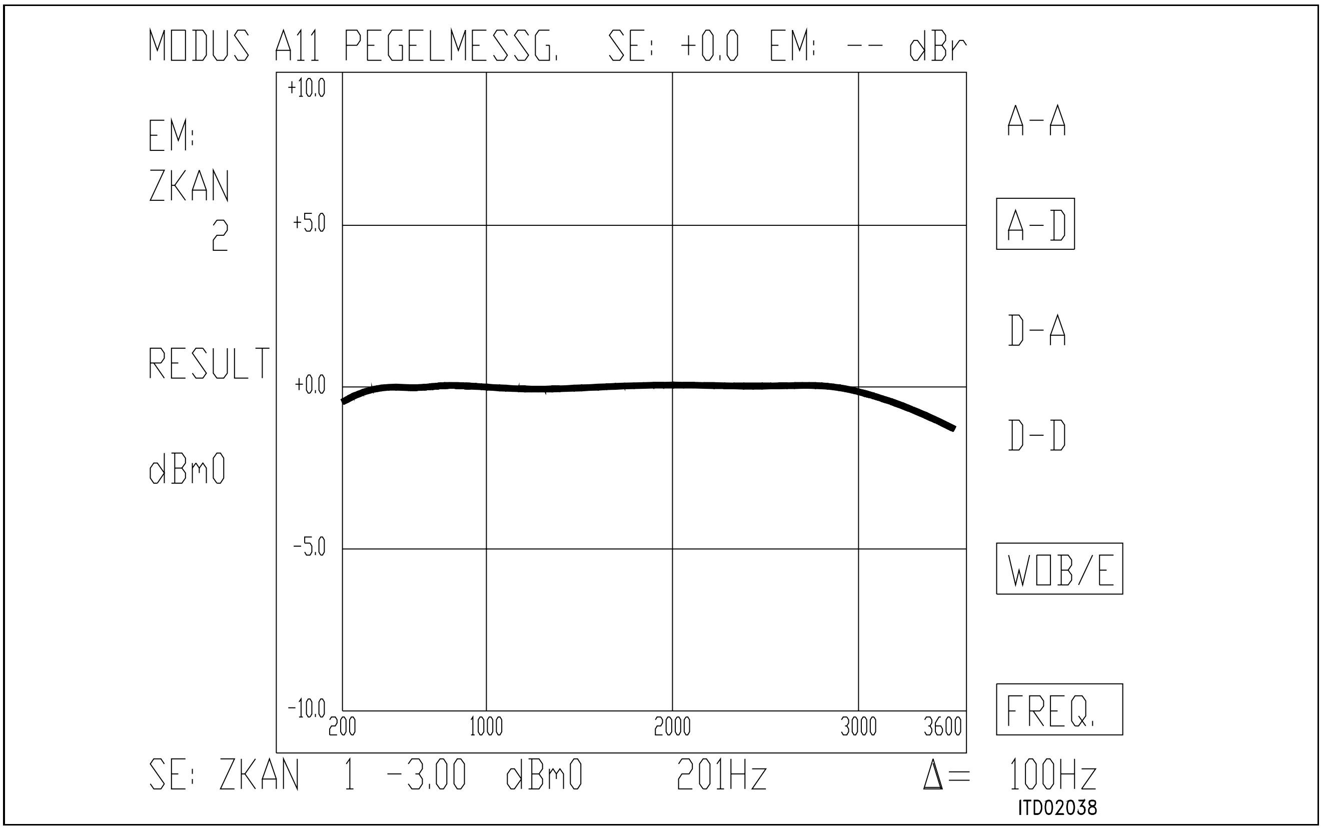


Figure 4

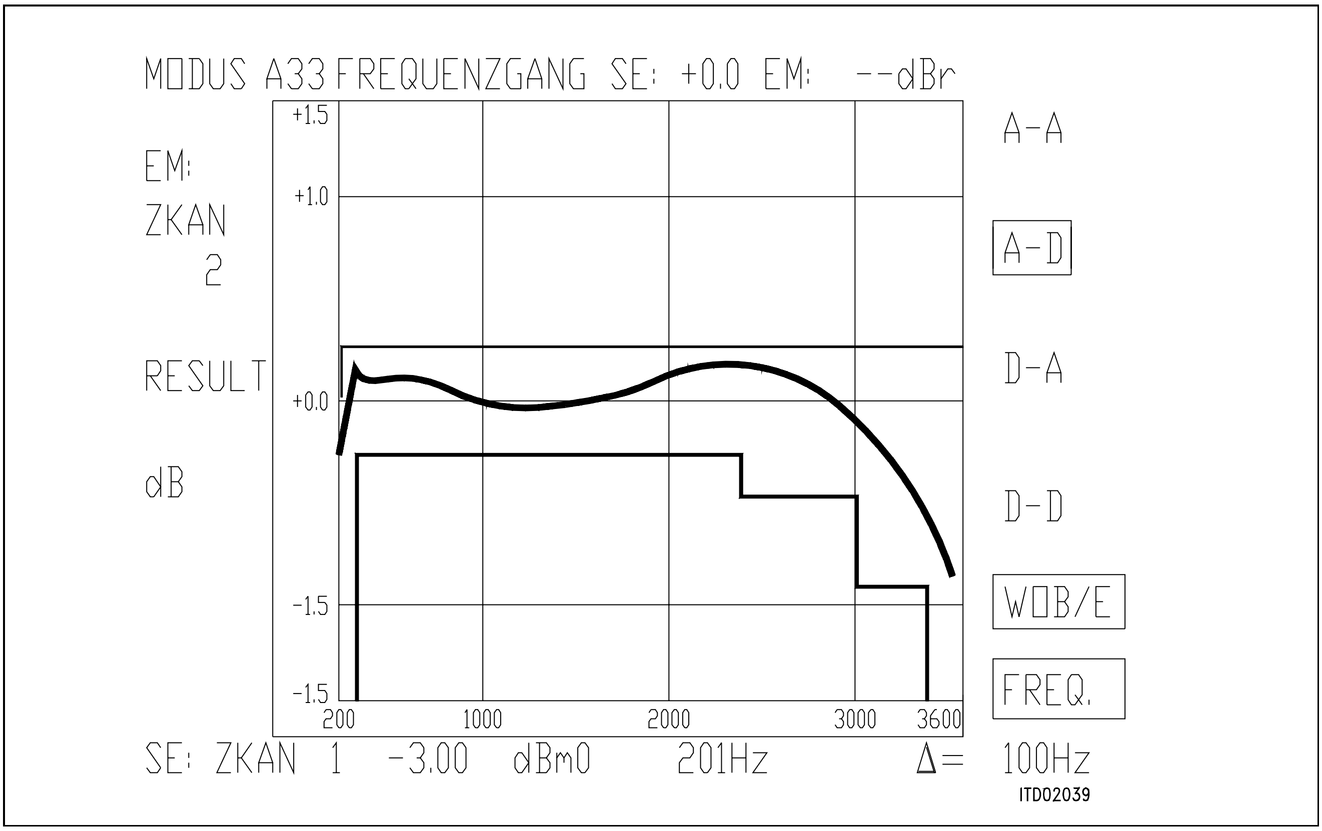


Figure 5

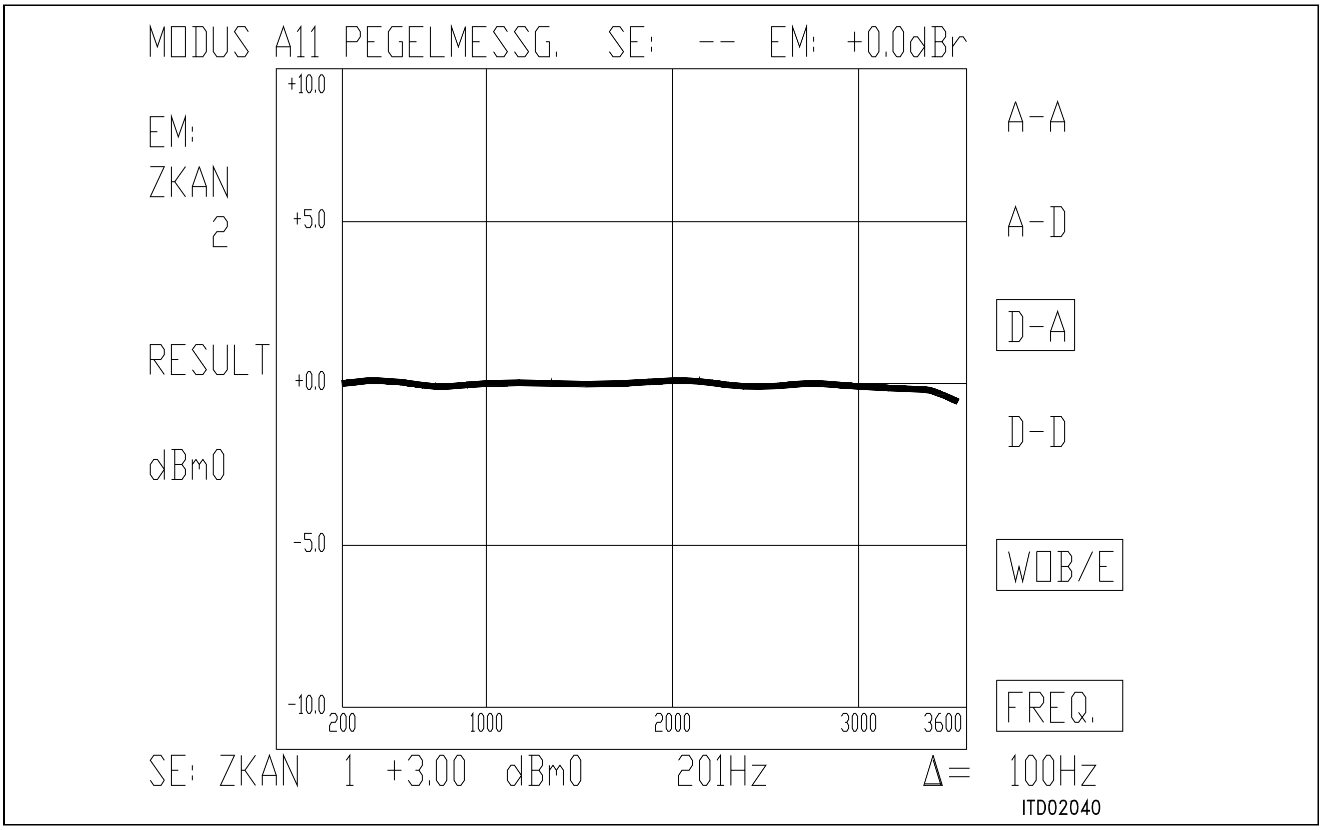


Figure 6

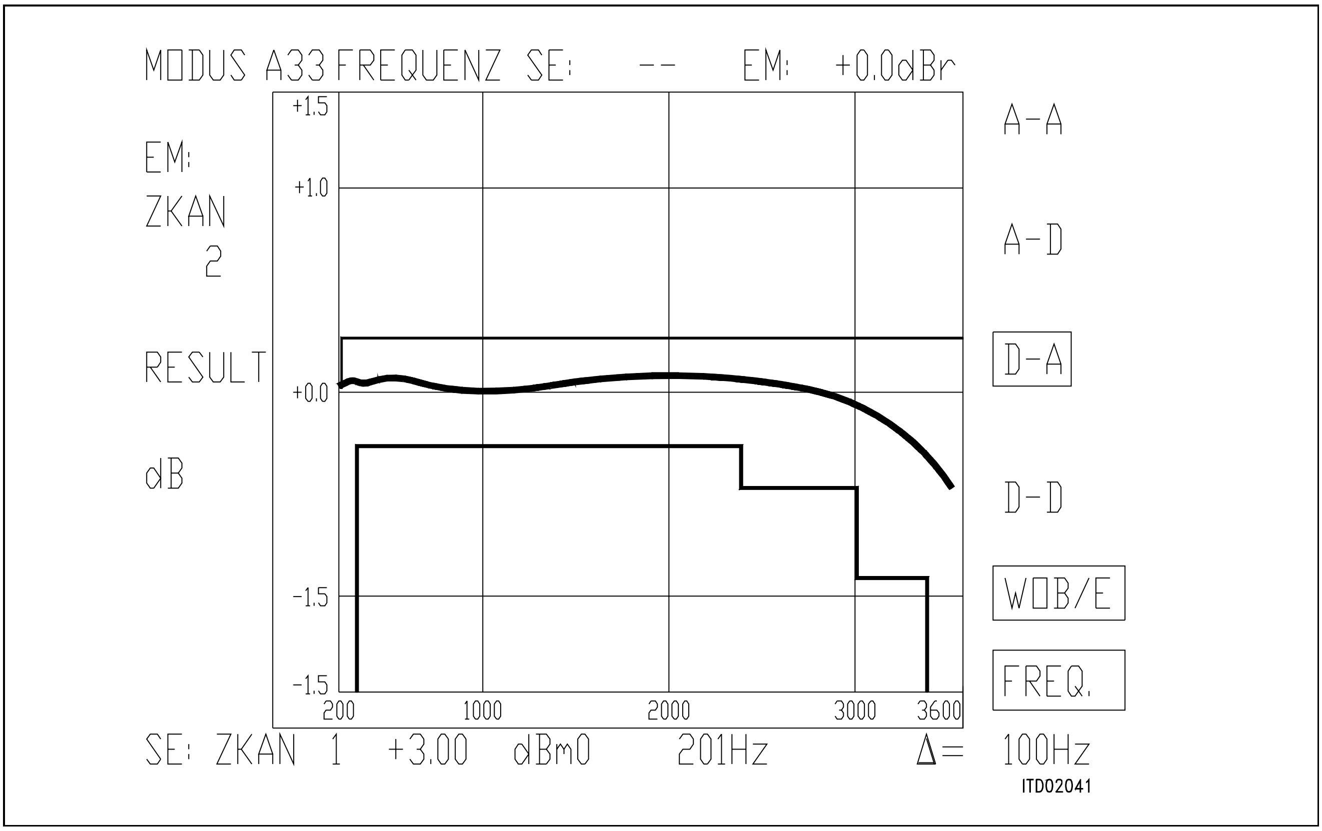


Figure 7

SICOFI® Layout Recommendations for Analog Line-Card Applications

Contents **Page**

1 Introduction

The most important steps in designing a low noise Line Card are to insure that the layout of the circuit components and of the electrical paths guarantees a minimum of cross-coupling between analog and digital signals, and to provide well bypassed and clean power supplies, solid ground plane and minimal lead lenghts between components.

This paper is a general guide line for the layout of an Analog Line Card. In most cases two printed circuit layers are sufficient but with more layers it is possible to separate the different channels, to have a better ground plane and to obtain a smaller printed circuit board.

2 Power Supply

All leads of the power sources should be bypassed to ground on each printed circuit board. At least one electrolytic capacitor is recommended (at least 10 μF) at the point where all power traces from the components join prior to interfacing with the power connector.

3 SICOFI® Decoupling

It is recommended to connect a bypass filter close to each SICOFI composed of an electrolytic capacitor (10 μF) in parallel to a ceramic capacitor (e.g. 100 nF) between the power supplies (+ 5 V and – 5 V) and ground. Thus spikes due to digital switching and high frequency components would be filtered out.

The optimum value for the ceramic capacitor is determined by trying and changing the value and observing the noise in each channel.

4 SICOFI® Analog and Digital Ground Pins

The best configuration to minimize the noise is to connect the digital ground pin and the analog ground pin directly under the SICOFI to the analog ground of the printed board.

Definitions: AGND = Analog Ground
DGND = Digital Ground

5 Separation of Digital and Analog Lines

The layout of the traces should be such that the analog signals are separated from the digital clock and data leads as far as possible.

6 Pairing Voice Leads

Analog voice circuit leads should be paired on their layouts so that no interfering circuit paths should be permitted to run parallel to them and/or between them.

7 Structured Form

Arrange the layout for each line trunk or channel circuit on the board in identical form.

8 Crosstalk

Line circuits mounted extremely close to line circuits of adjacent channel increase the possibility of interchannel crosstalk.

9 Connector Pins

Avoid the assignment of adjacent connector pins to analog signals and digital signals or power.

10 Analog and Digital Ground Separation

The optimal grounding configuration except for the SICOFI parts is to maintain separate digital and analog grounds on the circuit boards, and to carry these grounds back to the power supply with a low impedance connection. This keeps the grounds separate over the entire system except at the power supply.

The SICOFI ground pins and the SLIC ground should be connected to AGND (**see figure 1**).

11 Voltage Difference between AGND and DGND

The voltage difference between analog ground leads (AGND) and digital ground leads (DGND) should be kept low.
One method of preventing any substantial voltage difference between leads is to connect two diodes back to back in opposite directions across these two ground leads on each board.

12 High Voltage

No digital or high voltage level (e.g. ringing supply) should run below or in parallel with analog voice frequency connections. If the analog lines are on the top of the printed circuit board, then AGND or power supply leads should be below them on the other side of the board to prevent analog coupling.

13 Ground Plane

The SICOFI should be separated from traces at the bottom of the printed circuit board by a ground plane directly under the device on the component side.

14 Resistance of Ground Leads

Both ground and power supply leads should have as little resistance and inductance as possible.

This can be accomplished by using a ground plane whenever possible. If traces have to be used for ground connections, a minimum width should be maintained for these leads (e.g. 2 mm) and extra large through holes be used when passing the ground connections through the printed circuit board.

15 Ground Loop

Make sure that no ground loops exist on the printed circuit board:

This would be a perfect antenna for all kind of noises.

16 Separation of Paths

Ground separation traces between sensitive leads can be used to avoid cross coupling.

17 Leads with Transients

Relay operation, ringing voltage, surges can produce transients. Leads carrying such signals should be routed well away from both analog and digital circuits on the line card and in backplanes.

18 Plug-in Boards Connector

For plug-in boards, it is recommended to use a connector with different pin lengths. This should help to connect the interface in a distinct order if the board is plugged in under power condition.

The correct order is:

– Super extra long ground pins (allow to discharge the electrostatic charges)
– Extra long pins for power supplies
– Long pins for the clock signals
– Normal pins for the rest of the signals.

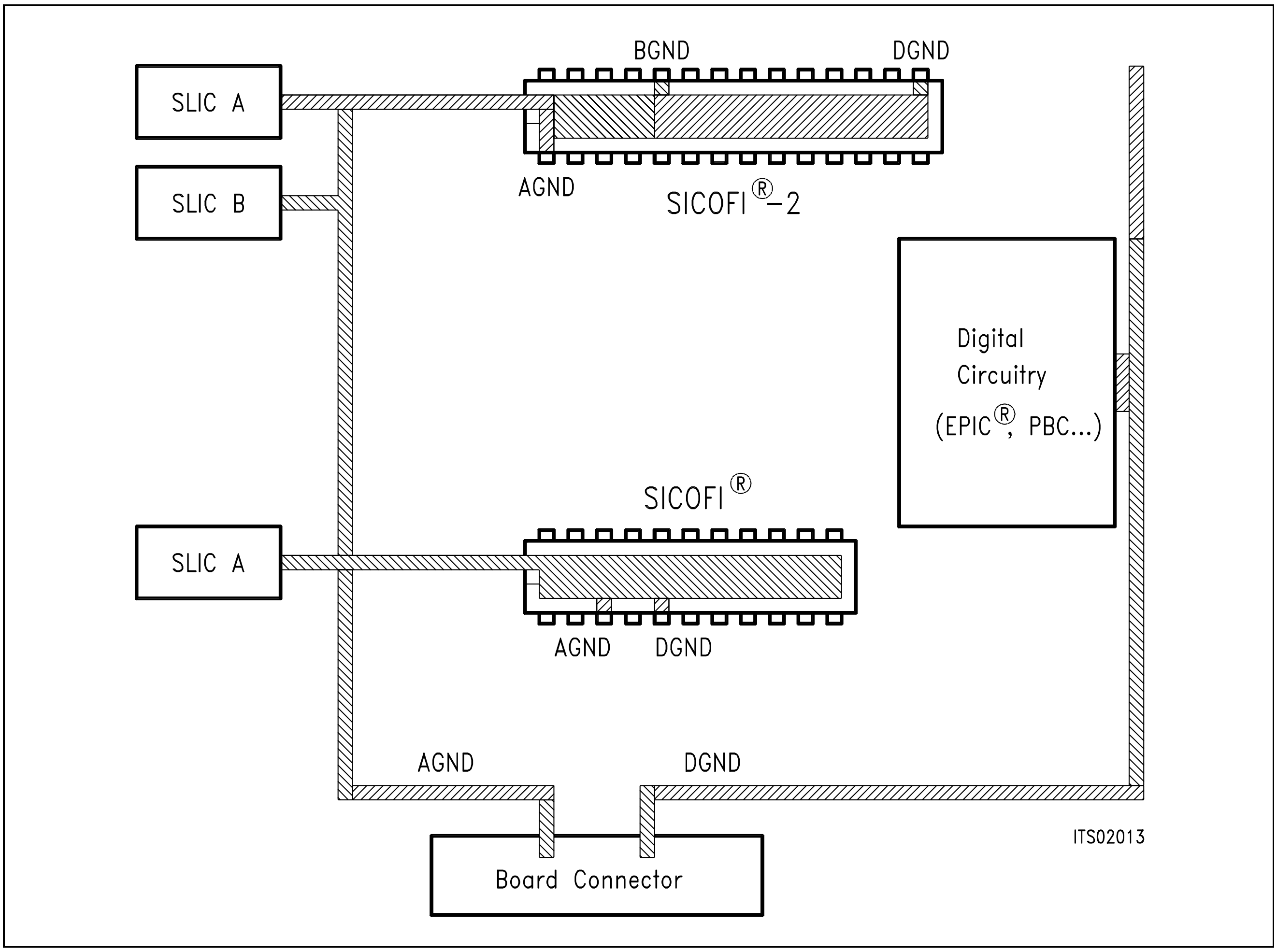


Figure 1

Using SICOFI®-2 (PEB 2260) in IOM®-2 Mode

Contents **Page**

1 Introduction

The SICOFI®-2 can work in two different serial interface modes

→ SLD
→ IOM-2

In this application note necessary programming steps for the SICOFI-2 in an IOM-2 environment are shown. They are documented and explained in a trackfile print out that is used on the SIPB 5000 Userboard System.

So the mnemonics refer directly to the modular architecture of the userboard concept. In order to verify this application note the following hardware equipment is used with a PC:

- Mainboard SIPB 5000
- Line-Card Module SIPB 5121
- SICOFI-2 Board SIPB 5135
- PCM4 Adaptor SIPB 5311a

2 Menu Trackfile Software

In this application note, the SICOFI-2 is connected to two HARRIS-SLICs HC 5502. Basically the SICOFI-2 will be

- identified
- initialized
- programmed.

The used coefficients for filter programming have been derived from the "SICOFI-Application Note HARRIS-SLIC HC 5502".

For any other hardware environment just use the register handling of the SICOFI-2 and modify it for your own application.

3 General Aspects

Using the IOM-2 interface with a data clock of 4.096 MHz (DCL) and an 8-kHz frame signal, eight IOM channels per 125 µs frame on each IOM-line will be offered. These IOM channels can be individually addressed by the SICOFI-2 by its time slots capability. A specific time slot (IOM channel) is selected by pin-strapping at TS1/TS2 pins at the SICOFI-2. This is carried out by external hardware and the switch S1 on the SICOFI-2 Board.

Selected IOM®-2 and TS1/TS2 Pins in Relation Switch S1

Table 1

IOM-2 Channel	TS1	TS2	Position S1
0	0	0	2
1	0	N	3
2	P	0	4
3	P	N	5
4	0	P	6
5	N	0	7
6	P	P	8
7	N	P	9

P = + 5 V, 0 = 0 V, N = – 5 V

Any IOM-channel can be splitted into 4 bytes:

- 2 data channels (8 bits each)
- 1 MONITOR channel (8 bits)
- C/I field (signaling, 6 bits)
- handshake bits MR, MX (2 bits) for MONITOR handshaking.

A basic demand in IOM-2 realizations is, that any connected circuit has to have its own address. For the SICOFI-2 the value 81_H has been specified.

Before any data can be transmitted to the SICOFI-2 via IOM-2 interface (e.g. SOP/COP commands) the specific address has to be sent in order to activate the device.

Additionally any IOM-2 device can identify itself on request. This is done by sending an identify request string, consisting of bytes 80_h, 00_h. The SICOFI-2 responds with bytes 80_h, 80_h.

Note: SICOFI-2 Version 1.x has a minor error that can be temporarily solved by programming a work-around.

Problem: A Write sequence to the SICOFI-2 blocks the next three commands. They will be just ignored.

Work-around: Any Write command is followed by a Read command. The Read command enables correct acception of new commands.

Therefore all programming sequences to the SICOFI-2 end with a SOP-Read command in this application note. As reaction, the SICOFI-2 sends the contents of CR1 back. For versions higher 1.x, the additional SOP-Read command can be omitted.

```
C *******************************************
C *        SICOFI2                         *
C *         with                        *
C *      HARRIS HC 5502                      *
C *******************************************
C
C Hardware: Line Card SIPB 5121
C        SICOFI2 BOARD SIPB 5135
C        PCM4 Adaptor SIPB 5311
C
C configuration:
C        Line Card: via software
C
C        ICOFI 2: S1 in position 5
C
C        PCM4 Adaptor: J1 is open

C *******************************************
C
C SICOFI2 set up in channel 3 of IOM2
C
C        S1 in position 5
C
C *******************************************
C please run the trackfile
C        LC_IOM2.TRK
C first to configure the Line Card

C *******************************************
C *******************************************
C
C selecting EPIC to monitor handshake
C in channel 3
W /LINECA/EPIC/MCHSTR/MFSAR 1C

C *******************************************
C in case of channel 0 MFSAR = 04           *
C            S1 position 2        *
C in case of channel 1 MFSAR = 0C           *
C            S1 position 3        *
C in case of channel 2 MFSAR = 14           *
C            S1 position 4        *
C in case of channel 4 MFSAR = 24           *
C            S1 position 6        *
C in case of channel 5 MFSAR = 2C           *
C            S1 position 7        *
C in case of channel 6 MFSAR = 34           *
C            S1 position 8        *
C in case of channel 7 MFSAR = 3C           *
C            S1 position 9        *
C *******************************************
C
```

```
C channel 3 B1 to PCM timeslot 1
W /LINECA/EPIC/MARSCR/MADR 81
W /LINECA/EPIC/MARSCR/MAAR B0
W /LINECA/EPIC/MARSCR/MACR 71
W /LINECA/EPIC/MARSCR/MADR 0F
W /LINECA/EPIC/MARSCR/MAAR 81
W /LINECA/EPIC/MARSCR/MACR 60
C
C PCM timeslot 1 to channel 3 B1
W /LINECA/EPIC/MARSCR/MADR 01
W /LINECA/EPIC/MARSCR/MAAR 31
W /LINECA/EPIC/MARSCR/MACR 71
C
C channel 3 B2 to PCM timeslot 2
W /LINECA/EPIC/MARSCR/MADR 82
W /LINECA/EPIC/MARSCR/MAAR B1
W /LINECA/EPIC/MARSCR/MACR 71
W /LINECA/EPIC/MARSCR/MADR 0F
W /LINECA/EPIC/MARSCR/MAAR 82
W /LINECA/EPIC/MARSCR/MACR 60
C
C PCM timeslot 2 to channel 3 B2
W /LINECA/EPIC/MARSCR/MADR 02
W /LINECA/EPIC/MARSCR/MAAR 30
W /LINECA/EPIC/MARSCR/MACR 71
C
C
C sicofi identification:
C write to SICOFI2 80h, 00h
W /LINECA/EPIC/MCHSTR/MFFIFO 80
W /LINECA/EPIC/MCHSTR/MFFIFO 00
C EPIC enable receive + transmit
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C EPIC received data
R /LINECA/EPIC/MCHSTR/STAR 26
C first byte from SICOFI2
R /LINECA/EPIC/MCHSTR/MFFIFO 80
R /LINECA/EPIC/MCHSTR/STAR 26
C second byte from SICOFI2
R /LINECA/EPIC/MCHSTR/MFFIFO 80
R /LINECA/EPIC/MCHSTR/STAR 27
C reset FIFO
W /LINECA/EPIC/MCHSTR/CMDR 01
R /LINECA/EPIC/MCHSTR/STAR 25
C
C initialization of sicofi:
C CR4, CR3, CR2, CR1
```

```
C 00h, 00h, 00h, 00h
C for both channels of SICOFI2
C
C SICOFI2 address = 81h
W /LINECA/EPIC/MCHSTR/MFFIFO 81
W /LINECA/EPIC/MCHSTR/MFFIFO C2
W /LINECA/EPIC/MCHSTR/MFFIFO 21
W /LINECA/EPIC/MCHSTR/MFFIFO 04
W /LINECA/EPIC/MCHSTR/MFFIFO 90
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO 47
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the X-filter
C
C GX - filter programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO 30
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO 20
W /LINECA/EPIC/MCHSTR/MFFIFO 92
W /LINECA/EPIC/MCHSTR/MFFIFO 80
W /LINECA/EPIC/MCHSTR/MFFIFO 80
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO 47
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
W /LINECA/EPIC/MCHSTR/MFFIFO 81
```

```
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the GX-
C filter
C
C GR - filter programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO 32
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO A0
W /LINECA/EPIC/MCHSTR/MFFIFO 11
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO 47
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the GR-
C filter
C B - filter part 1 programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO 03
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO C4
W /LINECA/EPIC/MCHSTR/MFFIFO 12
W /LINECA/EPIC/MCHSTR/MFFIFO 23
W /LINECA/EPIC/MCHSTR/MFFIFO 32
W /LINECA/EPIC/MCHSTR/MFFIFO 72
```

```
W /LINECA/EPIC/MCHSTR/MFFIFO B9
W /LINECA/EPIC/MCHSTR/MFFIFO B2
W /LINECA/EPIC/MCHSTR/MFFIFO BA
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO 47
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the B-filter
C part 1
C
C B - filter part 2 programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO 0B
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 97
W /LINECA/EPIC/MCHSTR/MFFIFO FD
W /LINECA/EPIC/MCHSTR/MFFIFO C8
W /LINECA/EPIC/MCHSTR/MFFIFO DD
W /LINECA/EPIC/MCHSTR/MFFIFO 4C
W /LINECA/EPIC/MCHSTR/MFFIFO C2
W /LINECA/EPIC/MCHSTR/MFFIFO BC
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO 47
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
```

```
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the B-filter
C part 2
C
C B-filter delay programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO 18
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO 19
W /LINECA/EPIC/MCHSTR/MFFIFO 19
W /LINECA/EPIC/MCHSTR/MFFIFO 11
W /LINECA/EPIC/MCHSTR/MFFIFO 19
C read back CR1 and power up:
W /LINECA/EPIC/MCHSTR/MFFIFO 67
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the B-filter
C delay
C
C
C SICOFI2 CHANNEL B
C programming the filter
C
C Z-filter programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO 93
```

```
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO 20
W /LINECA/EPIC/MCHSTR/MFFIFO BA
W /LINECA/EPIC/MCHSTR/MFFIFO EA
W /LINECA/EPIC/MCHSTR/MFFIFO 25
W /LINECA/EPIC/MCHSTR/MFFIFO 23
W /LINECA/EPIC/MCHSTR/MFFIFO 41
W /LINECA/EPIC/MCHSTR/MFFIFO C1
W /LINECA/EPIC/MCHSTR/MFFIFO BB
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO C7
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the Z-filter
C
C R - filter programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO AB
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO D0
W /LINECA/EPIC/MCHSTR/MFFIFO C8
W /LINECA/EPIC/MCHSTR/MFFIFO 84
W /LINECA/EPIC/MCHSTR/MFFIFO DC
W /LINECA/EPIC/MCHSTR/MFFIFO B1
W /LINECA/EPIC/MCHSTR/MFFIFO 93
W /LINECA/EPIC/MCHSTR/MFFIFO 02
W /LINECA/EPIC/MCHSTR/MFFIFO 1D
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO C7
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
```

```
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the R-filter
C
C X - filter programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO A3
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO 50
W /LINECA/EPIC/MCHSTR/MFFIFO C8
W /LINECA/EPIC/MCHSTR/MFFIFO B5
W /LINECA/EPIC/MCHSTR/MFFIFO 4A
W /LINECA/EPIC/MCHSTR/MFFIFO C2
W /LINECA/EPIC/MCHSTR/MFFIFO 21
W /LINECA/EPIC/MCHSTR/MFFIFO 04
W /LINECA/EPIC/MCHSTR/MFFIFO 90
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO C7
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is emply
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the X-filter
C
C GX - filters programming
```

```
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO B0
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO 20
W /LINECA/EPIC/MCHSTR/MFFIFO 92
W /LINECA/EPIC/MCHSTR/MFFIFO 80
W /LINECA/EPIC/MCHSTR/MFFIFO 80
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO C7
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the GX-
C filters
C
C GR - filter programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO 32
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO A0
W /LINECA/EPIC/MCHSTR/MFFIFO 11
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO C7
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
```

```
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the GR-
C filters
C
C B - filter part 1 programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO 83
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO C4
W /LINECA/EPIC/MCHSTR/MFFIFO 12
W /LINECA/EPIC/MCHSTR/MFFIFO 23
W /LINECA/EPIC/MCHSTR/MFFIFO 32
W /LINECA/EPIC/MCHSTR/MFFIFO 72
W /LINECA/EPIC/MCHSTR/MFFIFO B9
W /LINECA/EPIC/MCHSTR/MFFIFO B2
W /LINECA/EPIC/MCHSTR/MFFIFO BA
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO C7
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the B-filter
C part 1
C
C B - filter part 2 programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO 8B
C coefficients:
```

```
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 97
W /LINECA/EPIC/MCHSTR/MFFIFO FD
W /LINECA/EPIC/MCHSTR/MFFIFO C8
W /LINECA/EPIC/MCHSTR/MFFIFO DD
W /LINECA/EPIC/MCHSTR/MFFIFO 4C
W /LINECA/EPIC/MCHSTR/MFFIFO C2
W /LINECA/EPIC/MCHSTR/MFFIFO BC
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO C7
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the B-filter
C part 2
C
C B - filter delay programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO 98
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO 19
W /LINECA/EPIC/MCHSTR/MFFIFO 19
W /LINECA/EPIC/MCHSTR/MFFIFO 11
W /LINECA/EPIC/MCHSTR/MFFIFO 19
C read back CR1 and power up:
W /LINECA/EPIC/MCHSTR/MFFIFO E7
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
```

```
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the B-filter
C delay
C
C SICOFI2 is programmed and power up
C of both channels
C
C ***********************************
C      activation of HARRIS-SLIC
C          /RC = 1 ,/PD = 1

C ***********************************
C
C ADR, C3A, CI2, CI1, C2, C1, 1, 1
C 1/0, X, X, X,/RC,/PD, 1, 1
C
C  SICOFI2 channel A
W /LINECA/EPIC/MARSCR/MADR 0F
W /LINECA/EPIC/MARSCR/MAAR 38
W /LINECA/EPIC/MARSCR/MACR 48
C
C  SICOFI2 channel B
W /LINECA/EPIC/MARSCR/MADR 8F
W /LINECA/EPIC/MARSCR/MAAR 38
W /LINECA/EPIC/MARSCR/MACR 48
C
C end of activation
C
C ***********************************
C    read the signaling information
C              /GKD, /SHD
C         from the HARRIS-SLIC

C ***********************************
C
C switch on the LAST-LOOK-LOGIC
C
W /LINECA/EPIC/MARSCR/CMDR 40
C
C CI2B, CI1B, I1B, CI2A, CI1A, I1A, 1, 1
C /GKD,/GKD,/SHD,/GKD,/GKD,/SHD, 1, 1
```

```
C  channel B , channel A , 1, 1
C
C SLIC at SICOFI2 channel B+A
C
C MADR = FF A= on hook B= on hook
C MADR = FB A=off hook B= on hook
C MADR = DF A= on hook B=off hook
C MADR = DB A=off hook B=off hook
C
W /LINECA/EPIC/MARSCR/MAAR B8
W /LINECA/EPIC/MARSCR/MACR C8
R /LINECA/EPIC/MARSCR/MADR D8
C both terminals are off-hook and no
C ground key
C end of trackfile
```

DAML Simulation Using the SIPB 5000 Userboard System

Contents **Page**

1 Introduction

This application note describes the simulation of a Digital Added Main Line (DAML) using components of the Siemens ISDN PC User Board system SIPB 5000.

In practice during the transition period from a pure analog telephone network to the future Integrated Services Digital Network (ISDN) the DAML provides a cost-effective provisional extension (doubling) of traffic capability of existing installations.

DAML is a concept of integrating digital transmission into an existing analog communication system with the aim of increasing its performance. It provides telephony facility for two independent analog subscribers on a single local wire pair. The transmission principle uses echo cancellation and message recovery according to American National Standards Institute (ANSI) T1E1 specification for the U interface (2B1Q line code).

This application note is not only to show the simplicity of insertion of this feature but also the high quality of the extra gained transmission channel. In addition this example is a good introduction to digital communication and to the flexibility in application of the SIPB system components.

For simulation a subscriber loop is reproduced using a TE and a NTS station. The necessary hardware is listed in section 2. Special information on setting up and running the test equipment are given in section 3.

As from versatility reasons several features of the ISDN components are left for software programming, the respective initializing procedure is performed by track files which are to be found in section 5. A PC AT serves for the interface to the user. Using the Siemens Menu Software which enables access down to the register level of the employed components gives deep insight into the operational procedure of such a set-up.

2 Required Hardware

Figure 1 shows the set-up of a subscriber loop between a NTS and a TE, where a DAML is to be simulated. The hardware required at the terminals differs slightly according to the peculiar configuration:

NTS-Configuration:

1 ITAC® Module SIPB 5140
1 Audio Interface Module V2.0 SIPB 5130
1 Layer-2 Module SIPB 5120-2
1 IEC-Q Reference Module LT SIPB 2091
1 SICOFI®-2 Board SIPB 5135
2 Analog Telephone Sets
2 SLICs (HARRIS HC 5502)
1 Adapter cable

TE-Configuration:

1 Audio Interface Module V2.0 SIPB 5130
1 Layer-2 Module SIPB 5120-2
1 IEC-Q Reference Module NT SIPB 2091
1 SICOFI®-2 Board SIPB 5135
2 Analog Telephone Sets
2 SLICs (HARRIS HC 5502)
1 Adapter Cable

As the SICOFI-2 Board has been developed originally for connection to the Line Card Module, and the Audio Interface Module at its Service Access Connector (SAC) shows a differring pinning, a peculiar Adapter Cable has to be used. The particular design depends on wether the RESET of the SICOFI-2 will be used or not (including an inverter stage or not). A schematic of these Adapter Cables is shown in **figure 2**.

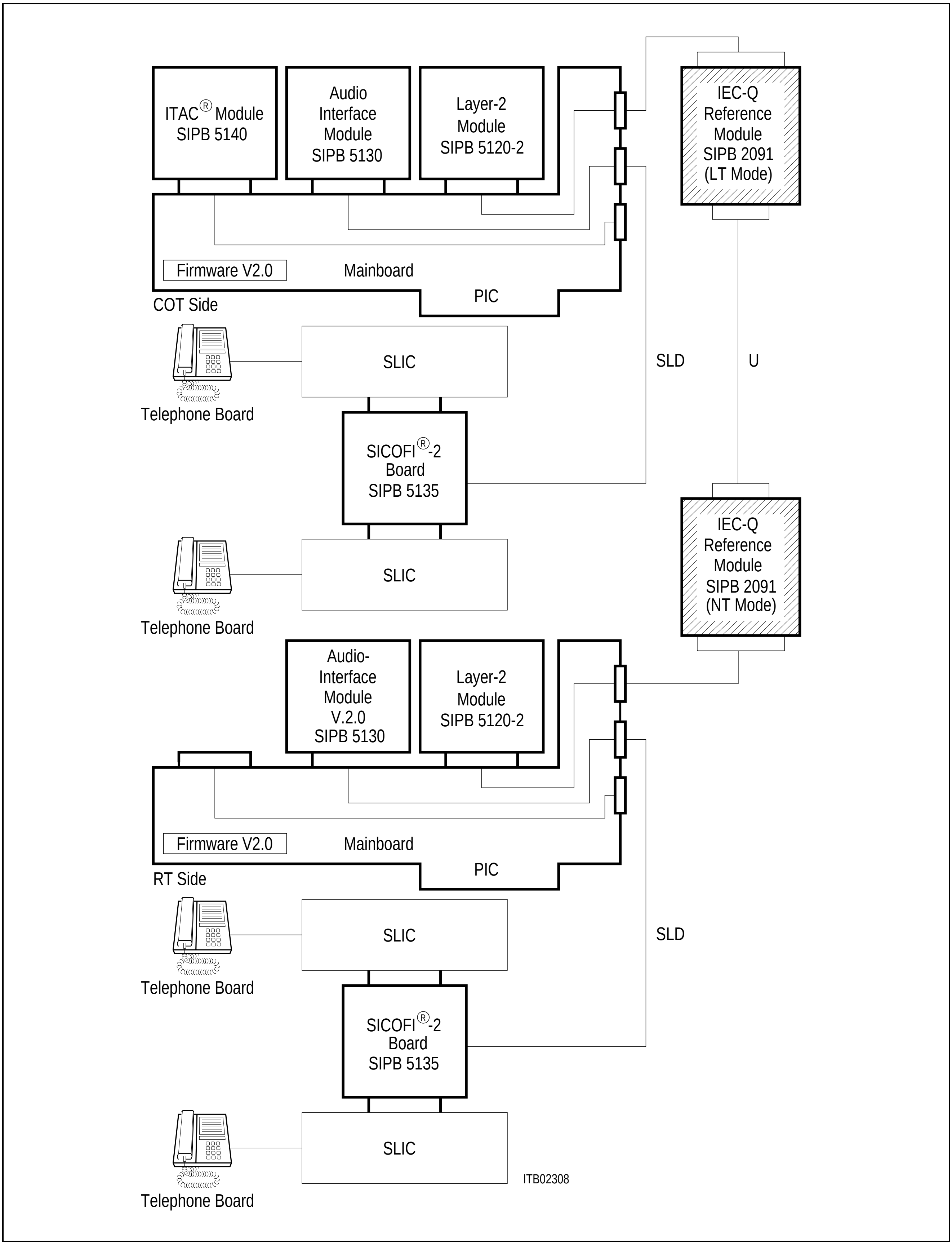
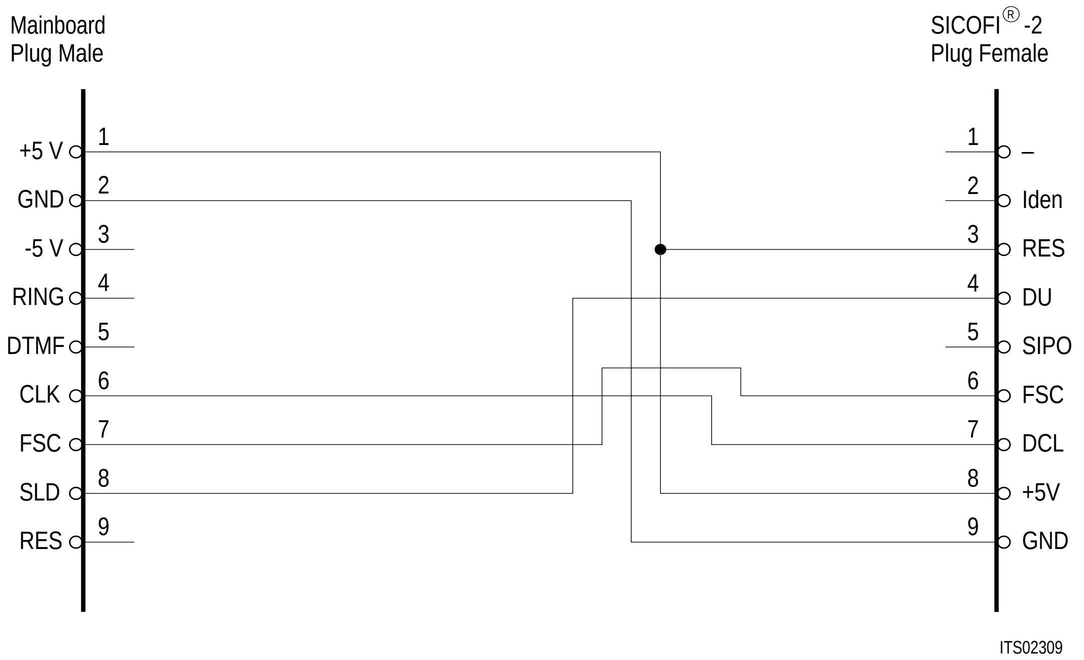


Figure 1
Set-Up for Simulating a DAML

Top: RESET not connected to the SICOFI-2 Board, bottom: RESET connected to the SICOFI-2 Board



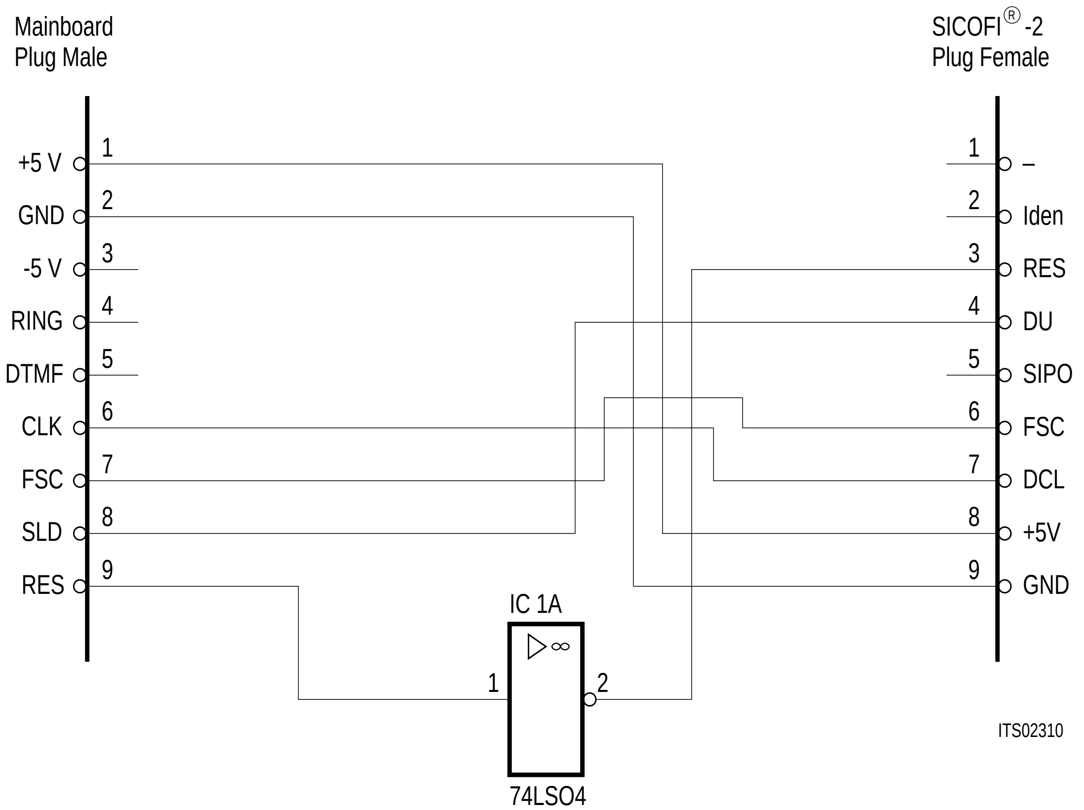


Figure 2

Wiring of the SICOFI-2 Adapter Cable

3 Operational Information

The modules of the NTS and TE configurations each are plugged to the Add-on Module Connectors (AMC) of a SIPB 5000 Mainboard, which in turn are inserted into an expansion slot of an IBM AT or compatible (For safety reasons please refer to the respective instructions of the User Manual of the computer manufacturer for internal installation procedures).

Before insertion into the PC, the modules are configured to the particular mode:

NTS:

Layer-2 Module	all DIP switches to OFF position
Audio Interface Module	Switches S1 … 4 to OFF position no jumpers set

TE:

Layer-2 Module	all DIP switches to OFF position
Audio Interface Module	Switches S1, S2, S4 to OFF position Switch S3 to ON position no jumpers set

The IEC-Q Reference Boards are connected externally to that SAC which corresponds to the AMC the Layer-2 Modules are plugged to. Similarly the SICOFI-2 Boards bearing two SLICs each are connected to the SAC corresponding to the Audio Interface Modules using the peculiar Adapter Cable (**refer to figure 1**).

Telephone sets and SLICs, and IEC-Q Reference Boards are interconnected using single wire pairs (a/b lines and U interface respectively).

The configuration of IEC-Q Reference Boards depends on the particular mode:

LT:

DIP switches 1 … 3 to OFF position
DIP switches 4 … 7 to ON position
Jumpers J1, J2 set, Jumper J5 open
Jumpers J3, J4 set to position a-b

TE:

DIP switch S1 to OFF position
DIP switches 2 … 7 to ON position
Jumpers J1, J2 set

At the SICOFI-2 Board the rotary switch S1 is put to position 0 (DIP switch S2 don't care).

4 Glossary

AMC	Add-on module connector
DAML	Digital added main line
IEC-Q	ISDN echo cancellation circuit conforming to 2B1Q transmission mode
ISDN	Integrated services digital network
ITAC	ISDN terminal adapter circuit
LT	Line termination
NT	Network termination
NTS	Network termination on S bus
SAC	Service access connector
SICOFI	Signal processing codec filter
SICOFI-2	Dual channel codec filter
SIPB	Siemens ISDN PC User Board (system)
SLIC	Subscriber line circuit
TE	Terminal equipment
2B1Q	Transmission mode requiring 120-kHz bandwidth

5 Track Files

Note: The filter coefficients of the SICOFI are calculated to meet the specifications of the Deutsche Bundespost.

5.1 Track File DAMLCOT.TRK for COT Side

```
C ****************************************
C this track file supports DAML applic-
C ations with the SICOFI2 board SIPB 5135
C and fits to the track file D A M L
C (RT = Remote Terminal)
C
C
C note:
C - please use audio module Version 2.0
C - please use firmware Version V2.0
C - please use a adaptor cable for SICOFI2
C   board SIPB 5135
C
C - start with this track file!
C ****************************************
C
C reset and deactivation the IECQ
W /LI_NTS/ICCB/SERIAL/CIXR 47
R /LI_NTS/ICCB/SERIAL/ISTA 04
R /LI_NTS/ICCB/SERIAL/CIRR 06
R /LI_NTS/ICCB/SERIAL/ISTA 00
W /LI_NTS/ICCB/SERIAL/CIXR 40
R /LI_NTS/ICCB/SERIAL/ISTA 04
R /LI_NTS/ICCB/SERIAL/CIRR 3E
R /LI_NTS/ICCB/SERIAL/ISTA 00
C
C S T O P - S T O P - S T O P
C now go to DAML RT side
C FOR reset and deactivation of RT
C
C
C activation of U interface
W /LI_NTS/ICCB/SERIAL/CIXR 60
R /LI_NTS/ICCB/SERIAL/ISTA 04
R /LI_NTS/ICCB/SERIAL/CIRR 22
C
C W A I T - W A I T - W A I T
C several seconds, max. 15sec,
C for adaption of echo cancellor
C and equalizer
C
R /LI_NTS/ICCB/SERIAL/ISTA 04
R /LI_NTS/ICCB/SERIAL/CIRR 1E
R /LI_NTS/ICCB/SERIAL/CIRR 1C
R /LI_NTS/ICCB/SERIAL/CIRR 1C
```

```
C
C S T O P - S T O P - S T O P
C go back to RT side
C for ACTIVATION INDICATION (AI)
C
R /LI_NTS/ICCB/SERIAL/ISTA 04
R /LI_NTS/ICCB/SERIAL/CIRR 32
R /LI_NTS/ICCB/SERIAL/ISTA 00
R /LI_NTS/ICCB/SERIAL/CIRR 30
R /LI_NTS/ICCB/SERIAL/CIRR 30
R /LI_NTS/ICCB/SERIAL/CIRR 30
R /LI_NTS/ICCB/SERIAL/ISTA 00
C
C switch the proper port of ICC
W /LI_NTS/ICCB/SERIAL/SPCR 45
D
C programming of SICOFI2
C the configuration register CR3-CR1
D
B 05
B 00
B 00
B 00
B 85
B 00
B 00
B 00
X /LI_NTS/ICCB/BUS/CONTR
C
C the Z-filters
D
B 13
B 20
B BA
B EA
B 25
B 23
B 41
B C1
B BB
B 93
B 20
B BA
B EA
B 25
B 23
B 41
B C1
B BB
X /LI_NTS/ICCB/BUS/CONTR
C
C the R-filters
```

```
D
B 2B
B D0
B C8
B 84
B DC
B B1
B 93
B 02
B 1D
B AB
B D0
B C8
B 84
B DC
B B1
B 93
B 02
B 1D
X /LI_NTS/ICCB/BUS/CONTR
D
C
C the X-filters
D
B 23
B 50
B C8
B B5
B 4A
B C2
B 21
B 04
B 90
B A3
B 50
B C8
B B5
B 4A
B C2
B 21
B 04
B 90
X /LI_NTS/ICCB/BUS/CONTR
C
C the B-filters part 1
D
B 0B
B 00
B 97
B FD
B C8
B DD
```

```
B 4C
B C2
B BC
B 8B
B 00
B 97
B FD
B C8
B DD
B 4C
B C2
B BC
X /LI_NTS/ICCB/BUS/CONTR
C
C the B-filters part 2
D
B 03
B C4
B 12
B 23
B 32
B 72
B B9
B B2
B BA
B 83
B C4
B 12
B 23
B 32
B 72
B B9
B B2
B BA
X /LI_NTS/ICCB/BUS/CONTR
C
C the B-filters delay
D
B 18
B 19
B 19
B 11
B 19
B 98
B 19
B 19
B 11
B 19
X /LI_NTS/ICCB/BUS/CONTR
C
C the GX filters
D
```

```
B 30
B 20
B 92
B 80
B 80
B B0
B 20
B 92
B 80
B 80
X /LI_NTS/ICCB/BUS/CONTR
C
C the GR-filters
D
B 3A
B A0
B 11
B BA
B A0
B 11
X /LI_NTS/ICCB/BUS/CONTR
C
C switch on all filters
D
B 25
B 00
B 00
B FC
B A5
B 00
B 00
B FC
X /LI_NTS/ICCB/BUS/CONTR
C
C activation of the HARRIS-SLIC
W /LI_NTS/ICCB/SERIAL/SSCX 33
C
C now you can talk
C
C ****************************************
C END of TRACK FILE
C ****************************************
```

5.2 Track File DAMLRT.TRK for RT Side

```
C ****************************************
C this track file supports DAML applic-
C ations with the SICOFI2 board SIPB 5135
C and fits to the track file D A M L
C (COT = Central Office Terminal)
C
C
C note:
C - please use audio module Version 2.0
C - please use firmware Version V2.0
C - please use a adaptor cable for SICOFI2
C   board SIPB 5135
C
C - start with DAML (COT)!
C ****************************************
C
C  reset and deactivate the IECQ
W /LI_TE/ICCB/SERIAL/SPCR 80
W /LI_TE/ICCB/SERIAL/CIXR 47
W /LI_TE/ICCB/SERIAL/SPCR 00
R /LI_TE/ICCB/SERIAL/ISTA 04
R /LI_TE/ICCB/SERIAL/CIRR 1E
R /LI_TE/ICCB/SERIAL/ISTA 04
R /LI_TE/ICCB/SERIAL/CIRR 02
R /LI_TE/ICCB/SERIAL/ISTA 00
W /LI_TE/ICCB/SERIAL/CIXR 7C
R /LI_TE/ICCB/SERIAL/ISTA 04
R /LI_TE/ICCB/SERIAL/CIRR 3E
R /LI_TE/ICCB/SERIAL/ISTA 00
C
C  S T O P - S T O P - S T O P
C  go back to DAML COT side
C  for activation the U interface
C
R /LI_TE/ICCB/SERIAL/ISTA 04
R /LI_TE/ICCB/SERIAL/CIRR 22
R /LI_TE/ICCB/SERIAL/ISTA 00
R /LI_TE/ICCB/SERIAL/CIRR 20
R /LI_TE/ICCB/SERIAL/ISTA 00
C
C  ACTIVATION INDICATION (AI)
C
W /LI_TE/ICCB/SERIAL/CIXR 70
R /LI_TE/ICCB/SERIAL/ISTA 04
R /LI_TE/ICCB/SERIAL/CIRR 32
R /LI_TE/ICCB/SERIAL/CIRR 30
R /LI_TE/ICCB/SERIAL/CIRR 30
R /LI_TE/ICCB/SERIAL/ISTA 00
C
C  now the U interface is transparent
```

```
C
C
C switch the proper port in ICC
W /LI_TE/ICCB/SERIAL/SPCR 45
W /LI_TE/ICCB/SERIAL/SSCX 00
C
C programming of SICOFI2
C the configuration register CR3-CR1
D
B 05
B 00
B 00
B 00
B 85
B 00
B 00
B 00
X /LI_TE/ICCB/BUS/CONTR
C
C the Z-filters
D
B 13
B 20
B BA
B EA
B 25
B 23
B 41
B C1
B BB
B 93
B 20
B BA
B EA
B 25
B 23
B 41
B C1
B BB
X /LI_TE/ICCB/BUS/CONTR
C
C the R-filters
D
B 2B
B D0
B C8
B 84
B DC
B B1
B 93
B 02
B 1D
```

```
B AB
B D0
B C8
B 84
B DC
B B1
B 93
B 02
B 1D
X /LI_TE/ICCB/BUS/CONTR
D
C
C the X-filters
D
B 23
B 50
B C8
B B5
B 4A
B C2
B 21
B 04
B 90
B A3
B 50
B C8
B B5
B 4A
B C2
B 21
B 04
B 90
X /LI_TE/ICCB/BUS/CONTR
C
C the B-filters part 1
D
B 0B
B 00
B 97
B FD
B C8
B DD
B 4C
B C2
B BC
B 8B
B 00
B 97
B FD
B C8
B DD
B 4C
```

```
B C2
B BC
X /LI_TE/ICCB/BUS/CONTR
C
C the B-filters part 2
D
B 03
B C4
B 12
B 23
B 32
B 72
B B9
B B2
CB BA
B 83
B C4
B 12
B 23
B 32
B 72
B B9
B B2
B BA
X /LI_TE/ICCB/BUS/CONTR
C
C the B-filters delay
D
B 18
B 19
B 19
B 11
B 19
B 98
B 19
B 19
B 11
B 19
X /LI_TE/ICCB/BUS/CONTR
C
C the GX filters
D
B 30
B 20
B 92
B 80
B 80
B B0
B 20
B 92
B 80
B 80
```

```
X /LI_TE/ICCB/BUS/CONTR
C
C the GR-filters
D
B 3A
B A0
B 11
B BA
B A0
B 11
X /LI_TE/ICCB/BUS/CONTR
C
C switch on all filters
D
B 25
B 00
B 00
B FC
B A5
B 00
B 00
B FC
X /LI_TE/ICCB/BUS/CONTR
C
C activation of the HARRIS-SLIC
W /LI_TE/ICCB/SERIAL/SSCX 33
C
C now you can talk
C
C ****************************************
C END of TRACK FILE
C ****************************************
```